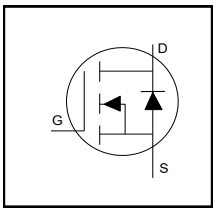
**StrongIRFET™ power MOSFET**

| | |
|---|---|
| $V_{DSS}$ | 40V |
| $R_{DS(on)}$ typ. | 1.9mΩ |
| max | 2.4mΩ |
| $I_{D\ (Silicon\ Limited)}$ | 180A① |
| $I_{D\ (Package\ Limited)}$ | 90A |

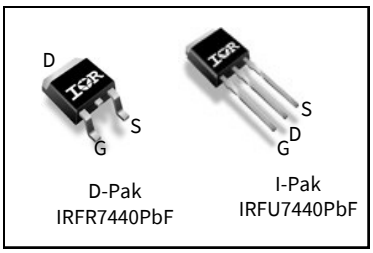



**Application**

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Electronic ballast applications
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant containing no Lead, no Bromide, and no Halogen




D-Pak
IRFR7440PbF

I-Pak
IRFU7440PbF

| G | D | S |
|---|---|---|
| Gate | Drain | Source |

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRFR7440PbF | D-Pak | Tube | 75 | IRFR7440PbF |
| | | Tape and Reel | 2000 | IRFR7440TRPbF |
| IRFU7440PbF | I-Pak | Tube | 75 | IRFU7440PbF |

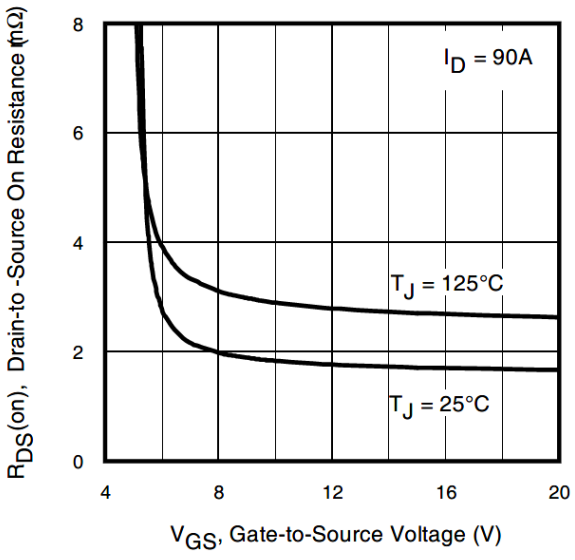



**Fig 1.** Typical On-Resistance vs. Gate Voltage

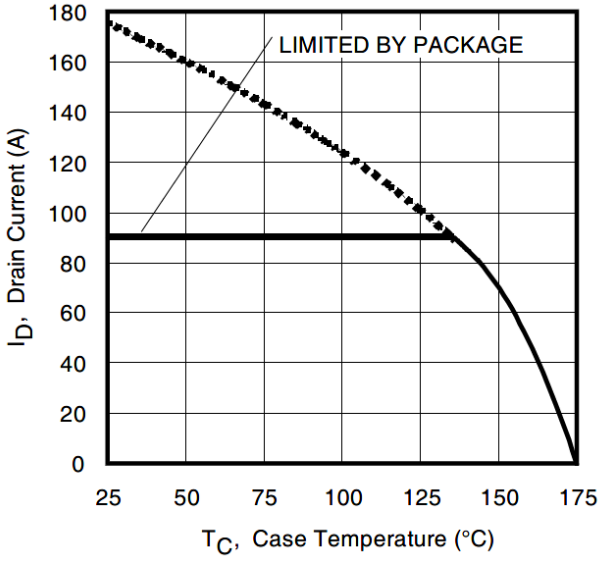



**Fig 2.** Maximum Drain Current vs. Case Temperature

## Absolute Maximum Rating

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 180① | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 125① | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited) | 90 | |
| $I_{DM}$ | Pulsed Drain Current ② | 760 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 140 | W |
| | Linear Derating Factor | 0.95 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| dv/dt | Peak Diode Recovery④ | 4.4 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |

## Avalanche Characteristics

| | | | |
|---|---|---|---|
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ③ | 160 | mJ |
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ⑩ | 376 | |
| $I_{AR}$ | Avalanche Current ② | See Fig 15, 16, 23a, 23b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ② | | mJ |

## Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑨ | --- | 1.05 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑧ | --- | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient ⑨ | --- | 110 | |

## Static @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | --- | --- | V | $V_{GS}$ = 0V, $I_D$ = 250µA ② |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | --- | 28 | --- | mV/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | --- | 1.9 | 2.4 | mΩ | $V_{GS}$ = 10V, $I_D$ = 90A ⑤ |
| | | --- | 2.8 | --- | | $V_{GS}$ = 6.0V, $I_D$ = 50A ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.2 | 3.0 | 3.9 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 100µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | --- | --- | 1.0 | µA | $V_{DS}$ = 40V, $V_{GS}$ = 0V |
| | | --- | --- | 150 | | $V_{DS}$ = 40V,$V_{GS}$ = 0V,$T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | --- | --- | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | --- | --- | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Gate Resistance | --- | 2.6 | --- | Ω | |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 90A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.04mH, $R_G$ = 50Ω, $I_{AS}$ = 90A, $V_{GS}$ =10V.

④ $I_{SD}$ ≤ 100A, di/dt ≤ 1306A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.please refer to application note to AN-994

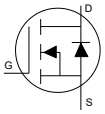
⑨ $R_\theta$ is measured at $T_J$ approximately 90°C.

⑩ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 1mH, $R_G$ = 50Ω, $I_{AS}$ = 27A, $V_{GS}$ =10V.

**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 280 | --- | --- | S | $V_{DS}$ = 10V, $I_D$ =90A |
| $Q_g$ | Total Gate Charge | --- | 89 | 134 | nC | $I_D$ = 90A<br>$V_{DS}$ = 20V<br>$V_{GS}$ = 10V |
| $Q_{gs}$ | Gate-to-Source Charge | --- | 26 | --- | | |
| $Q_{gd}$ | Gate-to-Drain Charge | --- | 26 | --- | | |
| $Q_{sync}$ | Total Gate Charge Sync. (Qg– Qgd) | --- | 63 | --- | | |
| $t_{d(on)}$ | Turn-On Delay Time | --- | 11 | --- | ns | $V_{DD}$ = 20V<br>$I_D$ = 30A<br>$R_G$= 2.7Ω<br>$V_{GS}$ = 10V⑤ |
| $t_r$ | Rise Time | --- | 39 | --- | | |
| $t_{d(off)}$ | Turn-Off Delay Time | --- | 51 | --- | | |
| $t_f$ | Fall Time | --- | 34 | --- | | |
| $C_{iss}$ | Input Capacitance | --- | 4610 | --- | pF | $V_{GS}$ = 0V<br>$V_{DS}$ = 25V<br>$f$ = 1.0MHz, See Fig.7 |
| $C_{oss}$ | Output Capacitance | --- | 690 | --- | | |
| $C_{rss}$ | Reverse Transfer Capacitance | --- | 460 | --- | | |
| $C_{oss\ eff.(ER)}$ | Effective Output Capacitance (Energy Related) | --- | 855 | --- | | $V_{GS}$ = 0V, VDS = 0V to 32V⑦ |
| $C_{oss\ eff.(TR)}$ | Output Capacitance (Time Related) | --- | 1210 | --- | | $V_{GS}$ = 0V, VDS = 0V to 32V⑥ |

**Diode Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | --- | --- | 180① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ② | --- | --- | 760 | | |
| $V_{SD}$ | Diode Forward Voltage | --- | 0.9 | 1.3 | V | $T_J$ = 25°C,$I_S$ = 90A,$V_{GS}$ = 0V ⑤ |
| $t_{rr}$ | Reverse Recovery Time | --- | 34 | --- | ns | $T_J$ = 25°C |
| | | --- | 35 | --- | | $T_J$ = 125°C |
| $Q_{rr}$ | Reverse Recovery Charge | --- | 33 | --- | nC | $T_J$ = 25°C |
| | | --- | 34 | --- | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | --- | 1.8 | --- | A | $T_J$ = 25°C |

$V_R$ = 34V
$I_F$ = 90A
di/dt = 100A/µs ⑤

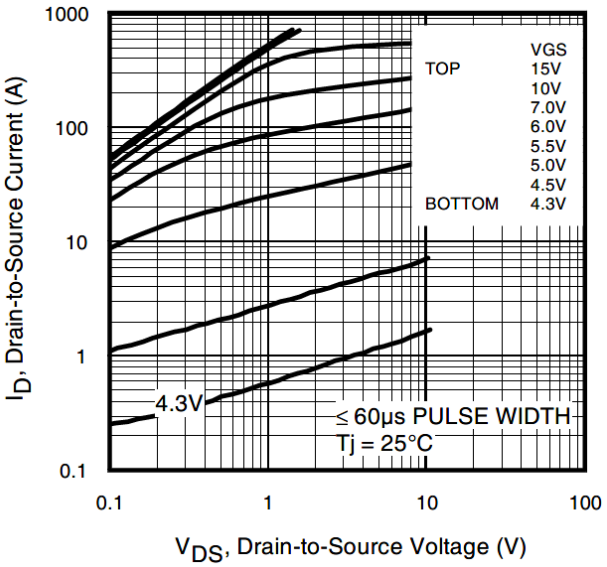



**Fig 3.** Typical Output Characteristics

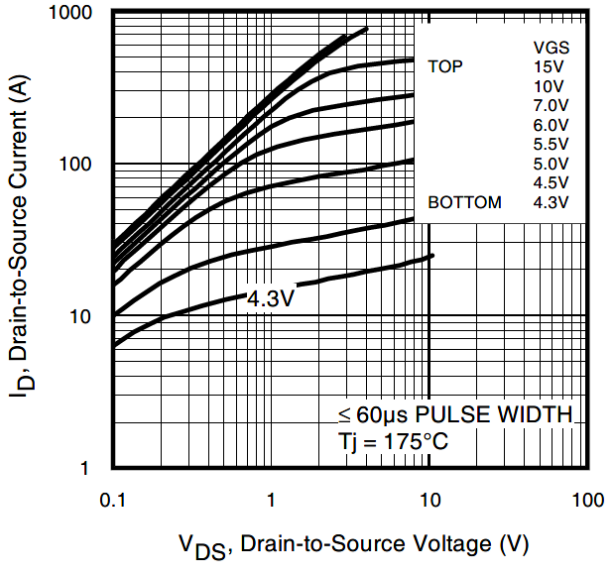



**Fig 4.** Typical Output Characteristics

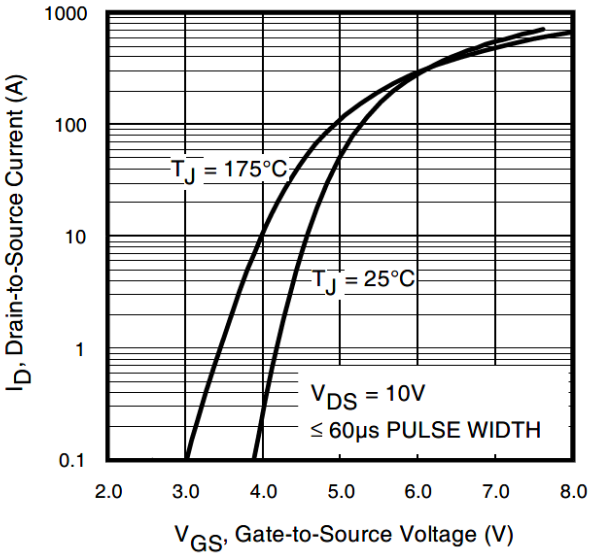



**Fig 5.** Typical Transfer Characteristics

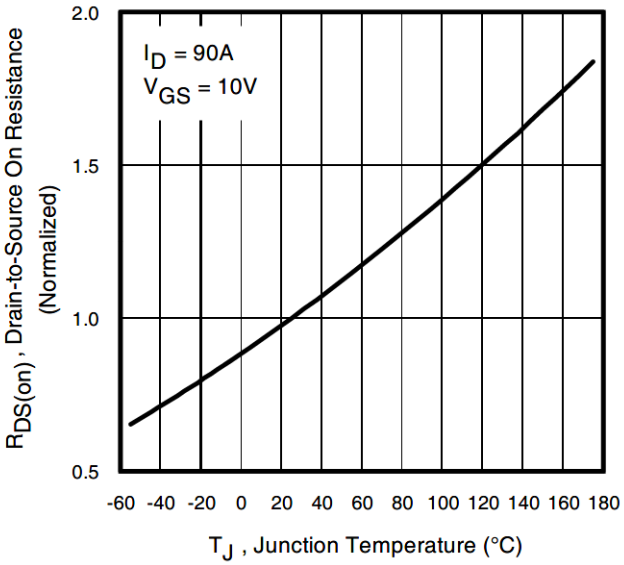



**Fig 6.** Normalized On-Resistance vs. Temperature

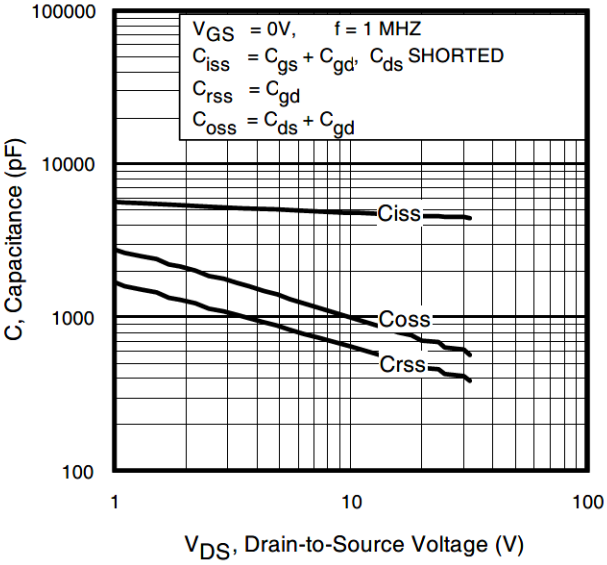



**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

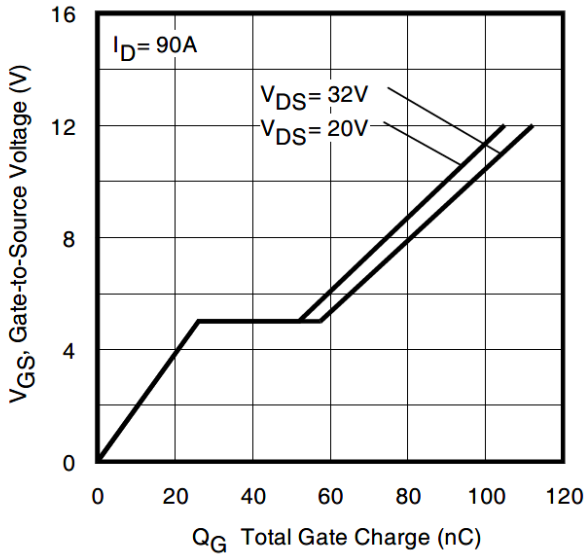



**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage

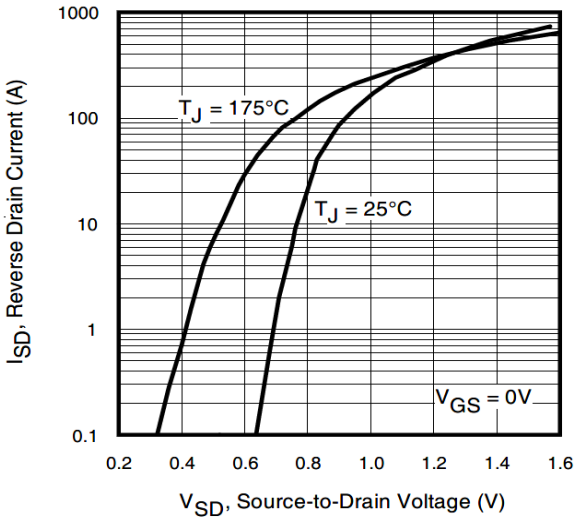



**Fig 9.** Typical Source-Drain Diode Forward Voltage

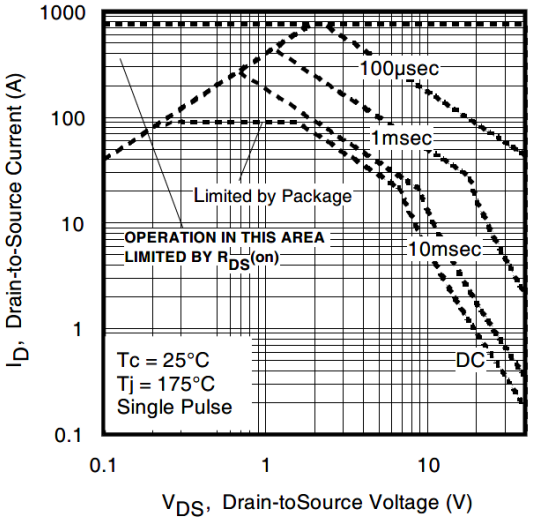



**Fig 10.** Maximum Safe Operating Area

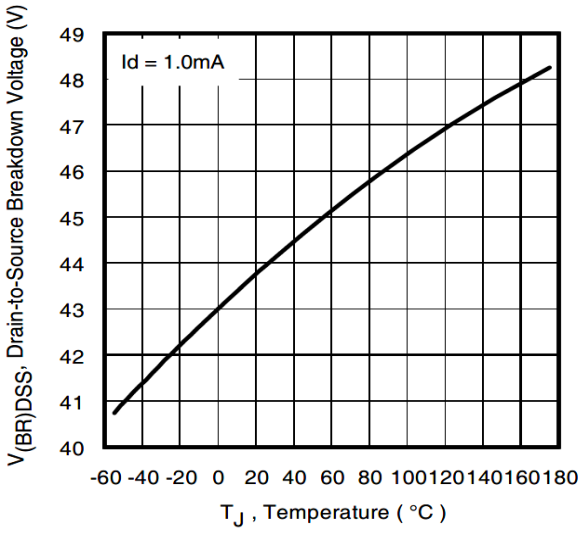



**Fig 11.** Drain-to-Source Breakdown Voltage

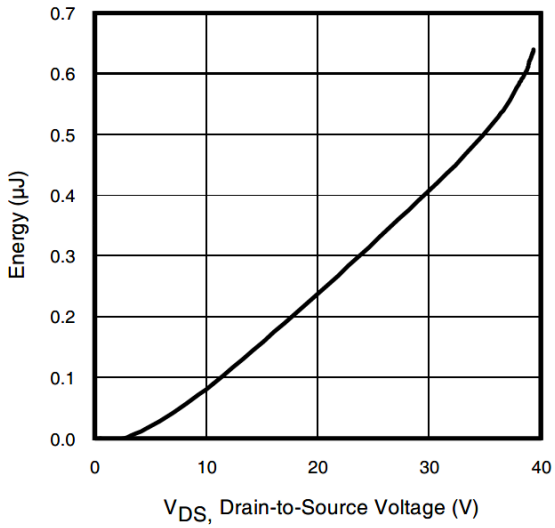



**Fig 12.** Typical $C_{oss}$ Stored Energy

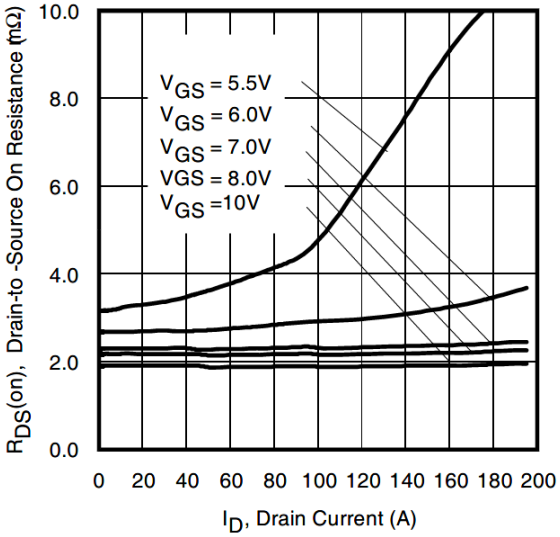



**Fig 13.** Typical On-Resistance vs. Drain Current

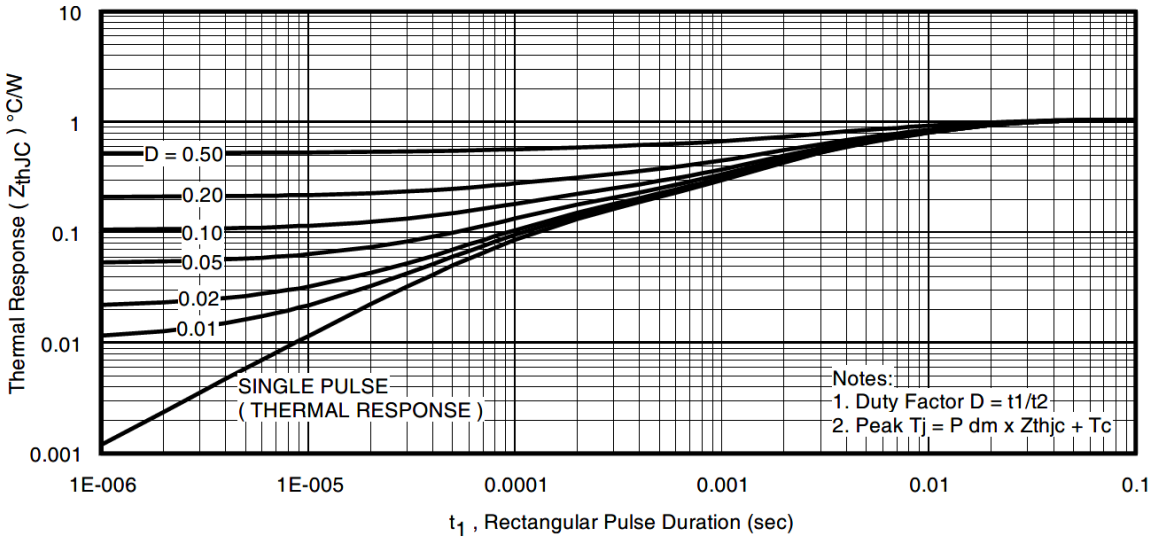



**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

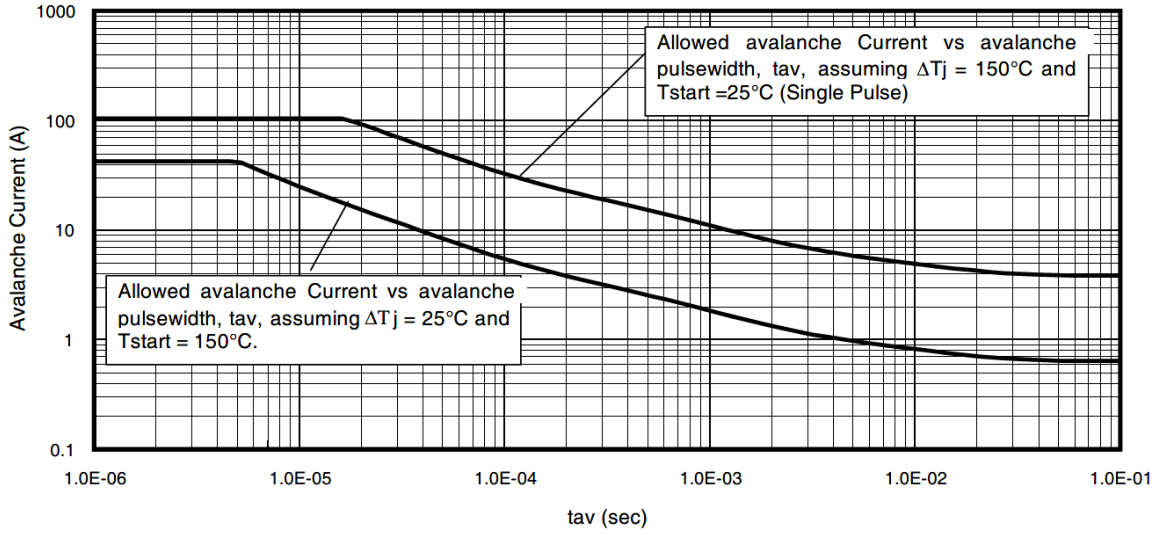



**Fig 15.** Avalanche Current vs. Pulse Width

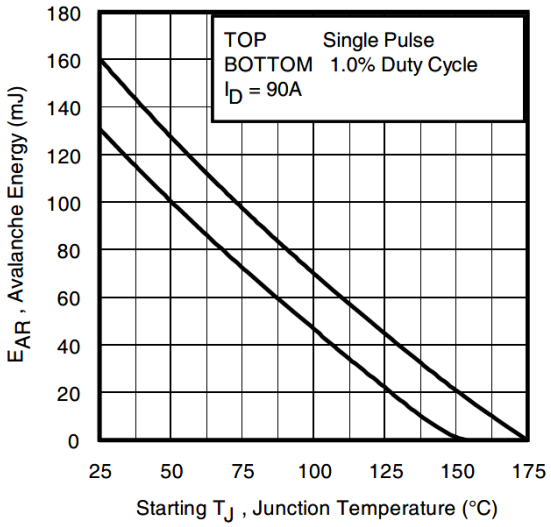



**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$P_{D\,(ave)} = 1/2\,(1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

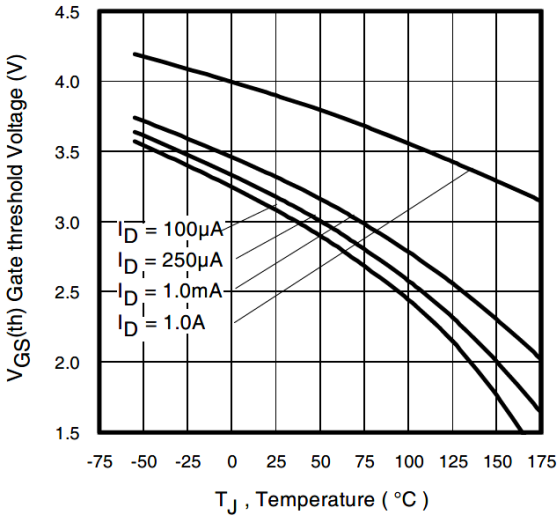



**Fig 17.** Threshold Voltage vs. Temperature

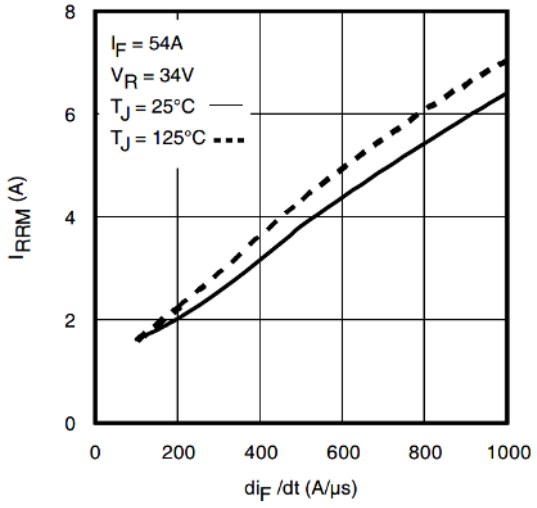



**Fig 18.** Typical Recovery Current vs. dif/dt

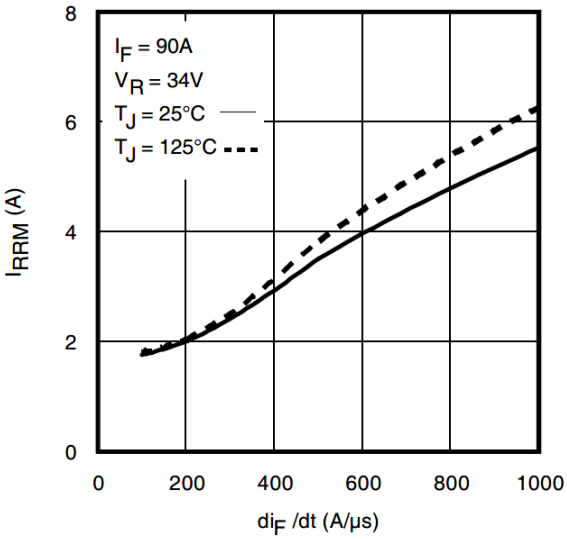



**Fig 19.** Typical Recovery Current vs. dif/dt

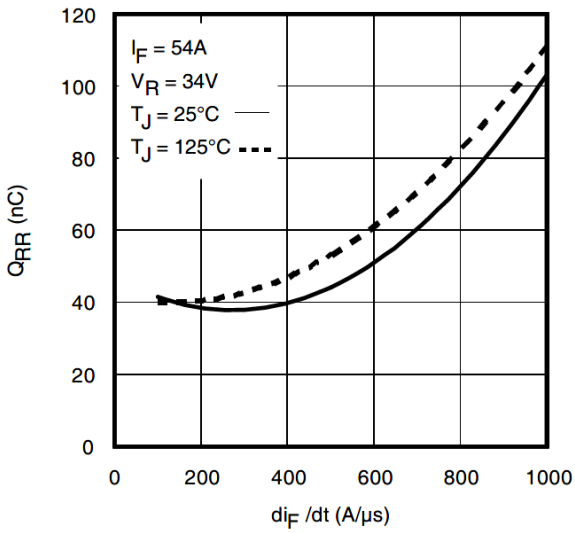



**Fig 20.** Typical Stored Charge vs. dif/dt

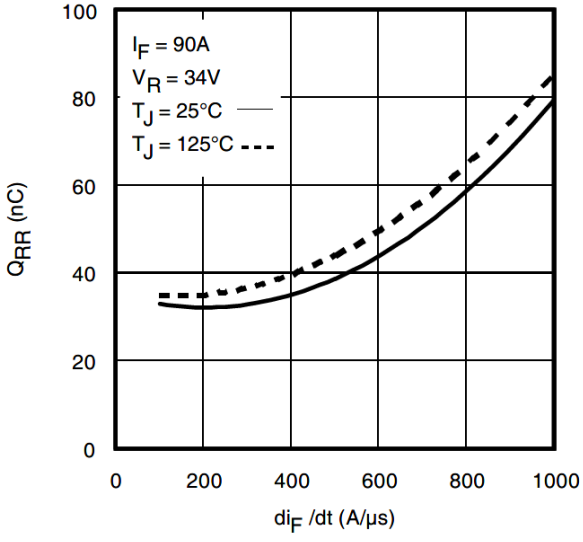



**Fig 21.** Typical Stored Charge vs. dif/dt

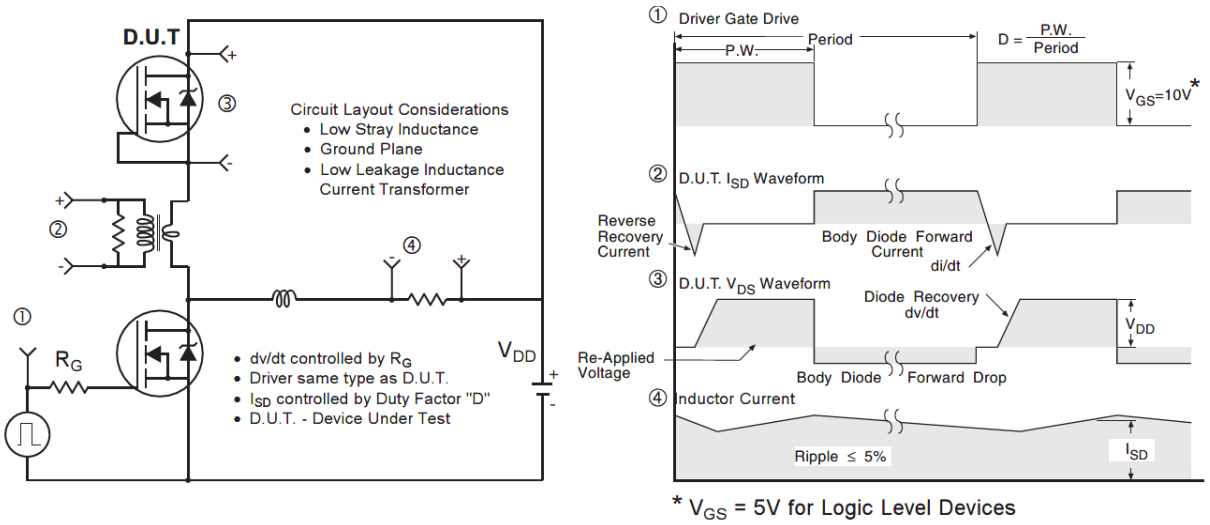



**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

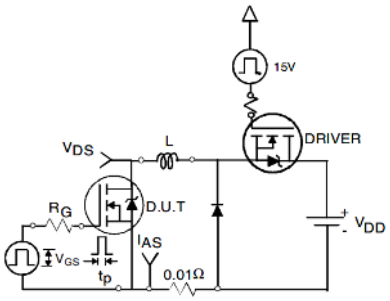



**Fig 23a.** Unclamped Inductive Test Circuit

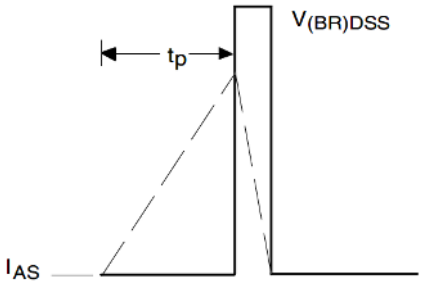



**Fig 23b.** Unclamped Inductive Waveforms

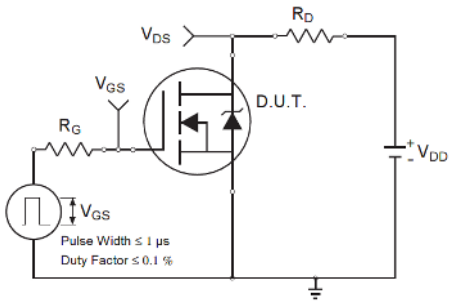



**Fig 24a.** Switching Time Test Circuit

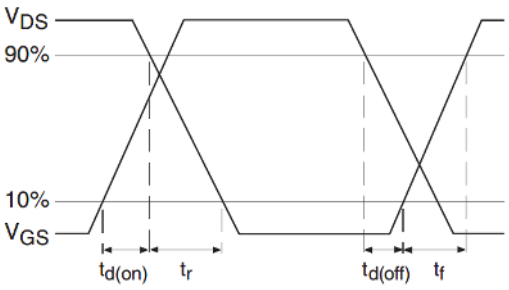



**Fig 24b.** Switching Time Waveforms

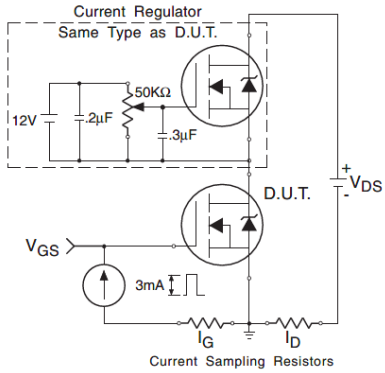



**Fig 25a.** Gate Charge Test Circuit

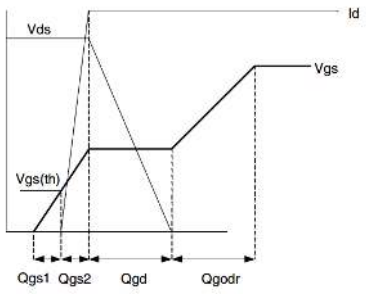
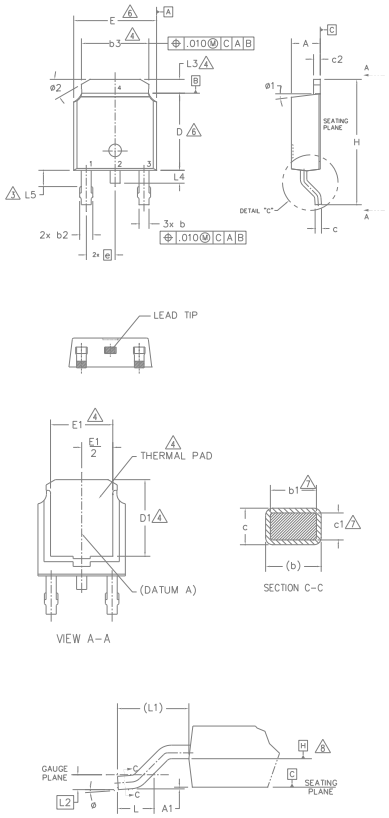



**Fig 25b.** Gate Charge Waveform

## D-Pak (TO-252AA) Package Outline Dimensions are shown in millimeters (inches)




NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– LEAD DIMENSION UNCONTROLLED IN L5.

4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | – | 0.13 | – | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.64 | 0.79 | .025 | .031 | 7 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | 7 |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | – | .205 | – | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | – | .170 | – | 4 |
| e | 2.29 BSC | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 BSC | | .108 REF. | | |
| L2 | 0.51 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | 4 |
| L4 | – | 1.02 | – | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| ø | 0° | 10° | 0° | 10° | |
| ø1 | 0° | 15° | 0° | 15° | |
| ø2 | 25° | 35° | 25° | 35° | |

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBT & CoPAK

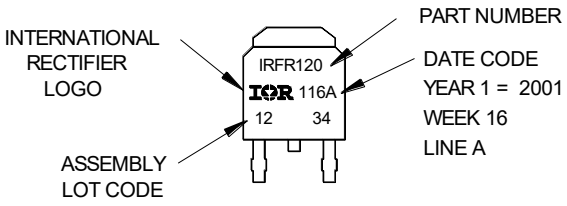
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

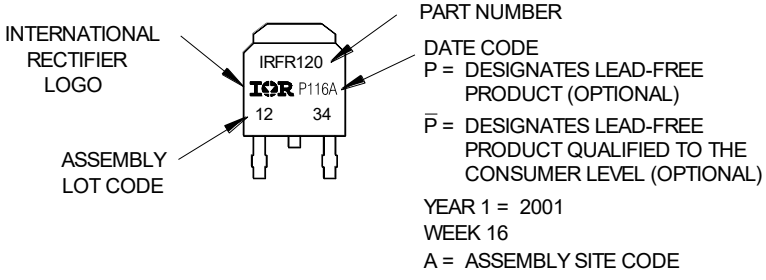
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

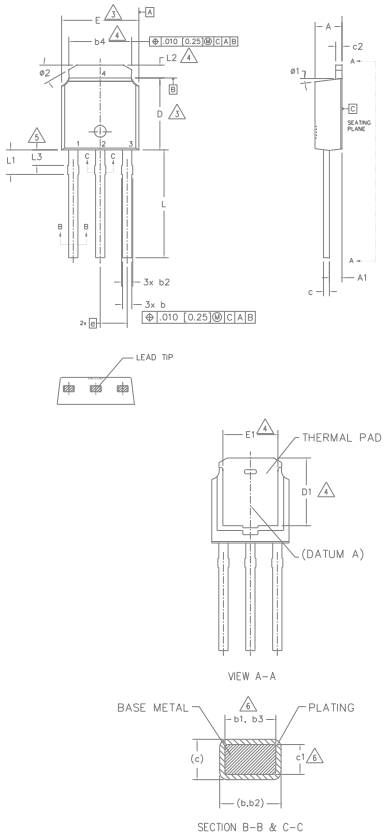
"$\bar{P}$" in assembly line position indicates "Lead-Free" qualification to the consumer-level




OR



## I-Pak (TO-251AA) Package Outline Dimensions are shown in millimeters (inches)




NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.

5. LEAD DIMENSION UNCONTROLLED IN L3.

6. DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.

7.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–251AA (Date 06/02).

8.– CONTROLLING DIMENSION : INCHES.

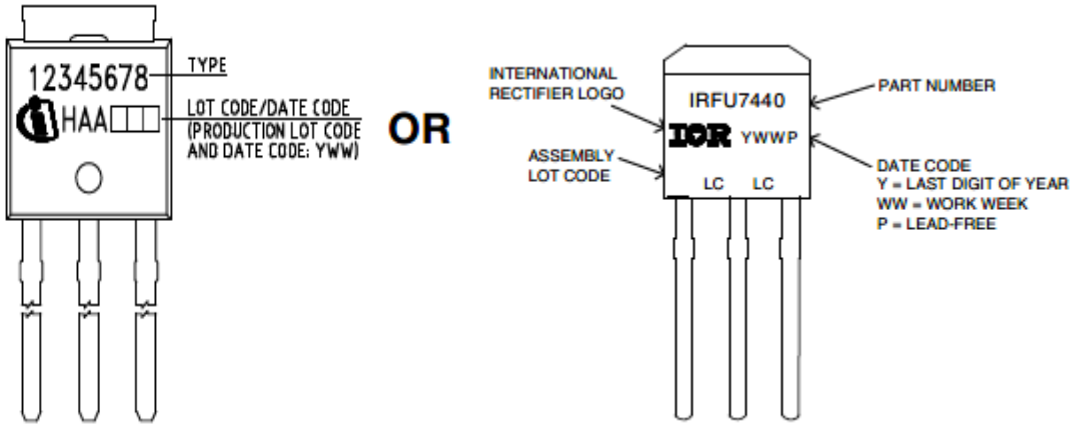
| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | 0.89 | 1.14 | .035 | .045 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.65 | 0.79 | .025 | .031 | 6 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 0.76 | 1.04 | .030 | .041 | 6 |
| b4 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | 6 |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | 3 |
| D1 | 5.21 | – | .205 | – | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 3 |
| E1 | 4.32 | – | .170 | – | 4 |
| e | 2.29 BSC | | .090 BSC | | |
| L | 8.89 | 9.65 | .350 | .380 | |
| L1 | 1.91 | 2.29 | .045 | .090 | |
| L2 | 0.89 | 1.27 | .035 | .050 | 4 |
| L3 | 0.89 | 1.52 | .035 | .060 | 5 |
| ø1 | 0° | 15° | 0° | 15° | |
| ø2 | 25° | 35° | 25° | 35° | |

LEAD ASSIGNMENTS

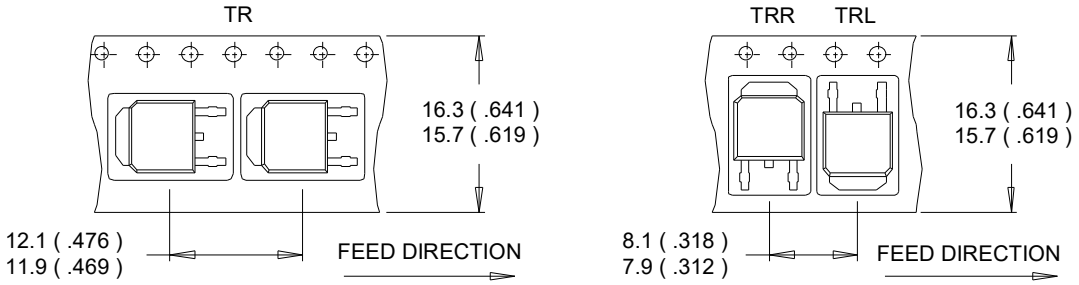
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

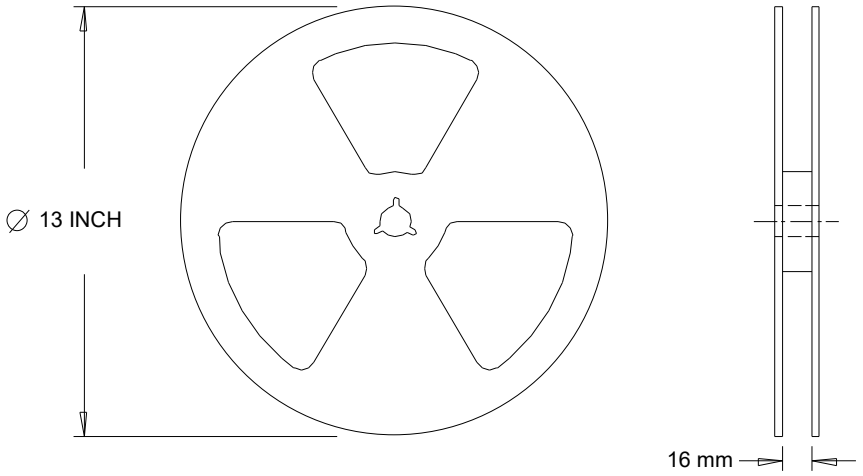
## I-Pak (TO-251AA) Part Marking Information



## D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. OUTLINE CONFORMS TO EIA-481.

## Qualification Information†

| | | |
|---|---|---|
| **Qualification Level** | Industrial<br>(per JEDEC JESD47F) †† | |
| **Moisture Sensitivity Level** | D-Pak | MSL1<br>(per JEDEC J-STD-020D)†† |
| | I-Pak | |
| **RoHS Compliant** | Yes | |

† Qualification standards can be found at Infineon web site: https://www.infineon.com/

†† Applicable version of JEDEC standard at the time of product release.

## Revision History

| Date | Rev. | Comments |
|---|---|---|
| 10/17/2012 | 2.1 | • Added I-Pak-All pages |
| 05/01/2014 | 2.2 | • Updated datasheet based on corporate template.<br>• Added "Stong Fet" on header on page7.<br>• Updated package outline and part marking on page 9 & 10. |
| 01/06/2015 | 2.3 | • Updated EAS (L =1mH) = 376mJ on page 2<br>• Updated note 10 “Limited by $T_{Jmax,}$ starting $T_J$ = 25°C, L = 1mH, $R_G$ = 50Ω, $I_{AS}$ = 27A, $V_{GS}$ =10V”. on page 2 |
| 06/05/2023 | 2.4 | • Updated datasheet based on IFX template.<br>• Removed “HEXFET® Power MOSFET /StrongIRFET™ ” and replace with “StrongIRFET™ power MOSFET “-page1<br>• Updated Part marking –page 10 |

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