19-1994; Rev 2; 10/01

MAXIM

35Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

General Description

The MAX4696/MAX4697/MAX4698 low on-resistance (R_{ON}), low-voltage analog switches operate from a single +2.0V to +5.5V supply. The MAX4696/MAX4697 are single-pole/single-throw (SPST) analog switches, and the MAX4698 is a single-pole/double-throw (SPDT) analog switch. The MAX4696 is a normally open (NO) switch, and the MAX4697 is a normally closed (NC) switch.

When powered from a 2.7V supply, these devices feature 35Ω (max) R_{ON}, with 2Ω (max) R_{ON} matching and 13Ω (max) flatness. The MAX4696/MAX4697/MAX4698 offer fast switching speeds (t_{ON} = 80ns max, t_{OFF} = 25ns max). The MAX4698 offers a break-before-make function.

The digital logic inputs are 1.8V logic compatible from a +2.7V to +3.3V supply and are TTL/CMOS compatible from a +4.5V to +5.5V supply. The MAX4696/MAX4697/MAX4698 are packaged in the chip-scale package (UCSP™), significantly reducing the required PC board area. The device occupies only a 1.50mm × 1.02mm area. The 3 × 2 array of solder bumps are spaced with a 0.5mm bump pitch.

Applications

MP3 Players
Battery-Operated Equipment
Relay Replacement
Audio and Video Signal Routing
Communications Circuits
PCMCIA Cards
Cellular Phones
Hard Drives
Modems

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.
UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- **6-Bump, 0.5mm Pitch, UCSP (Package pending full qualification—expected completion date 6/30/01. See *UCSP Reliability* section for more details.)**
- **R_{ON}**
  35Ω max (+3V Supply)
  20Ω max (+5V Supply)
- **2Ω max R_{ON} Match Between Channels**
- **13Ω max R_{ON} Flatness Over Signal Range**
- **Low Leakage Currents Over Temperature**
  1nA (max) at T_A = +25°C
- **Fast Switching: t_{ON} = 80ns, t_{OFF} = 25ns**
- **Guaranteed Break-Before-Make (MAX4698)**
- **+2.0V to +5.5V Single-Supply Operation**
- **Rail-to-Rail® Signal Handling**
- **Low Crosstalk: -75dB (100kHz)**
- **High Off-Isolation: -75dB (100kHz)**
- **1.8V CMOS Logic Compatible**
- **-3dB Bandwidth: >200MHz**

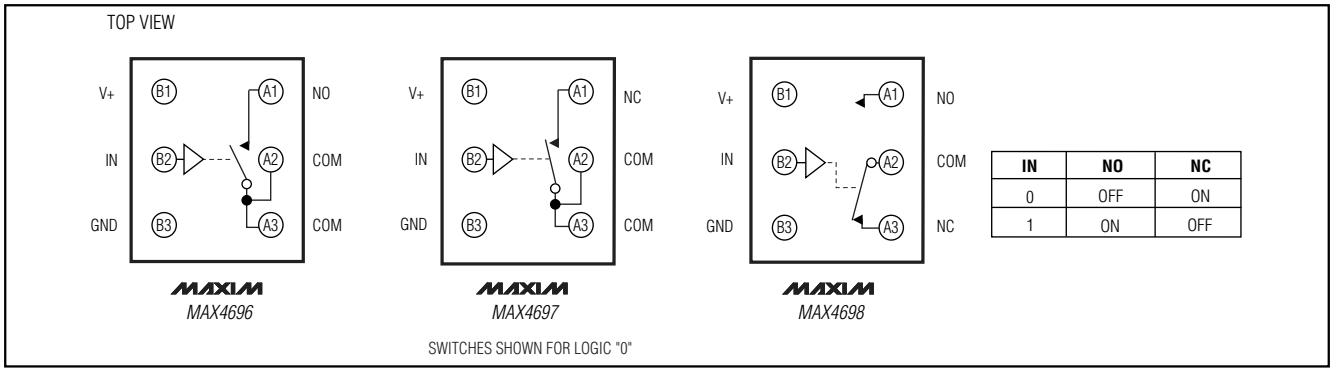
Ordering Information

PART	TEMP. RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4696EBT	-40°C to +85°C	6 UCSP*	AAL
MAX4697EBT	-40°C to +85°C	6 UCSP*	AAM
MAX4698EBT	-40°C to +85°C	6 UCSP*	AAN

* ***Note:*** *Requires special solder temperature profile described in the Absolute Maximum Ratings section.*

**UCSP reliabilty is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability section of this data sheet for more infromation.*

Pin Configurations/Functional Diagrams/Truth Table



IN	NO	NC
0	OFF	ON
1	ON	OFF

35Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND
V+, IN .....-0.3V to +6V
COM, NO, NC (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current COM, NO, NC .....±20mA
Peak Current COM, NO, NC
(pulsed at 1ms, 10% duty cycle) .....±40mA

Continuous Power Dissipation (T_A = +70°C)
3 × 2 UCSP (derate 10.1mW/°C at +70°C).....808mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering) (Note 2)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C

Note 1: Signals on NO, NC, and COM exceeding V+ are clamped by an internal diode. Limit forward-diode current to maximum current rating.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 3, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}		T_{MIN} to T_{MAX}	0		V+	V
On-Resistance	R_{ON}	V+ = +2.7V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1.5V	+25°C		30	35	Ω
			T_{MIN} to T_{MAX}			40	
On-Resistance Match Between Channels (MAX4698 only) (Note 5)	ΔR_{ON}	V+ = +2.7V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1.5V	+25°C		1	2	Ω
			T_{MIN} to T_{MAX}			3	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = +2.7V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1V, 1.5V, 2V	+25°C		10	13	Ω
			T_{MIN} to T_{MAX}			15	
NO, NC Off-Leakage Current (Note 4)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = +3.6V; V_{COM} = 0.3V, 3.3V; V_{NO} or V_{NC} = 3.3V, 0.3V	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM Off-Leakage Current (Note 4) (MAX4696, MAX4697 only)	$I_{COM\_(OFF)}$	V+ = +3.6V; V_{COM} = 0.3V, 3.3V; V_{NO} or V_{NC} = 0.3V, 3.3V	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM On-Leakage Current (Note 4)	$I_{COM\_(ON)}$	V+ = +3.6V; V_{COM} = 0.3V, 3.3V; V_{NO} or V_{NC} = 0.3V, 3.3V, or floating	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-2		2	
DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 4)	t_{ON}	V+ = +2.7V; V_{NO}, V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		50	80	ns
			T_{MIN} to T_{MAX}			110	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 3, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Turn-Off Time (Note 4)	t_{OFF}	V+ = +2.7V; V_{NO}, V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		20	25	ns
			T_{MIN} to T_{MAX}			40	
Break-Before-Make Time (MAX4698 only) (Note 4)	t_{BBM}	V+ = +3.3V; V_{NO}, V_{NC} = 1.5V, Figure 2	+25°C		15		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 3	+25°C		8		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out, Figure 4	+25°C		200		MHz
Off-Isolation (Note 7)	V_{ISO}	f = 100kHz, R_L = 50Ω, C_L = 5pF, Figure 4	+25°C		-75		dB
Crosstalk (MAX4698 only) (Note 8)	V_{CT}	f = 100kHz, R_L = 50Ω, C_L = 5pF, Figure 4	+25°C		-75		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, 2Vp-p, R_L = 600Ω	+25°C		0.014		%
NO, NC Off-Capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1MHz, Figure 5	+25°C		15		pF
COM Off-Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 5	+25°C		15		pF
Switch On-Capacitance	$C_{(ON)}$	f = 1MHz, Figure 6	+25°C		30		pF
DIGITAL I/O							
Input Logic High	V_{IH}		T_{MIN} to T_{MAX}	1.4			V
Input Logic Low	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	I_{IN}	V_{IN} = 0 or V+	T_{MIN} to T_{MAX}	-1		1	µA
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	2.0		5.5	V
Supply Current	I+	V+ = +3.3V, V_{IN} = 0 or V+	T_{MIN} to T_{MAX}			1	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V_{IH} = +2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +5V and T_A = +25°C.) (Notes 3, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}			0		V+	V
On-Resistance	R_{ON}	V+ = +4.5V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1V, 3.5V	+25°C		15	20	Ω
			T_{MIN} to T_{MAX}			25	
On-Resistance Match (MAX4698 only) (Note 5)	ΔR_{ON}	V+ = 4.5V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1V, 3.5V	+25°C		1	3	Ω
			T_{MIN} to T_{MAX}			4	

35Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V_{IH} = +2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +5V and T_A = 25°C.) (Notes 3,9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = +4.5V, I_{COM} = 1mA, V_{NO} or V_{NC} = 1V, 2.25V, 3.5V	+25°C		3	4	Ω
			T_{MIN} to T_{MAX}			5	
NO, NC Off-Leakage Current (Note 4)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = +5.5V; V_{COM} = 1V, 4.5V; V_{NO} or V_{NC} = 4.5V, 1V	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM Off-Leakage Current (MAX4696, MAX4697 only) (Note 4)	$I_{COM\_(OFF)}$	V+ = +5.5V; V_{COM} = 1V, 4.5V; V_{NO} or V_{NC} = 4.5V, 1V	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM On-Leakage Current (Note 4)	$I_{COM\_(ON)}$	V+ = +5.5V; V_{COM} = 1V, 4.5V; V_{NO} or V_{NC} = 1V, 4.5V, or floating	+25°C	-0.5	±0.01	0.5	nA
			T_{MIN} to T_{MAX}	-2		2	
Turn-On Time (Note 4)	t_{ON}	V+ = +5.5V, V_{NO}, V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		30	40	ns
			T_{MIN} to T_{MAX}			50	
Turn-Off Time (Note 4)	t_{OFF}	V+ = +5.5V, V_{NO}, V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		15	20	ns
			T_{MIN} to T_{MAX}			25	
Break-Before-Make Time (MAX4698 only) (Note 4)	t_{BBM}	V+ = +5.5V, V_{NO}, V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		9		ns
			T_{MIN} to T_{MAX}	2			
DIGITAL I/O							
Input Logic High	V_{IH}			2.4			V
Input Logic Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0 or V+		-1		1	µA
SUPPLY							
Power-Supply Range	V+			2.0		5.5	V
Supply Current	I+	V+ = +5.5V, V_{IN} = 0 or V+				1	µA

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: Guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$, between switches.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Off-Isolation = $20\log_{10}(V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

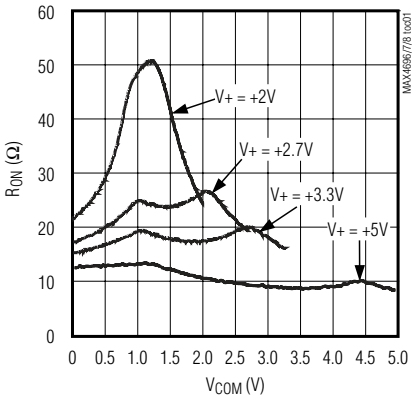
Note 8: Between switches.

Note 9: UCSP parts are 100% tested at +25°C only, and guaranteed by correlation at the full-rated temperature.

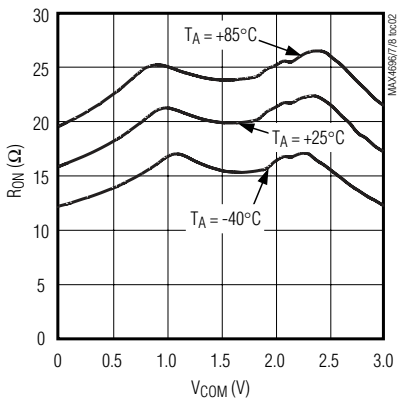
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

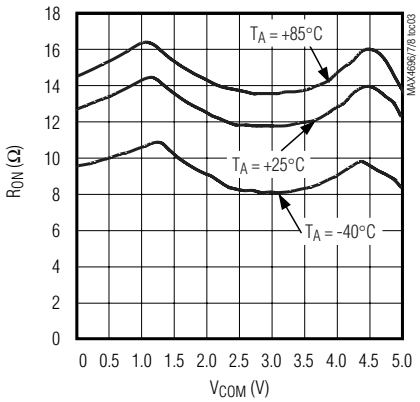
ON-RESISTANCE vs. V_{COM}



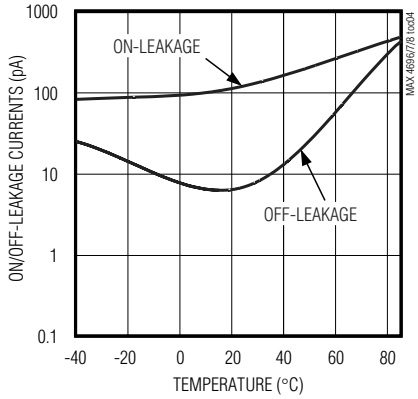
ON-RESISTANCE vs. V_{COM} (V+ = +3V)



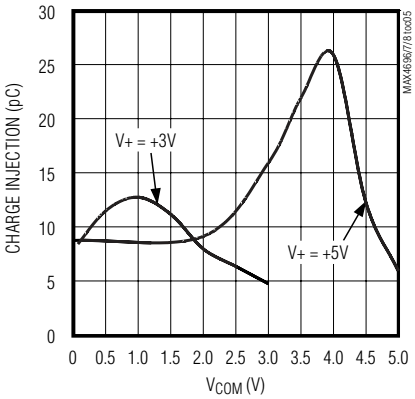
ON-RESISTANCE vs. V_{COM} (V+ = +5V)



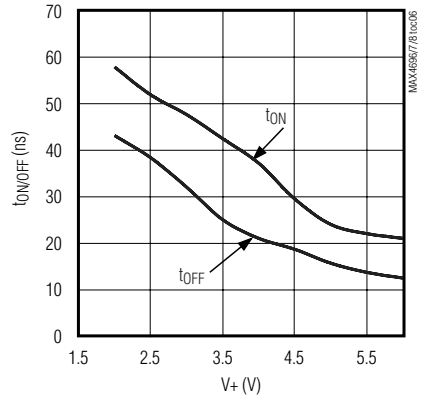
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



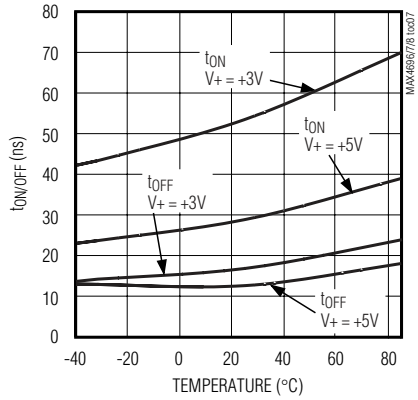
CHARGE INJECTION vs. V_{COM}



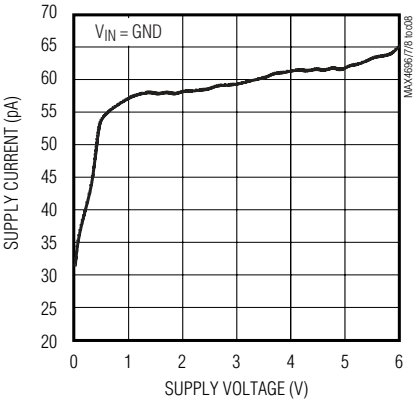
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



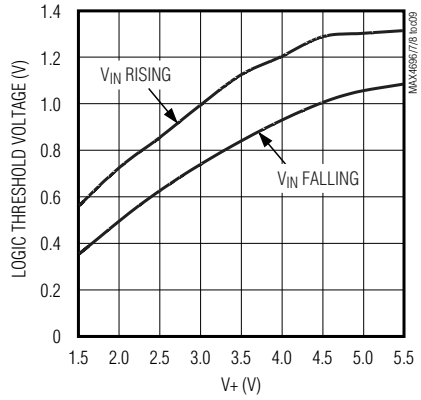
TURN-ON/OFF TIME vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE

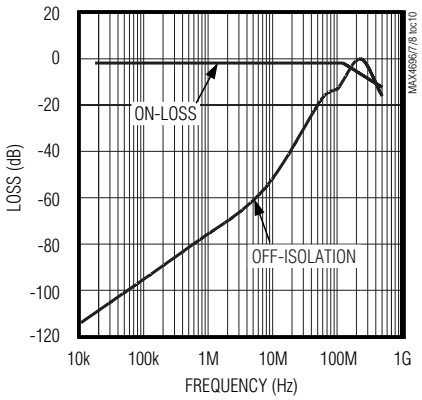


35Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

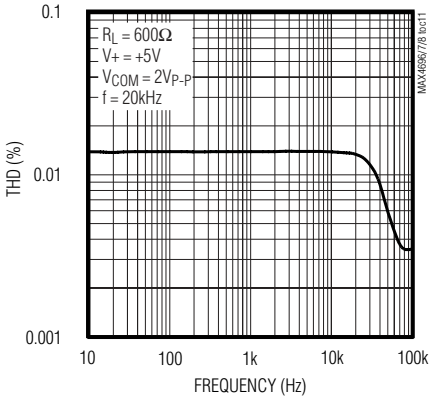
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin/Bump Description

PIN/BUMP			NAME	FUNCTION
MAX4696	MAX4697	MAX4698		
B1	B1	B1	V+	Positive Supply Voltage Input
B2	B2	B2	IN	Digital Control Input
B3	B3	B3	GND	Ground
—	A1	A3	NC	Analog Switch, Normally Closed Terminal
A2, A3	A2, A3	A2	COM	Analog Switch, Common Terminal
A1	—	A1	NO	Analog Switch, Normally Open Terminal

Applications Information

Logic Inputs

Where the MAX4696/MAX4697/MAX4698 have a +3.3V supply, IN may be driven low to GND and driven high to 5.5V. Driving IN rail-to-rail minimizes power consumption. Logic inputs accept up to +5.5V regardless of supply voltage.

Analog Signal Levels

Analog signals that range over the entire supply voltage (GND to V+) are passed with very little change in R_{ON} (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO, NC, and COM terminals are both inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

CAUTION: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small-signal diode (D1) as shown in Figure 6. Adding a protection diode reduces the analog range to a diode drop (about 0.7V) below V+ (for D1). R_{ON} increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V. Protection diode D1 also protects against some overvoltage situations. No

damage will result on the circuit in Figure 6 if the supply voltage is below the absolute maximum rating and if a fault voltage up to the absolute maximum rating is applied to an analog signal terminal.

UCSP Package Consideration

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note "Wafer-Level Ultra-Chip-Scale Packages".

UCSP Reliability

The chip-scale package (UCSP) represents a unique package that greatly reduces board space compared to other packages. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering a UCSP. Performance through Operating Life Test and Moisture Resistance is equal to conventional package technology as it is primarily determined by the wafer-fabrication process. However, this form factor may not perform equally to a packaged product through traditional mechanical reliability tests.

Mechanical stress performance is a greater consideration for a UCSP. UCSP solder joint contact integrity must be considered since the package is attached through direct solder contact to the user's PC board. Testing done to characterize the UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website, at www.maxim-ic.com.

Test Circuits/Timing Diagrams

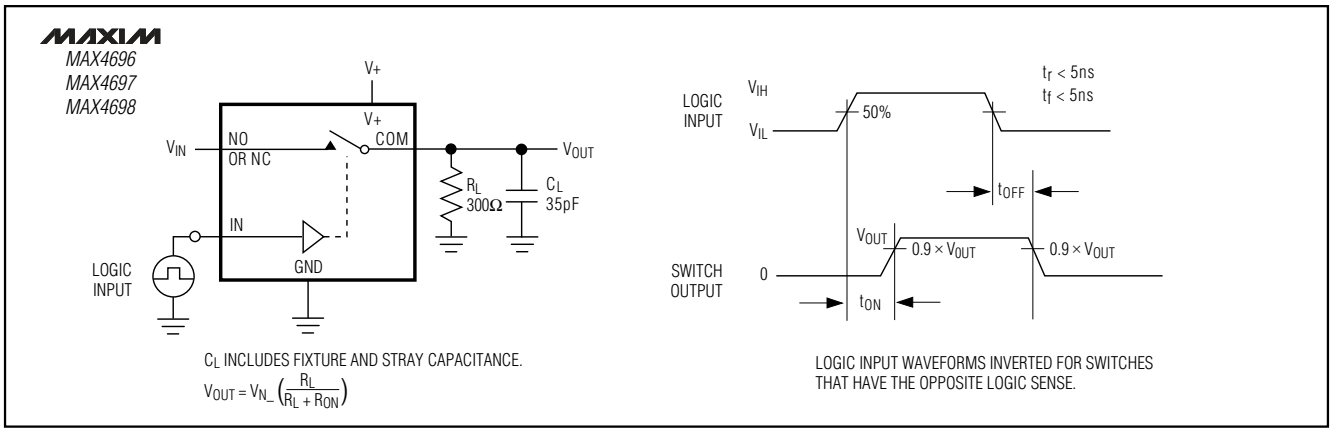


Figure 1. Switching Time

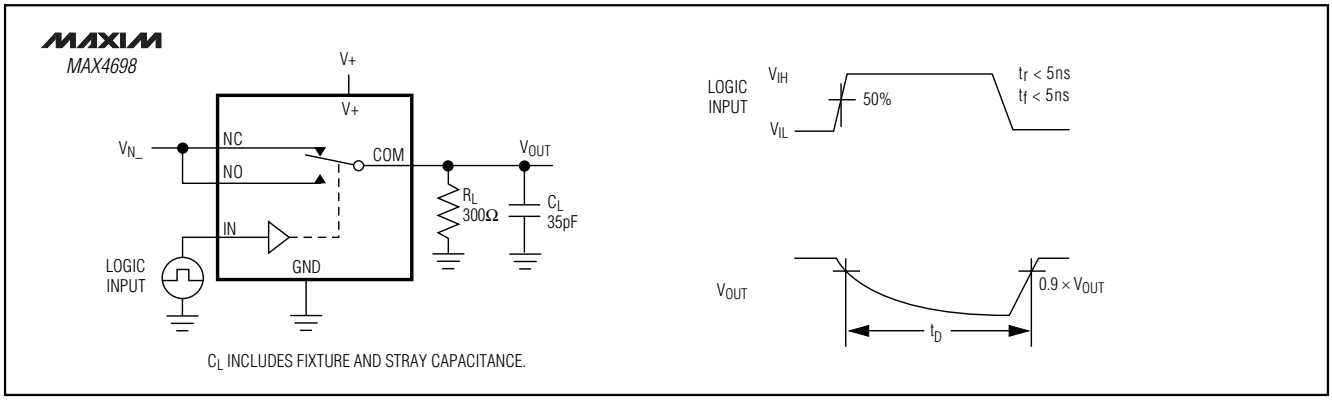


Figure 2. Break-Before-Make Interval (MAX4698 only)

35Ω, Low-Voltage, SPST/SPDT Analog Switches in UCSP Package

Test Circuits/Timing Diagrams (continued)

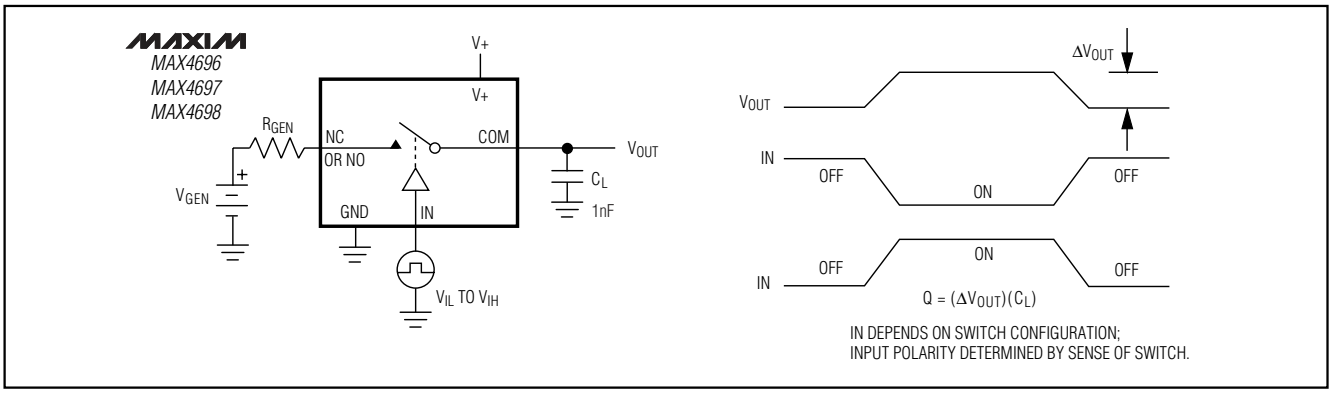


Figure 3. Charge Injection

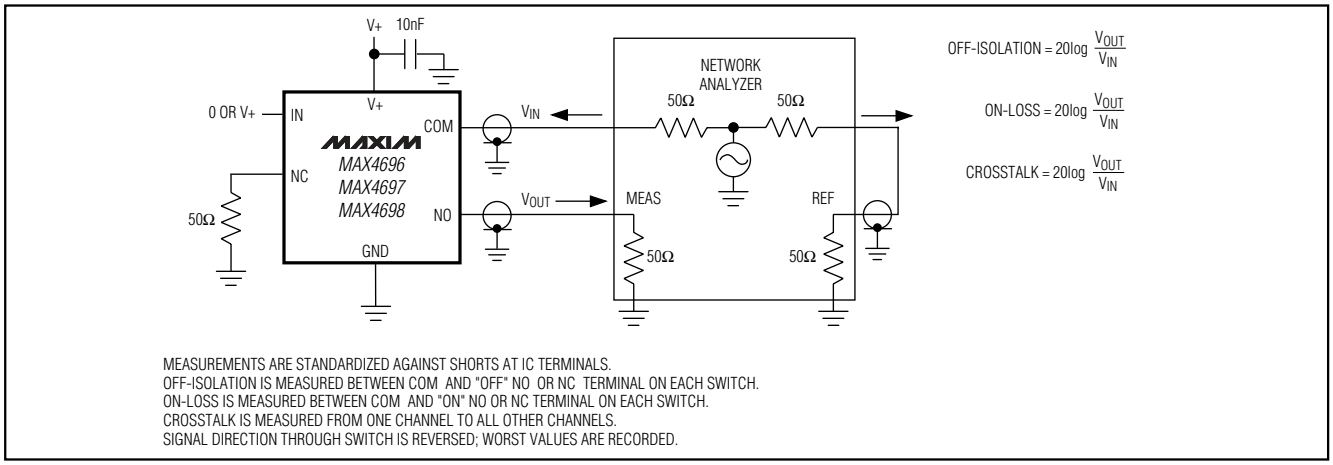


Figure 4. Off-Isolation/On-Channel Bandwidth, Crosstalk

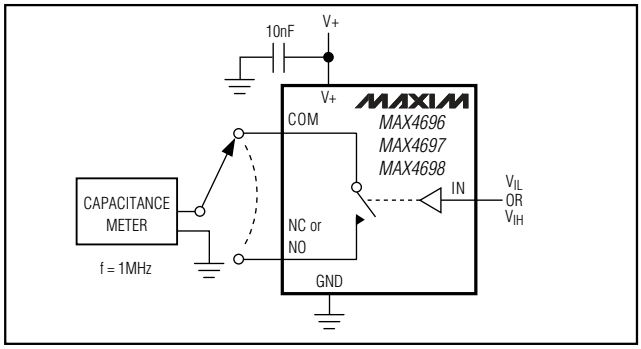


Figure 5. Channel Off/On-Capacitance

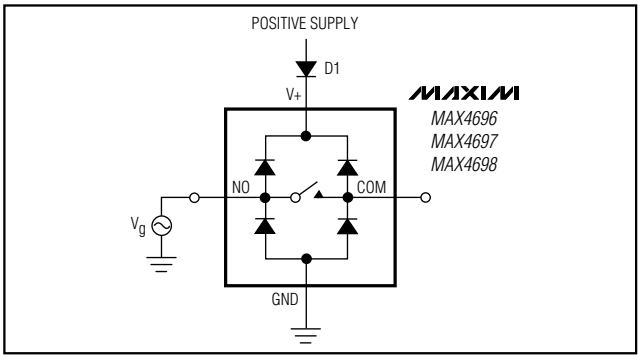


Figure 6. Overvoltage Protection Using External Blocking Diodes

Chip Information

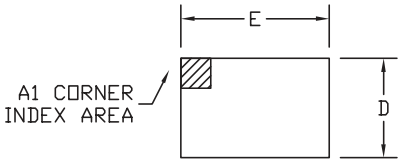
TRANSISTOR COUNT: 50

Package Information

6L, UCSP.EPS

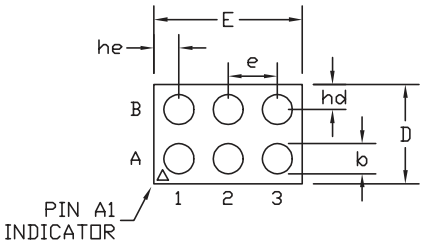
SYMBOL	DIMENSIONS
A	0.60±0.05
D	1.02±0.05
E	1.52±0.05
e	0.50 BASIC
b	ø 0.35 BASIC
A1	0.27±0.04
A2	0.33 Ref.
hd	0.26 Ref.
he	0.26 Ref.

SOLDER BALL DEPOPULATION	
PKG. CODE	DEPOPULATED BALL
B6-1	NONE
B6-2	B2

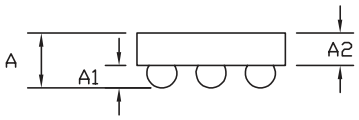


TOP VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MEETS JEDEC M0195.



BOTTOM VIEW



SIDE VIEW

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 3x2 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0097	C	1/1