74HC40105; 74HCT40105

4-bit x 16-word FIFO register

Rev. 4 — 29 January 2016 Product data sheet

1. General description

The 74HC40105; 74HCT40105 is a first-in/first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It can handle input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A logic 1 signifies that the data at that position is filled and a logic 0 denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the logic 0 state and sees a logic 1 in the preceding flip-flop, it generates a clock pulse. The clock pulse transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to logic 0. The first and last control flip-flops have buffered outputs. All empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end. As a result, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full. The status of the last flip-flop (data-out ready output - DOR) indicates whether the FIFO contains data. As the earliest data is removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Input levels:
  - For 74HC40105: CMOS level
  - For 74HCT40105: TTL level
- 3-state outputs
- Complies with JEDEC standard JESD7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC40105D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT40105D				
74HC40105DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT40105DB				
74HC40105PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

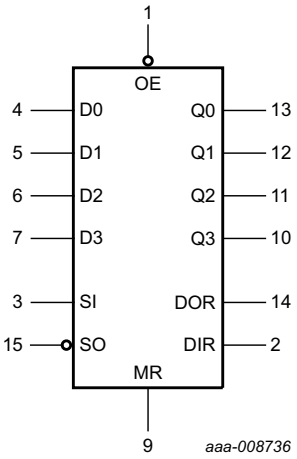


Fig 1. Logic symbol

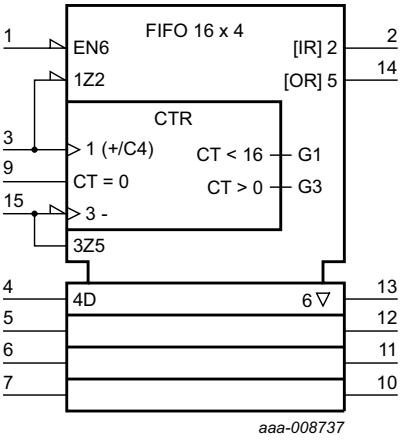


Fig 2. IEC logic symbol

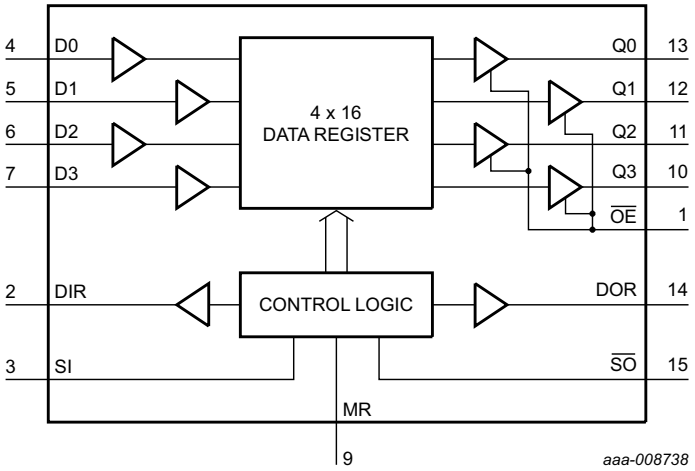
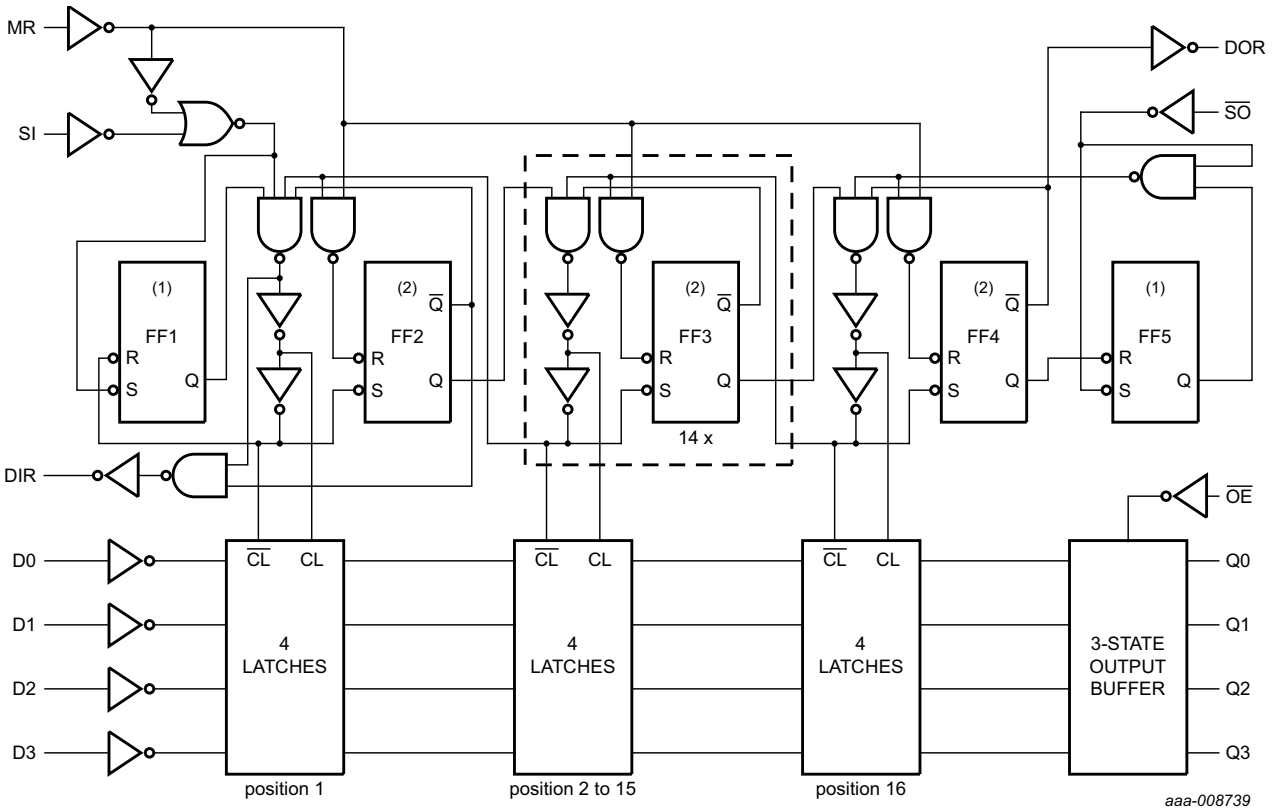


Fig 3. Functional diagram



LOW on $\overline{S}$ input of FF1 and FF5 sets Q output to HIGH independent of state on $\overline{R}$ input.
LOW on $\overline{R}$ input of FF2, FF3 and FF4 sets Q output to LOW independent of state on $\overline{S}$ input.

Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

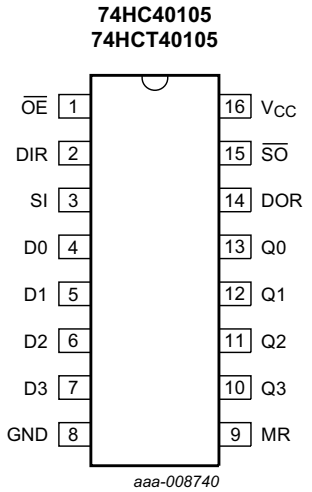


Fig 5. Pin configuration SO16

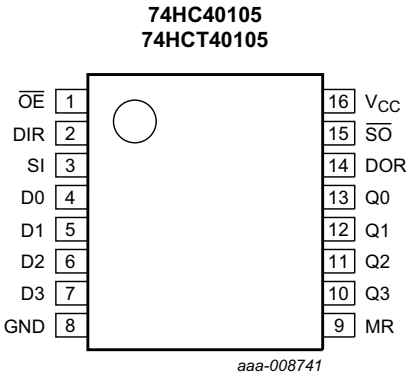


Fig 6. Pin configuration (T)SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (LOW-to-HIGH, edge triggered)
D0 to D3	4, 5, 6, 7	parallel data input
GND	8	ground (0 V)
MR	9	asynchronous master-reset input (active HIGH)
Q0 to Q3	13, 12, 11, 10	data output
DOR	14	data-out-ready output
$\overline{SO}$	15	shift-out input (HIGH-to-LOW, edge triggered)
V_{CC}	16	supply voltage

6. Functional description

6.1 Inputs and outputs

6.1.1 Data inputs (D0 to D3)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration. For example, it can be reduced to 3 x 16, down to 1 x 16, by tying unused data input pins to V_{CC} or GND.

6.1.2 Data outputs (Q0 to Q3)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration as described for data inputs. In a reduced format, the unused data outputs pins must be left open circuit.

6.1.3 Master-reset (MR)

When MR is HIGH, the control functions within the FIFO are cleared, and date content is declared invalid. The data-in ready (DIR) flag is set HIGH and the data-out-ready (DOR)

flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

6.1.4 Status flag outputs (DIR, DOR)

Two status flags, data-in-ready (DIR) and data-out-ready (DOR), indicate the status of the FIFO:

1. DIR = HIGH indicates that the input stage is empty and ready to accept valid data;
2. DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy);
3. DOR = HIGH assures valid data is present at the outputs Q0 to Q3 (does not indicate that new data is awaiting transfer into the output stage);
4. DOR = LOW indicates that the output stage is busy or there is no valid data.

6.1.5 Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. It also triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data is loaded at the falling edge of the MR signal.

6.1.6 Shift-out control ($\overline{SO}$)

A HIGH-to-LOW transition of $\overline{SO}$ causes the DOR flags to go LOW. A HIGH-to-LOW transition of $\overline{SO}$ causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

6.1.7 Output enable ($\overline{OE}$)

The outputs Q0 to Q3 are enabled when $\overline{OE}$ = LOW. When $\overline{OE}$ = HIGH the outputs are in the high impedance OFF-state.

6.2 Data input

Following power-up, the master-reset (MR) input is pulsed HIGH to clear the FIFO memory (see Figure 7). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D0 to D3 can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage. DIR going LOW provides a busy indication. The data remains at the first location in the FIFO until DIR is set to HIGH and data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Figure 8). To complete the shift-in process, the SI use must be made LOW. With the FIFO full, SI can be held HIGH until a shift-out ($\overline{SO}$) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This data remains at the first FIFO location until SI goes LOW (see Figure 9).

6.3 Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

6.4 Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q0 to Q3). The initial master-reset at power-on (MR = HIGH) sets DOR to LOW (see Figure 7). After MR = LOW, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH. As the DOR flag goes HIGH, data can be shifted-out using the $\overline{SO}$ = HIGH, data in the output stage is shifted out. DOR going LOW provides a busy indication. When $\overline{SO}$ is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted-out leaving the FIFO empty the DOR flag remains LOW (see Figure 11). With the FIFO empty, the last word that was shifted-out is latched at the output Q0 to Q3.

With the FIFO empty, the $\overline{SO}$ input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a shift-out of data occurring. The $\overline{SO}$ control must be made LOW before additional data can be shifted-out (see Figure 14).

6.5 High-speed burst mode

Assuming the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the status flags determine the shift-in/shift-out rates. However, without the status flags, a high-speed burst can be implemented. In this mode, pulse widths determine the burst-in/ burst-out rates of the shift-in/shift-out inputs. Burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figure 12 and Figure 13).

6.6 Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Figure 19). The basic operation and timing are identical to a single FIFO, except for an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figure 9 and Figure 20).

Due to the part-to-part spread of the ripple through time, the SI signals of FIFOA and FIFOB do not always coincide. As a result, the AND-gate does not produce a composite flag signal. The solution is given in Figure 20. The “40105” is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, the FIFOs perform all necessary communications and timing. The minimum flag pulse widths and the flag delays determine the intercommunication speed. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 32-words x 4-bits (see Figure 21).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		-	±25	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			−50	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	SO16 package	[2]	-	500	mW
		(T)SSOP16 package	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

[3] For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC40105			74HCT40105			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC40105										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA

Table 5. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT40105										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = -20$ µA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4$ mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = 20$ µA	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4$ mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8	-	80	-	160	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; Dn inputs	-	30	108	-	135	-	147	µA
		per input pin; $\overline{OE}$ input	-	75	270	-	338	-	368	µA
		per input pin; SI input	-	40	144	-	180	-	196	µA
		per input pin; MR input	-	150	540	-	675	-	735	µA
		per input pin; $\overline{SO}$ input	-	40	144	-	180	-	196	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 6. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 18.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC40105										
t_{pd}	propagation delay	MR to DIR or DOR; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	52	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	19	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	30	-	37	-	45	ns
		$\overline{SO}$ to Qn; see Figure 10 [1]								
		V_{CC} = 2.0 V	-	116	400	-	500	-	600	ns
		V_{CC} = 4.5 V	-	42	80	-	100	-	120	ns
		V_{CC} = 5 V; C_L = 15 pF	-	37	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	34	68	-	85	-	102	ns
t_{PHL}	HIGH to LOW propagation delay	SI to DIR; see Figure 8 [1]								
		V_{CC} = 2.0 V	-	52	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	19	42	-	53	-	63	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	36	-	45	-	54	ns
		$\overline{SO}$ to DOR; see Figure 11 [1]								
		V_{CC} = 2.0 V	-	55	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	20	42	-	53	-	63	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	36	-	45	-	54	ns
t_{PLH}	LOW to HIGH propagation delay	SI to DOR; see Figure 14 [1][5]								
		V_{CC} = 2.0 V	-	564	2000	-	2500	-	3000	ns
		V_{CC} = 4.5 V	-	205	400	-	500	-	600	ns
		V_{CC} = 6.0 V	-	165	340	-	425	-	510	ns
		$\overline{SO}$ to DIR; see Figure 9 [1][6]								
		V_{CC} = 2.0 V	-	701	2500	-	3125	-	3750	ns
		V_{CC} = 4.5 V	-	255	500	-	625	-	750	ns
		V_{CC} = 6.0 V	-	204	425	-	532	-	638	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 16 [2]								
		V_{CC} = 2.0 V	-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	12	26	-	33	-	38	ns

Table 6. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 18.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 16 [3]								
		V_{CC} = 2.0 V	-	41	140	-	175	-	210	ns
		V_{CC} = 4.5 V	-	15	28	-	35	-	42	ns
		V_{CC} = 6.0 V	-	12	24	-	30	-	36	ns
t_t	transition time	Qn; see Figure 10 [4]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	SI HIGH or LOW; see Figure 8								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$\overline{SO}$ HIGH or LOW; see Figure 11								
		V_{CC} = 2.0 V	120	39	-	150	-	180	-	ns
		V_{CC} = 4.5 V	24	14	-	30	-	36	-	ns
		V_{CC} = 6.0 V	20	11	-	26	-	31	-	ns
		DIR HIGH; see Figure 9								
		V_{CC} = 2.0 V	12	58	180	10	225	10	270	ns
		V_{CC} = 4.5 V	6	21	36	5	45	5	54	ns
		V_{CC} = 6.0 V	5	17	31	4	38	4	46	ns
		DOR LOW; see Figure 14								
		V_{CC} = 2.0 V	12	55	170	10	215	10	255	ns
		V_{CC} = 4.5 V	6	20	34	5	43	5	51	ns
		V_{CC} = 6.0 V	5	16	29	4	37	4	43	ns
		MR HIGH; see Figure 7								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	MR to SI; see Figure 15								
		V_{CC} = 2.0 V	50	14	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	5	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	4	-	11	-	13	-	ns
t_{su}	set-up time	Dn to SI; see Figure 17								
		V_{CC} = 2.0 V	–5	–39	-	–5	-	–5	-	ns
		V_{CC} = 4.5 V	–5	–14	-	–5	-	–5	-	ns
		V_{CC} = 6.0 V	–5	–11	-	–5	-	–5	-	ns

Table 6. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 18.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	Dn to SI; see Figure 17								
		V_{CC} = 2.0 V	125	44	-	155	-	190	-	ns
		V_{CC} = 4.5 V	25	16	-	31	-	38	-	ns
		V_{CC} = 6.0 V	21	13	-	26	-	32	-	ns
f_{max}	maximum frequency	SI, $\overline{SO}$ using flags or burst mode; see Figure 8 and Figure 11; see Figure 12 and Figure 13								
		V_{CC} = 2.0 V	3.6	10	-	2.8	-	2.4	-	MHz
		V_{CC} = 4.5 V	18	30	-	14	-	12	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	33	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	21	36	-	16	-	14	-	MHz
		SI, $\overline{SO}$ cascaded; see Figure 8 and Figure 11								
		V_{CC} = 2.0 V	3.6	10	-	2.8	-	2.4	-	MHz
		V_{CC} = 4.5 V	18	30	-	14	-	12	-	MHz
		V_{CC} = 6.0 V	21	36	-	16	-	14	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [7]	-	134	-	-	-	-	-	pF

Table 6. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 18.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT40105										
t_{pd}	propagation delay	MR to DIR or DOR; see Figure 7 [1]								
		V_{CC} = 4.5 V	-	18	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		$\overline{SO}$ to Qn; see Figure 10 [1]								
		V_{CC} = 4.5 V	-	40	80	-	100	-	120	ns
		V_{CC} = 5 V; C_L = 15 pF	-	35	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	SI to DIR; see Figure 8 [1]								
		V_{CC} = 4.5 V	-	21	42	-	53	-	63	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	-	-	ns
		$\overline{SO}$ to DOR; see Figure 11 [1]								
		V_{CC} = 4.5 V	-	20	42	-	53	-	63	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	-	-	ns
t_{PLH}	LOW to HIGH propagation delay	SI to DOR; see Figure 14 [1][5]								
		V_{CC} = 4.5 V	-	188	400	-	500	-	600	ns
		$\overline{SO}$ to DIR; see Figure 9 [1][6]								
		V_{CC} = 4.5 V	-	244	500	-	625	-	750	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 16 [2]								
		V_{CC} = 4.5 V	-	18	35	-	44	-	53	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 16 [3]								
		V_{CC} = 4.5 V	-	15	30	-	38	-	45	ns
t_t	transition time	Qn; see Figure 10 [4]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	SI HIGH or LOW; see Figure 8								
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		$\overline{SO}$ HIGH or LOW; see Figure 11								
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		DIR HIGH; see Figure 9								
		V_{CC} = 4.5 V	6	20	34	5	43	5	51	ns
		DOR LOW; see Figure 14								
		V_{CC} = 4.5 V	6	19	34	5	43	5	51	ns
		MR HIGH; see Figure 7								
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
t_{rec}	recovery time	MR to SI; see Figure 15								
		V_{CC} = 4.5 V	15	7	-	19	-	22	-	ns

Table 6. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 18.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to SI; see Figure 17								
		V_{CC} = 4.5 V	–5	–14	-	–4	-	–4	-	ns
t_h	hold time	Dn to SI; see Figure 17								
		V_{CC} = 4.5 V	27	16	-	34	-	41	-	ns
f_{max}	maximum frequency	SI, $\overline{SO}$ using flags or burst mode; see Figure 8 and Figure 11; see Figure 12 and Figure 13								
		V_{CC} = 4.5 V	-	28	-	12	-	10	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	31	-	-	-	-	-	MHz
		SI, $\overline{SO}$ cascaded; see Figure 8 and Figure 11								
		V_{CC} = 4.5 V	-	28	-	12	-	10	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V [7]	-	145	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

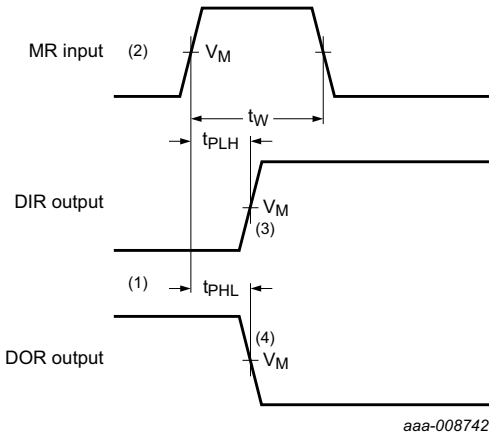
[5] This is the ripple through delay.

[6] This is the bubble-up delay.

[7] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

11.1 Master reset applied with FIFO full



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) DIR LOW; output ready HIGH; assume that FIFO is full

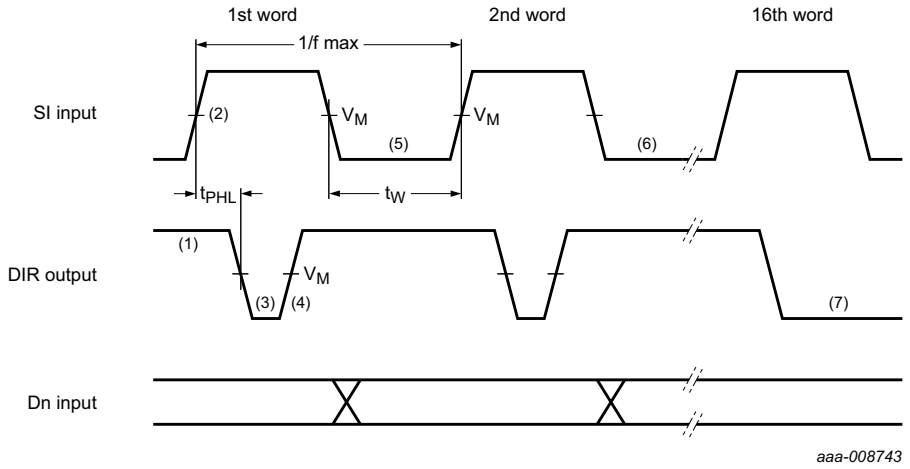
(2) MR pulse HIGH; clears FIFO

(3) DIR goes HIGH; flag indicates input prepared for valid data

(4) DOR goes LOW; flag indicates FIFO empty

Fig 7. Propagation delay MR input to DIR output, DOR output and Qn outputs and the MR pulse width.

11.2 Shifting in sequence FIFO empty to FIFO full



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) DIR initially HIGH; FIFO is prepared for valid data

(2) SI set HIGH; data loaded into input stage

(3) DIR drops LOW; input stage “busy”

(4) DIR goes HIGH; status flag indicates FIFO prepared for additional data

(5) SI set LOW; data from first location “ripple through”

(6) To load 2nd word through to 16th word into FIFO, repeat the process.

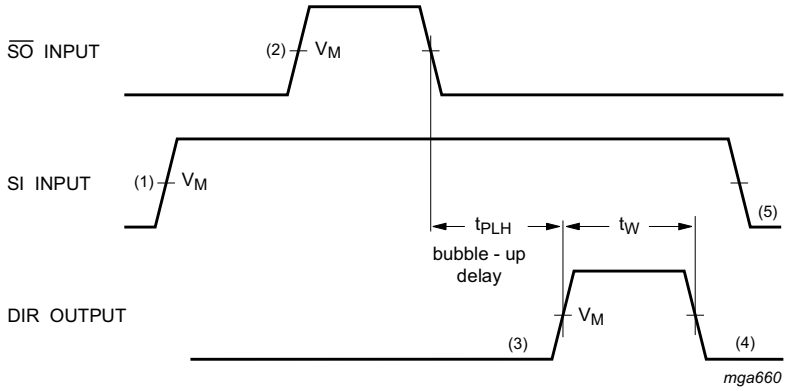
(7) DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

Fig 8. Propagation delay SI input to DIR output, the SI pulse width and the SI maximum frequency

Table 7. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC40105	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT40105	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

11.3 With FIFO full; SI held HIGH in anticipation of empty location



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) FIFO is initially full, shift-in is held HIGH

(2) $\overline{SO}$ pulse; data in output stage is unloaded, “bubble-up” process of empty location begins

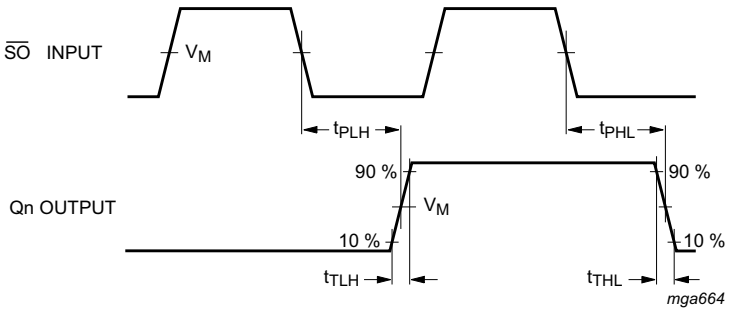
(3) DIR HIGH; when empty location reaches input stage, flag indicates that FIFO is prepared for data input

(4) DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again

(5) SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full

Fig 9. Bubble-up delay $\overline{SO}$ input to DIR output, the DIR pulse width.

11.4 $\overline{SO}$ input to Qn outputs propagation delay

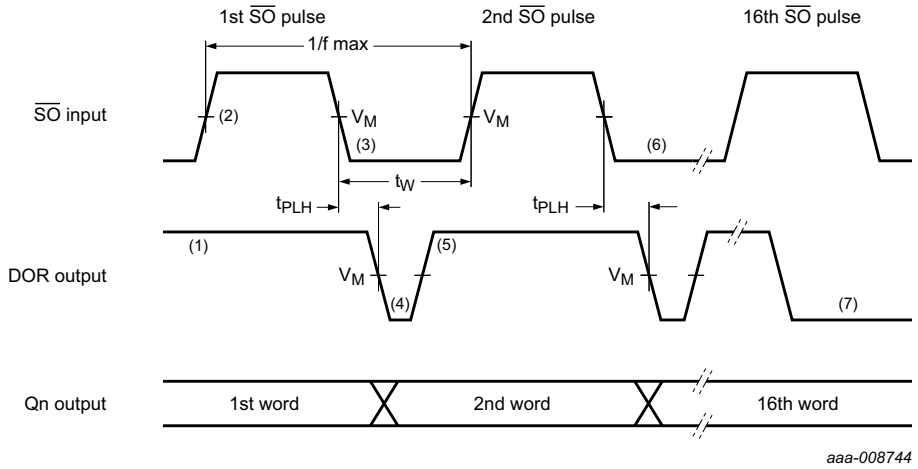


Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Propagation delay $\overline{SO}$ input to Qn outputs and the output transition time

11.5 Shifting out sequence; FIFO full to FIFO empty



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) DOR HIGH; no data transfer in progress, valid data is present at the output stage

(2) $\overline{SO}$ set HIGH; result in DOR going LOW

(3) $\overline{SO}$ set LOW; data in the input stage is unloaded, and new data replaces it as empty location “bubbles-up” to input stage

(4) DOR drops LOW; output stage “busy”

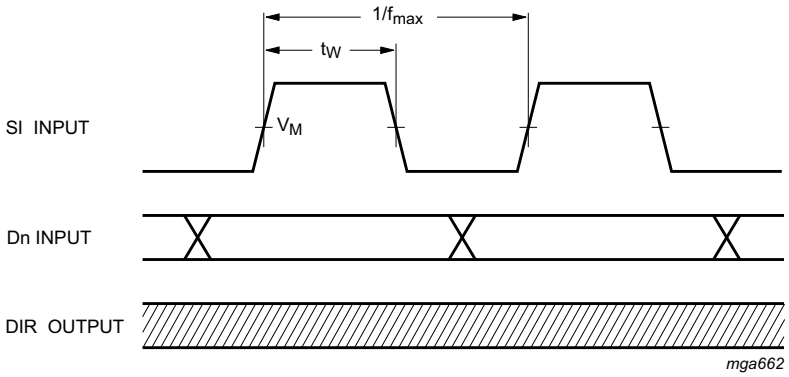
(5) DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay

(6) To unload the 3rd through the 16th word from FIFO, repeat the process

(7) DOR remains LOW; FIFO is empty

Fig 11. Propagation delay $\overline{SO}$ input to DOR output, the $\overline{SO}$ pulse width and the $\overline{SO}$ maximum frequency.

11.6 Shift-in operation; high-speed burst mode



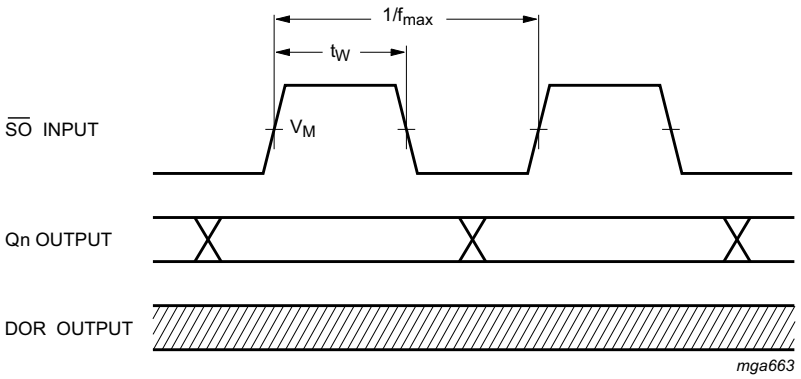
Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

In the high-speed mode, the minimum shift-in HIGH and shift-in LOW specifications determines the burst-in rate. The DIR status flag is a “don’t care” condition, and a shift-in pulse can be applied regardless of the flag. An SI pulse which would overflow the storage capacity of the FIFO is ignored.

Fig 12. The SI pulse width and the SI maximum frequency, in high-speed shift-in burst mode

11.7 Shift-out operation; high-speed burst mode



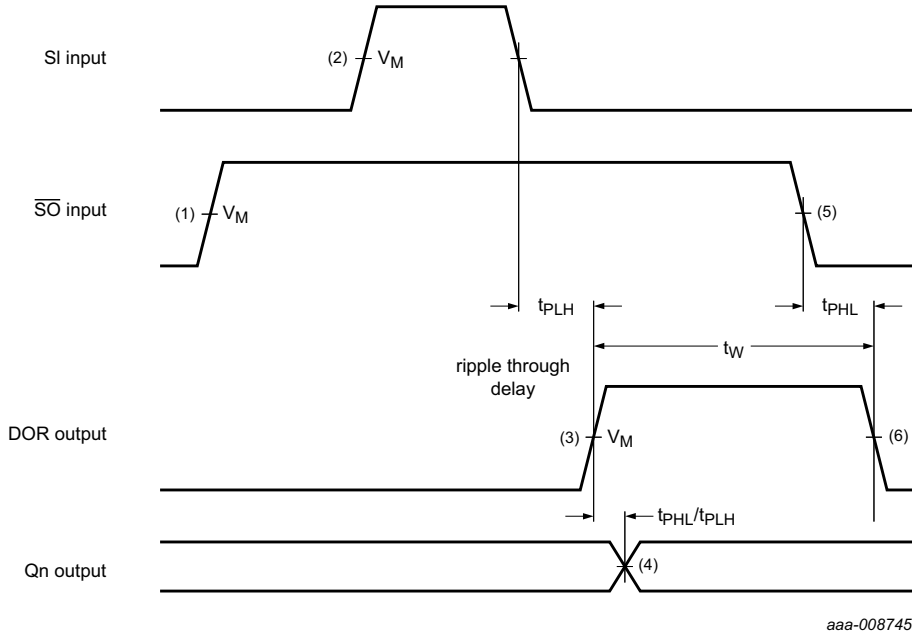
Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

In the high-speed mode, the minimum shift-out HIGH and shift-out LOW specifications determine the burst-out rate. The DOR flag is a “don’t care” condition, and an $\overline{SO}$ pulse can be applied without regard to the flag.

Fig 13. The $\overline{SO}$ pulse width and the $\overline{SO}$ maximum frequency, in high-speed shift-out burst mode

11.8 With FIFO empty; $\overline{SO}$ is held HIGH in anticipation



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) FIFO is initially empty. $\overline{SO}$ is held HIGH.

(2) SI pulse; loads data into FIFO and initiates ripple through process

(3) Output transition; data arrives at output stage after the specified propagation delay between the rising and falling edge of the DOR pulse to the Qn output

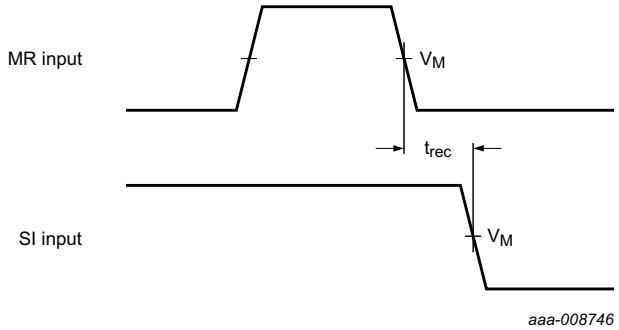
(4) DOR flag signals the arrival of valid data at the output stage

(5) $\overline{SO}$ set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty

(6) DOR goes LOW; data shift-out is completed, FIFO is empty again

Fig 14. Ripple through delay SI input to DOR output, propagation delay DOR input to Qn outputs and the DOR pulse width

11.9 MR to SI recovery time

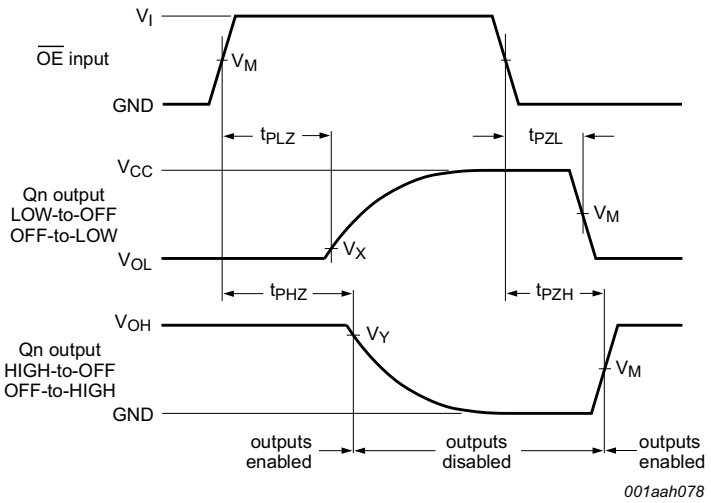


Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 15. MR to SI recovery time

11.10 Enable and disable times

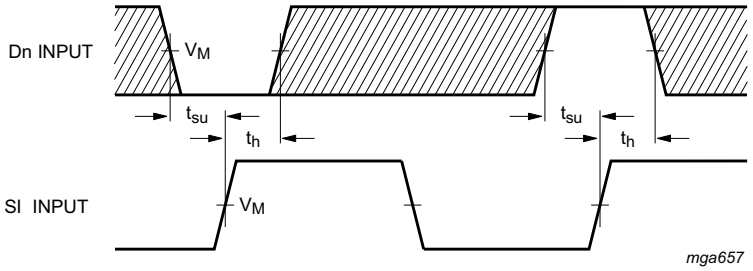


Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 16. Enable and disable times

11.11 Set-up and hold times



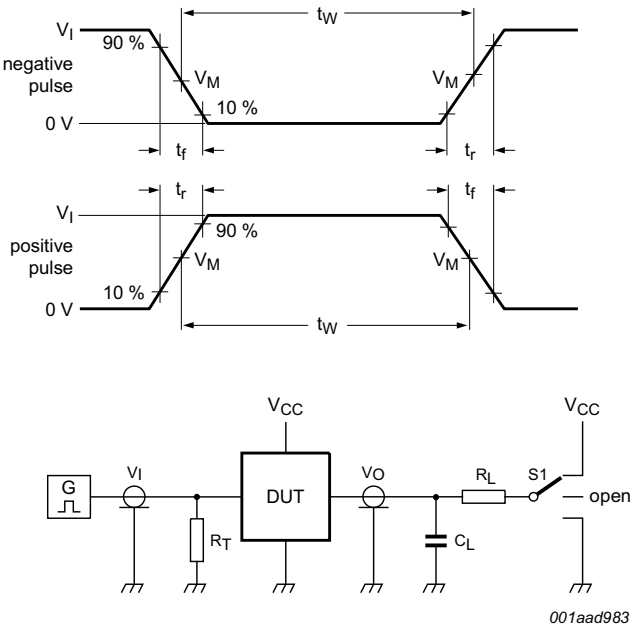
Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the output is permitted to change for predictable output performance

Fig 17. Set-up and hold times

11.12 Test circuit for measuring switching times



Test data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

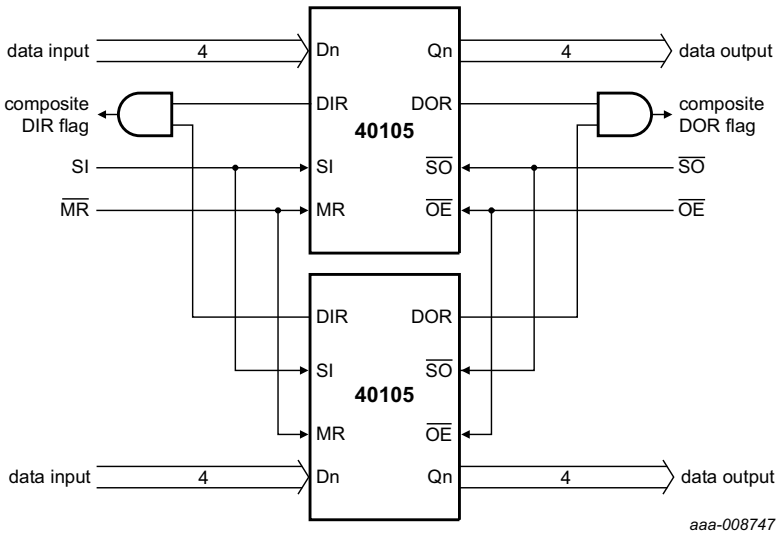
S1 = Test selection switch.

Fig 18. Test circuit for measuring switching times

Table 8. Test data

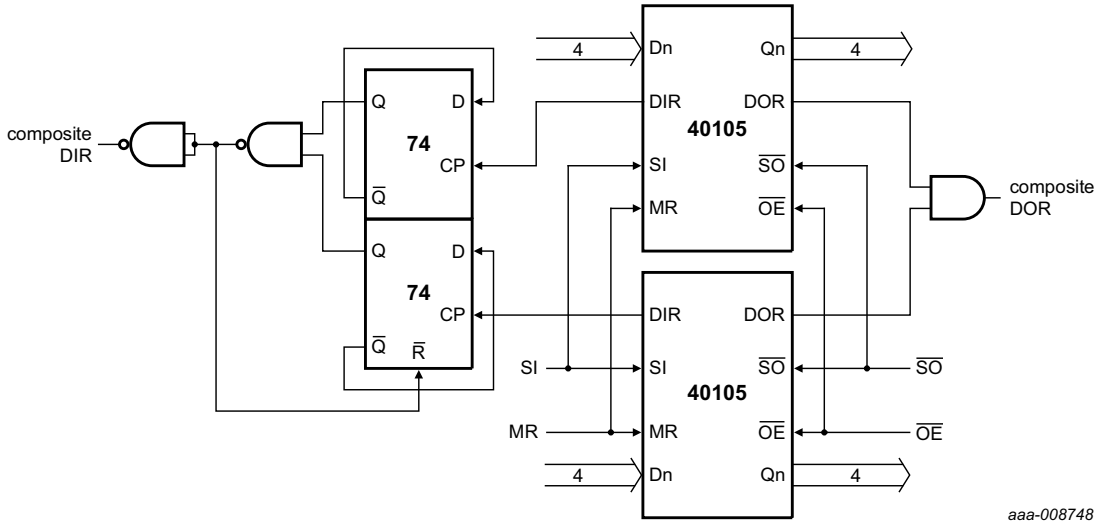
Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC40105	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT40105	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Application information



The 74HC40105; 74HCT40105 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, except for an added gate delay on the flags.

Fig 19. Expanded FIFO for increased word length; 16 words x 8 bits



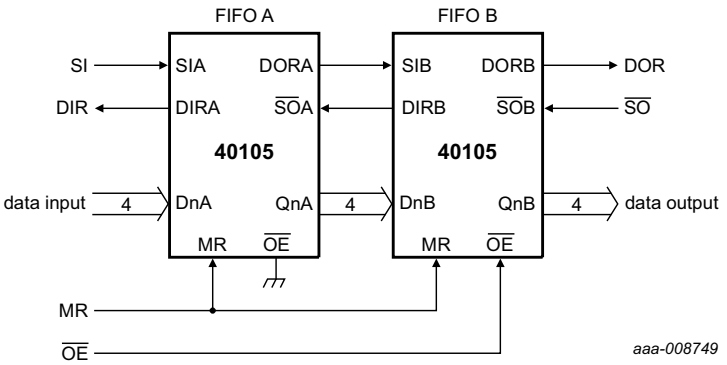
This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started (see Figure 9).

Fig 20. Expanded FIFO for increased word length

12.1 Expanded format

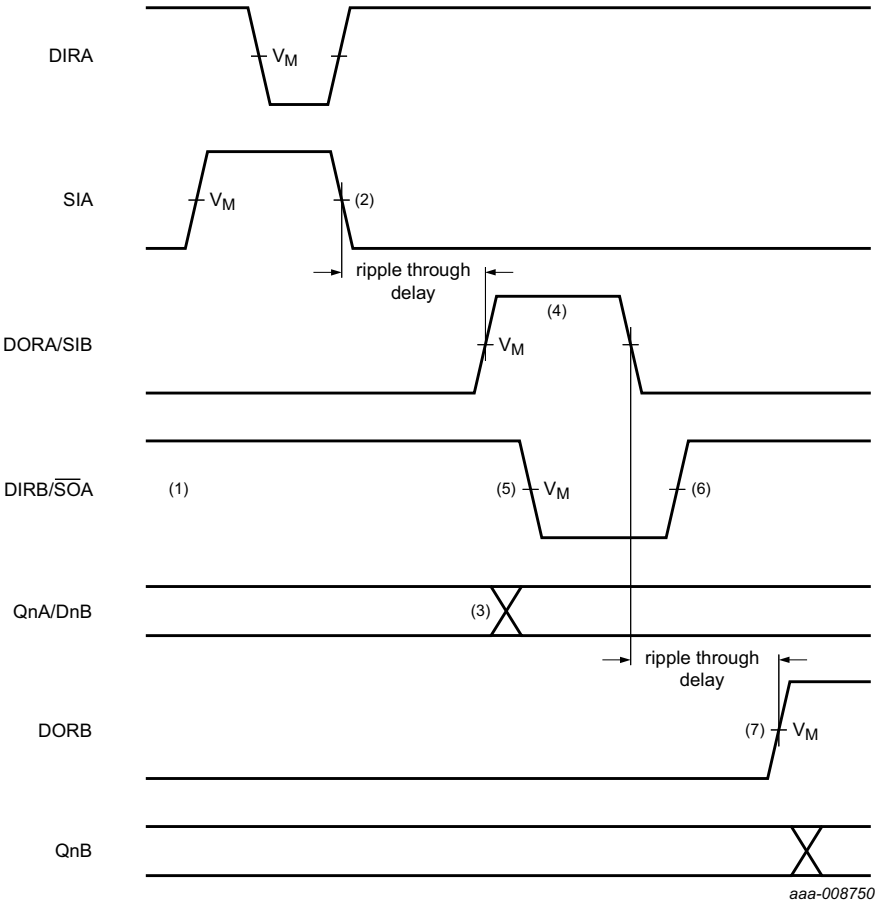
Figure 21 shows two cascaded FIFOs providing a capacity of 32 words x 4 bits. Figure 22 shows the signals on the nodes of both FIFOs after the application of the SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of FIFOA. Due to $\overline{SO}$A being HIGH, a DORA pulse is generated. The DORA pulse width and the timing between the rising edge of DORA and QnA satisfy the requirements of SIB and DnB. After a second ripple through delay data arrives at the output of FIFOB.

Figure 23 shows the signals on the nodes of both FIFOs after the application of the $\overline{SO}$B pulse, when both FIFOs are initially full. After a bubble-up delay, a DIRB pulse is generated, which acts as a $\overline{SO}$A pulse for FIFOA. One word is transferred from the output of FIFOA to the input of FIFOB. The pulse width of DORB satisfy the requirements of the $\overline{SO}$A pulse for FIFOA. After a second bubble-up delay, an empty space arrives at DnA, at which time DIRA goes HIGH. Figure 24 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.



The 74HC40105; 74HCT40105 is easily cascaded to increase word capacity without external circuitry. In cascaded format, the FIFOs handle all necessary communications. Figure 19 and Figure 21 demonstrate the communication timing between FIFOA and FIFOB. Figure 24 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

Fig 21. Cascading for increased word capacity; 32 words x 4 bits



(1) FIFOA and FIFOB are initially empty, $\overline{SO}$A held HIGH in anticipation of data

(2) Load one word into FIFOA; SI pulse; applied. results in DIR pulse

(3) Data-out A/ data-in B transition; valid data arrives at FIFOA output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFOB.

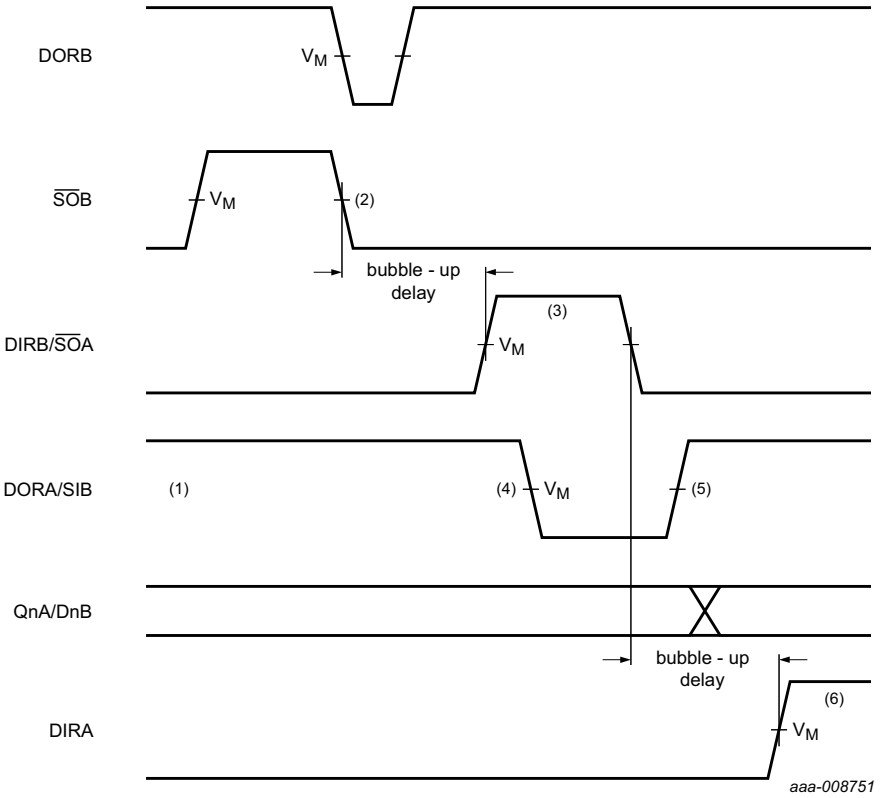
(4) DORA and SIB pulse HIGH; (ripple through delay after SIA LOW) data is unloaded from FIFOA as a result of the data output ready pulse, data is shifted into FIFOB

(5) DIRB and $\overline{SO}$A go LOW; flag indicates that input stage of FIFOB is busy, shift-out of FIFOA is complete

(6) $\overline{DIRB}$ and SOA go HIGH automatically; the input stage of FIFOB is again able to receive data, SO is held HIGH in anticipation of additional data

(7) $\overline{DORB}$ goes HIGH; (ripple through delay after SIB LOW) valid data is present one propagation delay later at the FIFOB output stage

Fig 22. FIFO to FIFO communication; input timing under empty condition



(1) FIFOA and FIFOB initially empty, SIB held HIGH in anticipation of shifting in new data as an empty location bubbles-up

(2) Unload one word from FIFOB; $\overline{SO}$ pulse applied, results in DOR pulse

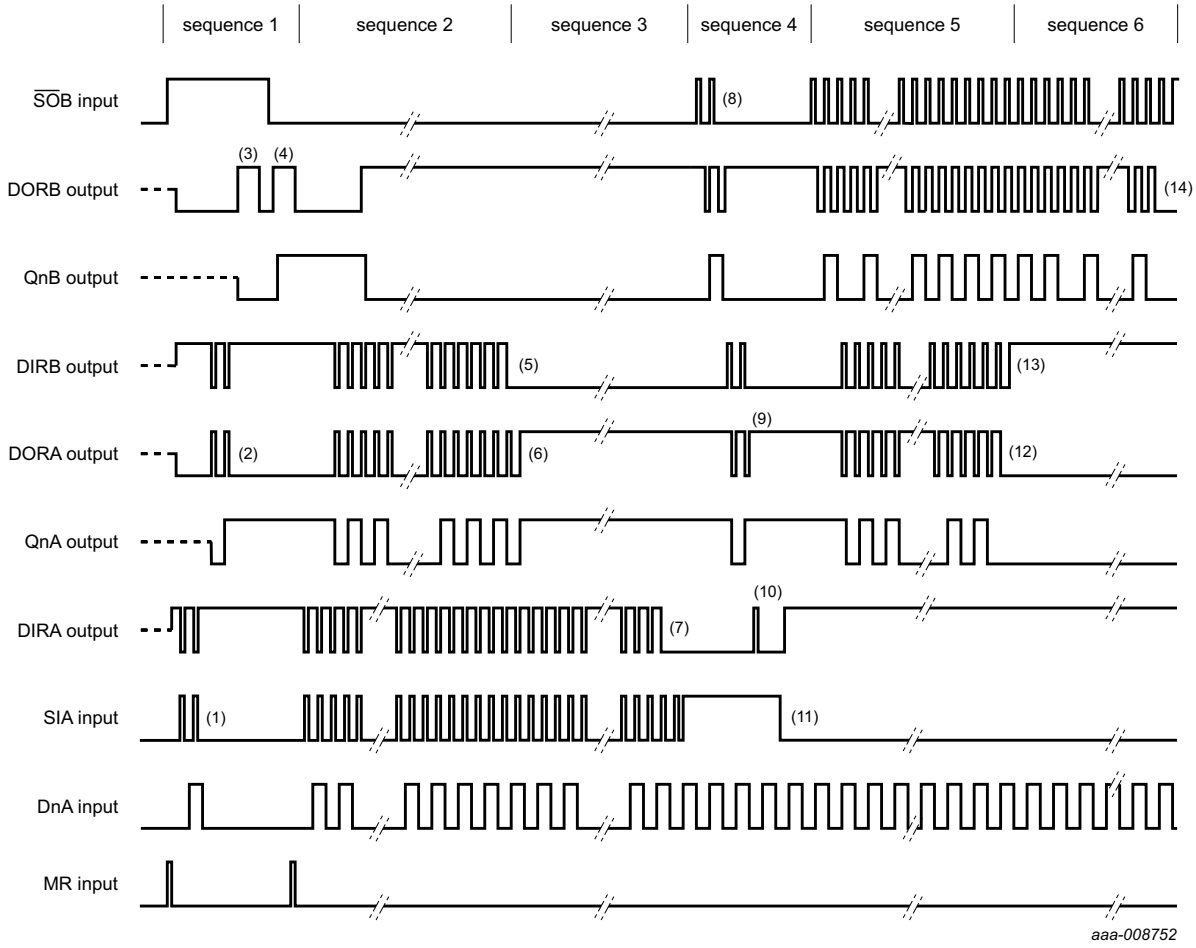
(3) DIRB and SOA pulse HIGH; (bubble-up delay after SOB LOW) data is loaded into FIFOB as a result of the DIR pulse, data is shifted out of FIFOA

(4) DORA and SIB go LOW; flag indicates that the output stage of FIFOA is busy, shift-in of FIFOB is complete

(5) DORA and SIB go HIGH; flag indicates that valid data is again available at FIFOA output stage, SIB is held HIGH, awaiting bubble-up of empty location.

(6) $\overline{\text{DIRA}}$ goes HIGH; (bubble-up delay after SOA LOW) an empty location is present at input stage of FIFOA

Fig 23. FIFO to FIFO communication; output timing under full condition



See also Section 12.1.1

Fig 24. Waveforms showing the functionality and intercommunication between to FIFOs (refer to Figure 19)

12.1.1 Sequence 1 (both FIFOs empty, starting SHIFT-IN process)

After an MR pulse has been applied, FIFOA and FIFOB are empty. The DOR flags of FIFOA and FIFOB go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SOB}$ is held HIGH and two SIA pulses are applied (1). These pulses allow two data words to ripple through the output stage of FIFOA and the input stage of FIFOB (2). When data arrives at the output of FIFOB, a DORB pulse is generated (3). When $\overline{SOB}$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DORB goes high (4).

12.1.2 Sequence 2 (FIFOB runs full)

After the MR pulse, a series of 16 SI pulses are applied. When 16 words are shifted in, DIRB remains LOW due to FIFOB being full (5). DORA goes LOW due to FIFOA being empty.

12.1.3 Sequence 3 (FIFOA runs full)

When 17 words are shifted in, DORA remains HIGH due to valid data remaining at the output of FIFOA. QnA remains HIGH, being the polarity of the 17th word (6). After the 32th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

12.1.4 Sequence 4 (both FIFOs full, starting SHIFT-OUT)

SIA is held HIGH and two $\overline{SOB}$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of FIFOB, and proceed to FIFOA (9). When the first empty location arrives at the input of FIFOA, a DIRA pulse is generated (10) and a new word is shifted into FIFOA. SIA is made LOW and now the second empty location reaches the input stage of FIFOA, after which DIRA remains HIGH (11).

12.1.5 Sequence 5 (FIFOA runs empty)

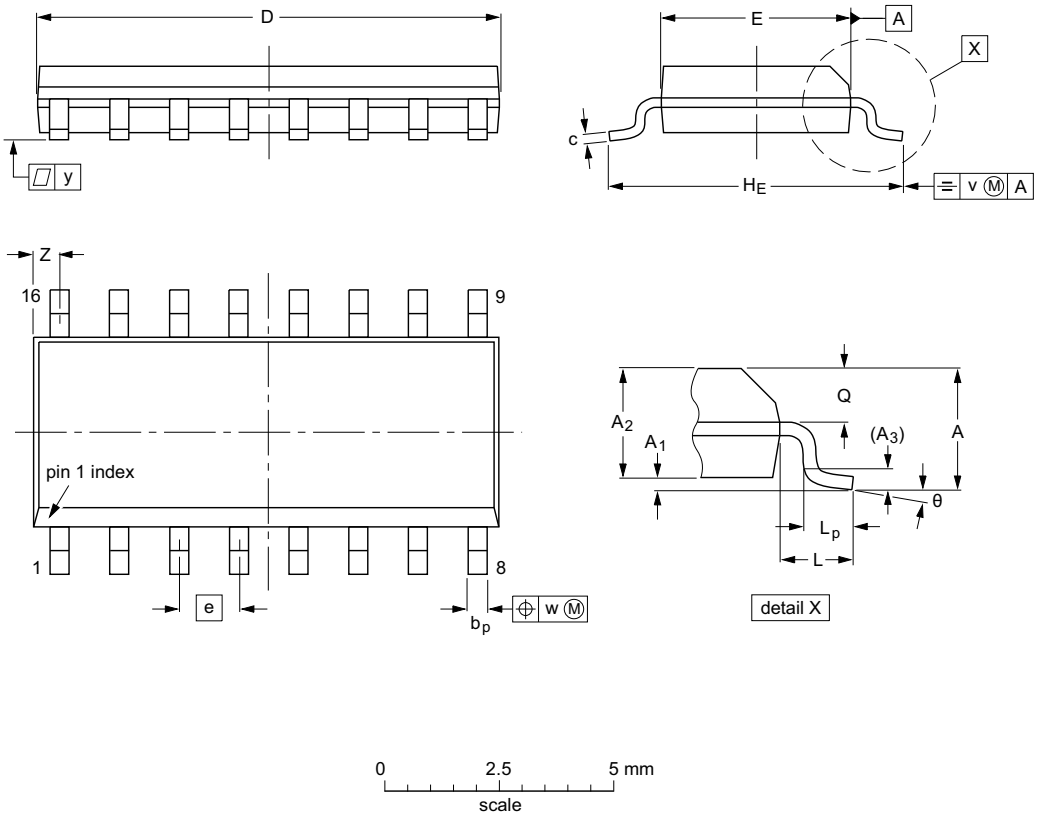
At the start of sequence 5, FIFOA contains 15 valid words due to two words being shifted out and one word being shifted in, in sequence 4. And additional series of $\overline{SOB}$ pulses are applied. After 15 $\overline{SOB}$ pulses, all words from FIFOA are shifted in FIFOB. DORA remains LOW (12).

12.1.6 Sequence 6 (FIFOB runs empty)

After the next $\overline{SOB}$ pulse, DIRB remains HIGH due to the input stage of FIFOB being empty (13). After another 15 $\overline{SOB}$ pulses, DORB remains LOW due to both FIFOS being empty (14). Additional $\overline{SOB}$ pulses have no effect. The last word remains available at the output Qn.

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

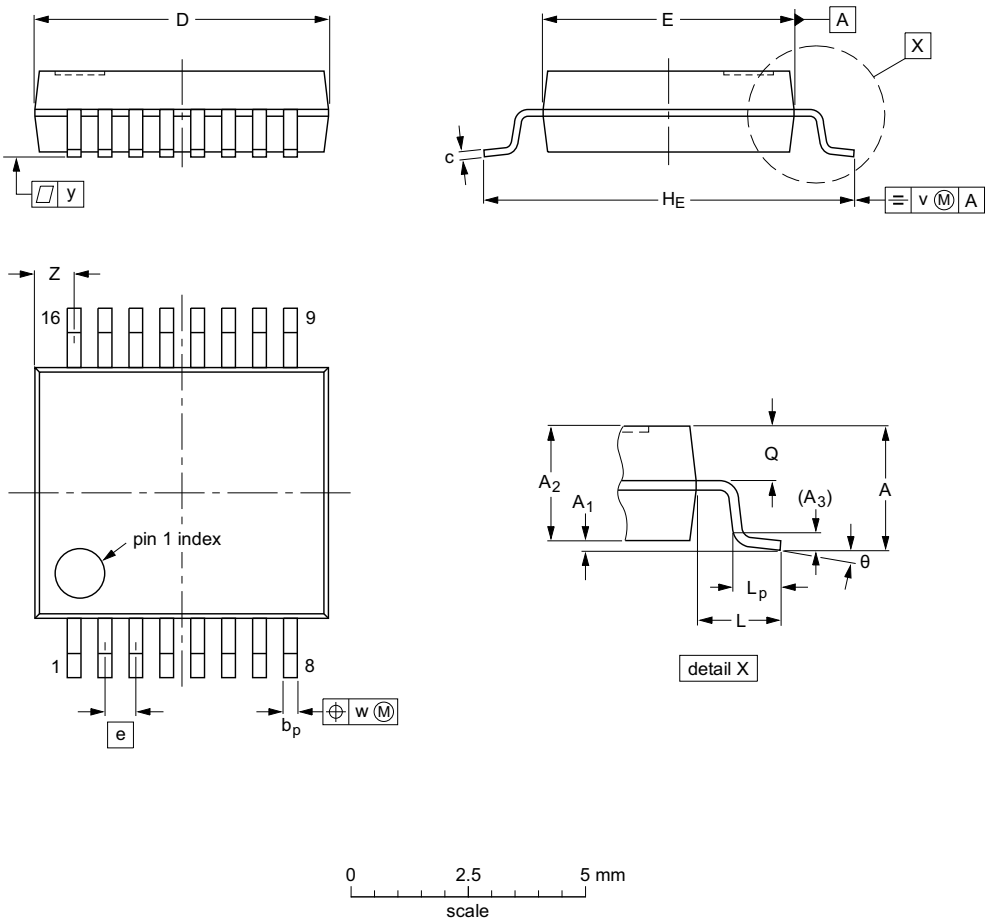
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 25. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

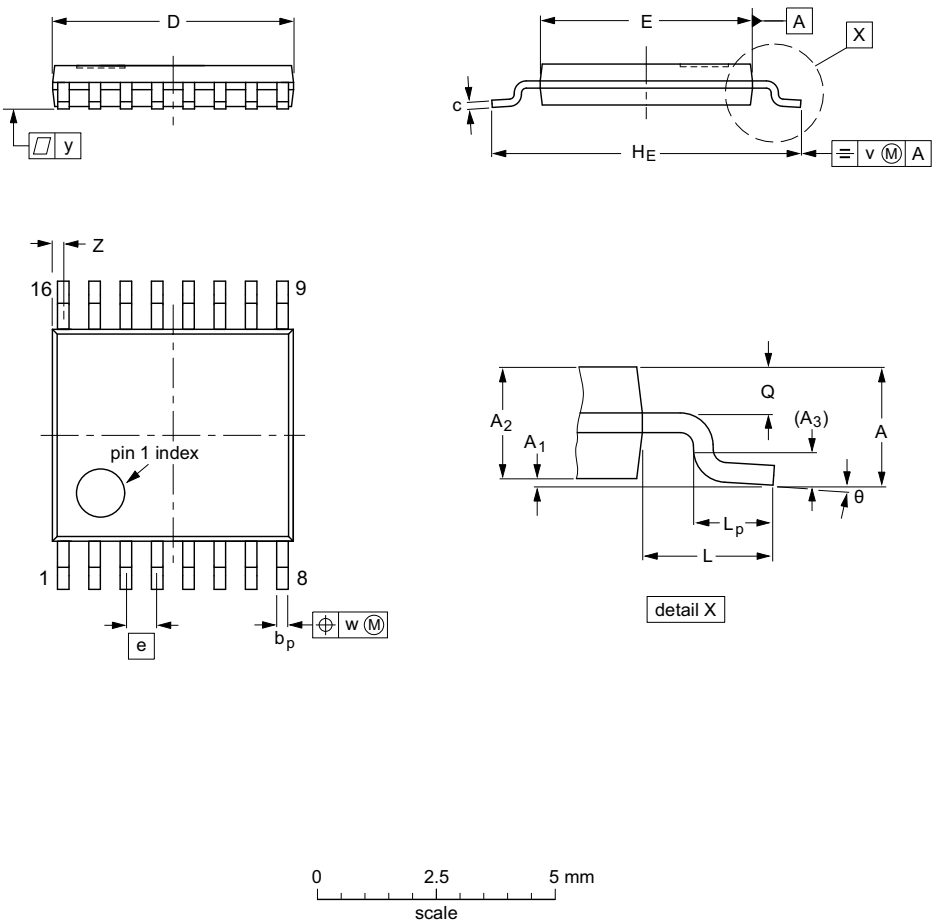
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 26. Package outline SOT338-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 27. Package outline SOT403-1 (SO16)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
FIFO	First In First Out

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT40105 v. 4	20160129	Product data sheet	-	74HC_HCT40105 v. 3
Modifications:	• Type numbers 74HC40105N and 74HCT40105N (SOT38-4) removed.			
74HC_HCT40105 v. 3	20130925	Product data sheet	-	74HC_HCT40105_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT40105_CNV v.2	19980123	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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18. Contents

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