晶 發 科 技 股 份 有 限 公 司
GI FAR TECHNOLOGY CO., LTD.
No. 81, Dongfeng St, Shulin District, 238034, New Taipei City, Taiwan, R.O.C.

SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFG128064I-FPFE-04

VERSION : C

DATE : 2022.11.21

CERTIFICATION : ROHS

Customer Sign	Approved By	Prepared By	Prepared By
	GIFAR 2022.11.21 Sidney	GIFAR 2022.11.21 Roger	GIFAR 2022.11.21 Hazel

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Revision Record

Data(y/m/d)	Ver.	Description	page
2012.08.31	A	Specification released	
2017.04.18	B	修改公司抬頭、格式統一	
2022.11.21	C	原 IC ST7565S 已經 EOL 替代料 ST7565P-G，更新規格書(4M-2022071101)	

CONTENTS

1. SCOPE

This specification covers the engineering requirements for the GFG128064I-FPFE-04 liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 128 × 64 dot matrix LCD
- FSTN , Positive mode LCD panel
- Transflective , Wide temperature type
- 6 o'clock
- Back light: Edge LED (white)
- Multiplexing driving : 1/65duty, 1/9bias
- Conteroller IC ST7565P-G

2.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	128 × 64
Dot dimensions(mm)	0.48 × 0.48
Dot spacing (mm)	0.52 × 0.52
Module dimensions (Horizontal × Vertical × Thickness, mm)	80 × 54 × 9.7 max.
Viewing area (Horizontal × Vertical, mm)	70.7 × 38.8
Active area (Horizontal × Vertical, mm)	66.52 × 33.24

2.3 Absolute Maximum Ratings (Without LED back-light)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	V_{DD}	V	-0.3 to +3.6
Input Voltage	V_{IN}	V	-0.3 to V_{DD}+0.3

Note 1: Referenced to V_{SS}=0V

2.4 Electrical Characteristics (Without LED back-light)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage(logic)	V_{DD}-V_{SS}	--	3.0	3.3	3.6	V
Input Voltage	V_{IH}	--	0.8V_{DD}	--	V_{DD}	V
	V_{IL}	--	V_{SS}	--	0.2V_{DD}	
Output Voltage	V_{OH}	I_{OH}=-0.1mA	0.8V_{DD}	--	V_{DD}	V
	V_{HL}	I_{OL}=0.1mA	V_{SS}	--	0.2V_{DD}	
Current Consumption	I_{DD}	V_{IN}=V_{DD}	--	0.4	2.0	mA

2.5 Optical Characteristics Absolute maximum ratings

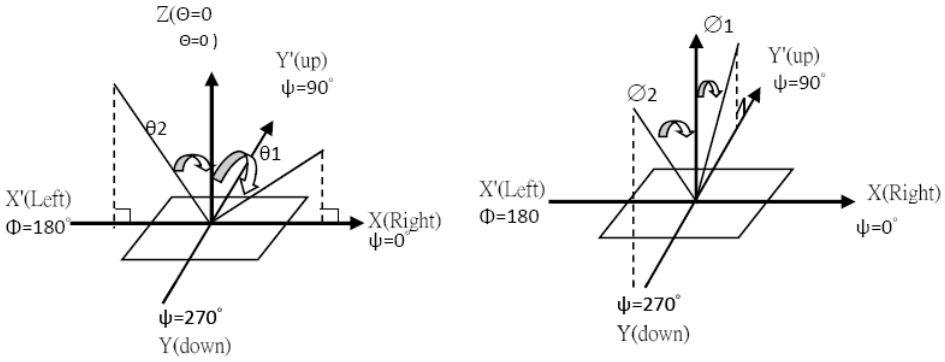
Item	Symbol	Rating	Unit
Operating temperature range	Top	-20~70	°C
Storage temperature range	Tst	-30~80	°C

2.6. Optical Characteristics

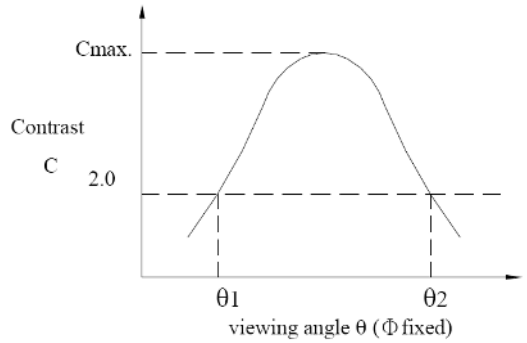
1/65 duty, 1/9 bias, Vop=9.5 V, Ta=25℃

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vop		9.2	9.5	9.8	
Viewing angle	θ1、θ2	C≥2.0,∅=0°C	30°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	2.0	-	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-	33	350ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	72	450ms	Note 4

Note 1: Definition of angles θ and ∅

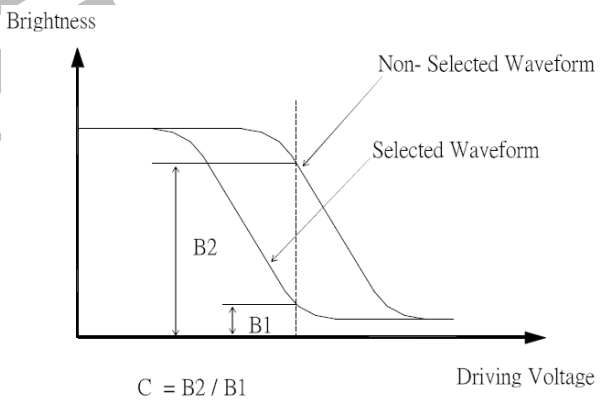


Note 2: Definition of viewing angles θ1 and θ2



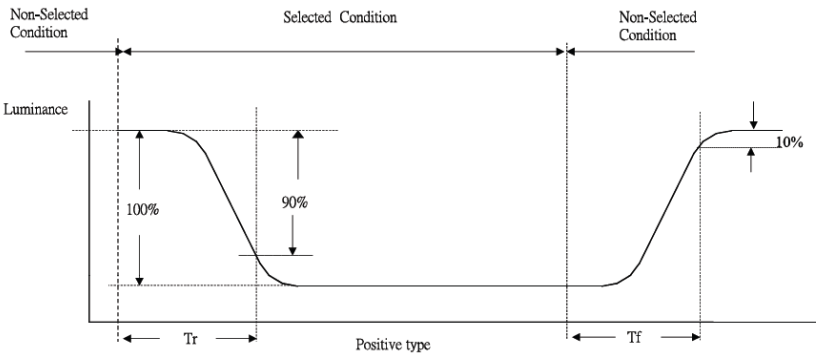
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C



C = B2 / B1

Note 4: Definition of response time



2.7 LED Back-light Characteristics

2.7.1 Electrical / optical specifications

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_f	If=80mA, White	2.7	3.0	3.3	V
LED *Luminous Intensity	I_V	If=80mA, White	400	600	--	cd/m^2
Chromaticity Coordinate	x	If=80mA, White	0.26	0.29	0.32	
	y		0.28	0.31	0.34	
Reverse Current	I_R	VR=5V, White	--	--	80	uA
Spectral Line half width	Δλ	If=80mA, White		30		nm
Luminous Uniformity	ΔLv	If=80mA, White	70			%

Note: * Measured at the bare LED back-light unit.

2.7.2 LED Maximum Operating Range

Item	Symbol	White	Unit
Power Dissipation	P_{AD}	256	mW
Forward Current	I_F	100	mA
Reverse Voltage	V_R	5	V

3. RELIABILITY

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	80℃	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-30℃	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40℃ 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	70℃	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	-20℃	120 hrs	Appearance Without defect	
6	Thermal Shock	-20℃, 30min. → 70℃,30min. ↑ (1cycle) ←		Appearance Without defect	10 cycles

** Dissipation current, contrast and display functions
** Polarizing filter deterioration, other appearance defects
** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.

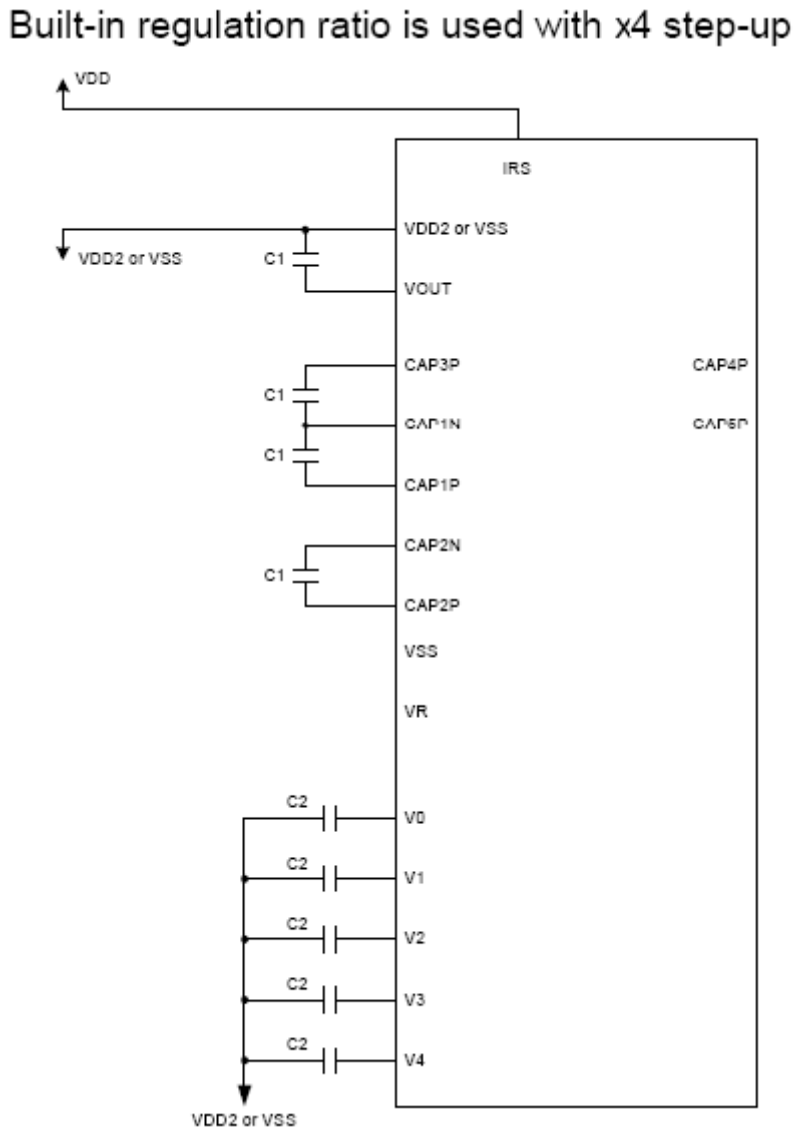
4. OPERATING INSTRUCTIONS

4.1 Input signal Function

Pin No	Symbol	I/O	Function
1	/CS1	I	This is the chip select signal. When CS1 = “L” and CS2 = “H,” then the chip select becomes active, and data/command I/O is enabled.
2	/RES	I	When RES is set to “L,” the settings are initialized. The reset operation is performed by the RES signal level.
3	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
4	WR(R/W)	I	• When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = “H”: Read. When R/W = “L”: Write.
5	RD(E)	I	• When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the RD signal of the 8080 MPU, and the ST7565S series data bus is in an output status when this signal is “L”. • When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.
6~13	D0 to D5 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = “L”) : D0 to D5 are set to high impedance. D6 : the serial clock input (SCL) ; D7 : serial data input (SI) . When the chip select is not active, D0 to D7 are set to high impedance.
14	VDD	PS	Shared with the MPU power supply terminal Vcc.
15	VSS	PS	This is a 0V terminal connected to the system GND.
16	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
17	CAP5+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
18	CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
19	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
20	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
21	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and

			the CAP2+ terminal.
22	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
23	CAP4+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
24	VRS	PS	This is the internal-output VREG power supply for the LCD power supply voltage regulator.
25~29	V4~V0	PS	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an opamp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. V0≧V1 ≧V2 ≧V3 ≧V4 ≧VSS
30	VR	I	Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider. IRS = “L” : the V5 voltage regulator internal resistors are not used . IRS = “H” : the V5 voltage regulator internal resistors are used .
31	C86	I	This is the MPU interface switch terminal. C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 MPU interface.
32	P/S	I	This pin configures the interface to be parallel mode or serial mode. P/S = “H”: Parallel data input/output. P/S = “L”: Serial data input. When P/S = “L”, D0 to D5 must be fixed to “H”. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. The serial access mode does NOT support read operation.
33	/HPM	I	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = “H”: Normal mode /HPM = “L”: High power mode
34	IRS	I	This terminal selects the resistors for the V5 voltage level adjustment. IRS = “H”: Use the internal resistors IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal

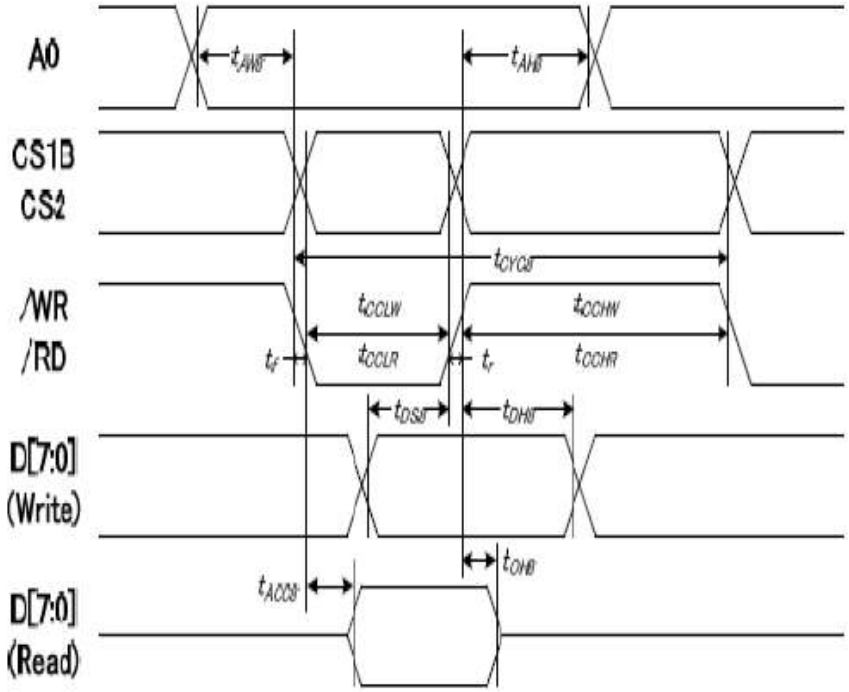
4.2 Voltage Generator Circuit



C1:1.0-4.7uf
C2:0.1-4.7uf

4.3 Timing Diagram

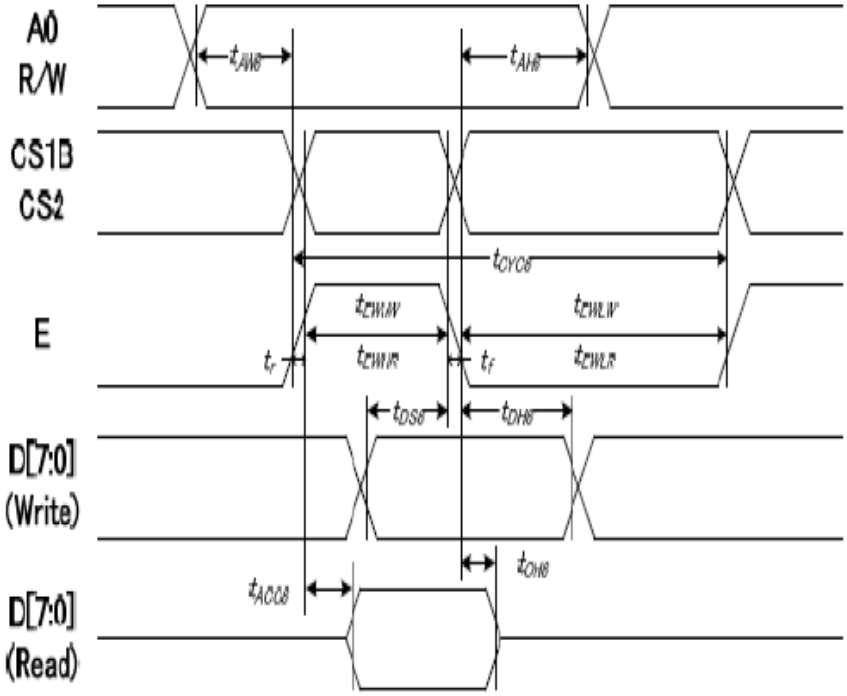
System Bus Timing for 8080 Series MPU



(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		240	—	
/WR L pulse width (WRITE)		tCCLW		80	—	
/WR H pulse width (WRITE)		tCCHW		80	—	
/RD L pulse width (READ)	RD	tCCLR		140	—	
/RD H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

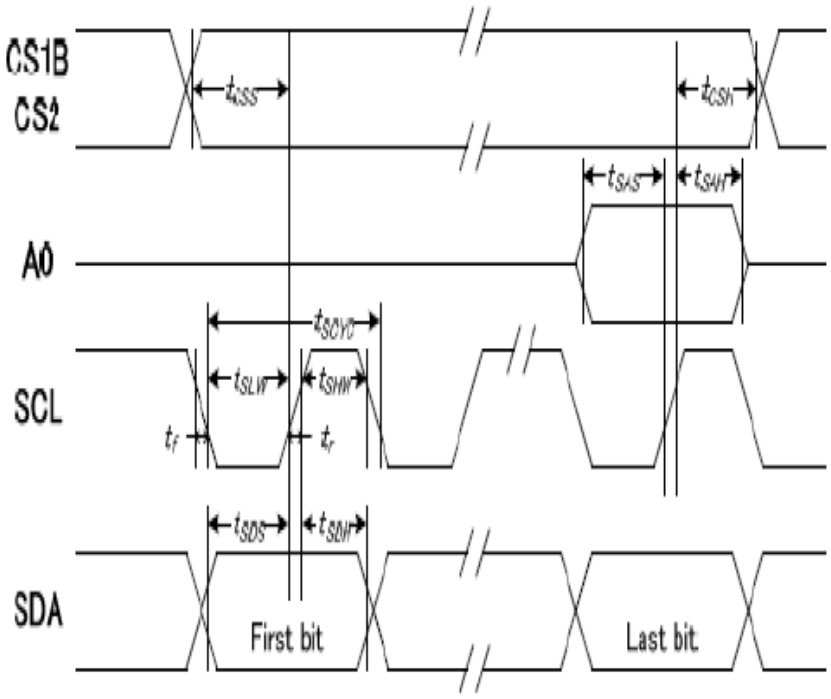
System Bus Timing for 6800 Series MPU



(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		0	—	
Read data access time		tACC6	CL = 100 pF	—	70	
Read data output disable time		tOH6	CL = 100 pF	5	50	

System Bus Timing for 4-Line Serial Interface



(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		50	—	ns
SCLK "H" pulse width		tSHW		25	—	
SCLK "L" pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCLK time	CS1B	tCSS		20	—	
CS-SCLK time	CS2	tCSH		40	—	

4.4. COMMAND LIST

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
Read Status	0	1	BUSY	MX	D	RST	0	0	0	0	Read IC Status
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
RESET	0	0	1	1	1	0	0	0	1	0	Software reset
COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
Power Save	0	0	Compound Command								Display OFF + All Pixel ON
Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL[1:0]=(0,0), x2, x3, x4 BL[1:0]=(0,1), x5 BL[1:0]=(1,1), x6
	0	0	0	0	0	0	0	0	BL1	BL0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Test	0	0	1	1	1	1	-	-	-	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

5. NOTES

▪ Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 °C±10 °C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

6. OPERATION PRECAUTIONS

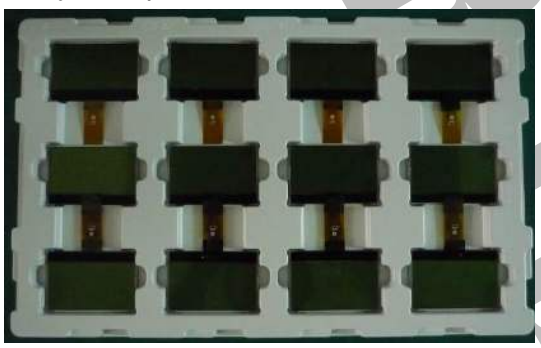
Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

Quality warranty period: Within one year after shipment date (excluding abnormal usage way and abnormal environments.)

7. PACKAGE INFORMATION

1	1 Tray	:	12 pcs (modules)
2	1 stack	:	7 tray +1 Cover tray
3	1 Carton	:	(1 Cover tray + 7 tray)x 3 stack
4	Total pcs	:	1 Carton (12pcs * 7tray * 3 stack) = 252 pcs
5	Carton size = NO. 17	:	495*315*435mm
7	Net weight	:	7.8 KG
8	Gross weight	:	12.2 KG

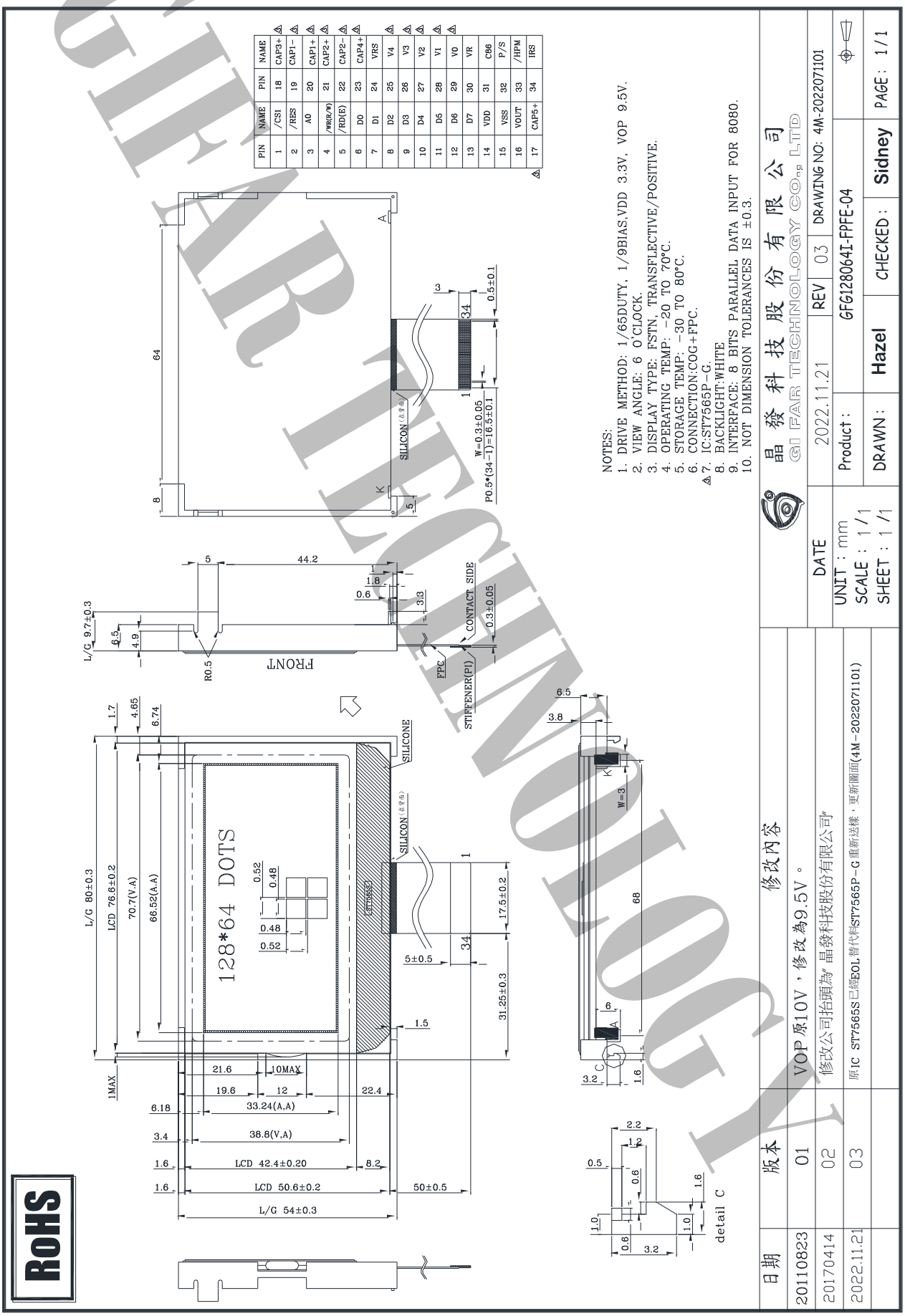
- 1 Tray = 12 pcs



- 1 stack=7 tray+1 Cover tray **Each layer of tray should be staggered stacked

- 1 Carton = 3 stack, Total pcs = 252 pcs

8. LCM Dimension



出貨檢驗標準書

Shipping inspection standard

核准 Approved by	審核 Checked by	作成 Made by
ANDY	JACKY	RUBY

1.目的 Purpose：
規範出貨產品之檢驗項目及判斷標準，確保產品出貨能滿足客戶要求。
Standardize the inspection items and judgment standards to ensure the products that shipped out can meet customer's requirements.

2.範圍 Area：
適用於出廠之所有產品。
Applicable to all products shipped from the factory.

3.名詞解釋 Explanation of terms：
3-1 主要缺陷：亦會造成功能缺失或嚴重外觀缺陷。
Major Defects: It also causes loss of function or serious appearance defects.

3-2 次要缺陷：稍有缺陷但不影響客戶使用。
Minor defect: Slightly defective but does not affect customer use.

4.檢驗體制 Inspection system：
4-1 抽樣計劃：依 ANSI/ASQ Z1.4 一般檢驗水準Ⅱ 之 正常檢驗一次抽驗方案。
Sampling plan: According to ANSI/ASQ Z1.4 general inspection level Ⅱ the normal inspection one-time sampling plan.

4-2 允收水準 Acceptable Level：(AQL)
主要缺陷 Major defect：0.4 %
次要缺陷 Minor defect：0.65 %

5.檢驗條件 Inspection conditions：
5-1 使用相關之檢測儀器及測試、量測工具。
Use relevant testing instrument, testing and measuring tools .

5-2 環境要求：其條件需控制在常溫下 23℃±3℃及溼度 70%RH 以下。
Environmental requirements: The conditions should be controlled at room temperature 23℃±3℃ and humidity below 70%RH.

5-3 外觀檢驗：須在 380±20% LUX 的白色日光燈下，其目視距離需於產品離 30±5 cm 檢驗。
Appearance inspection: Under the white fluorescent lamp of 380±20% LUX , the visual distance shall be checked above the product 30 ± 5 cm.

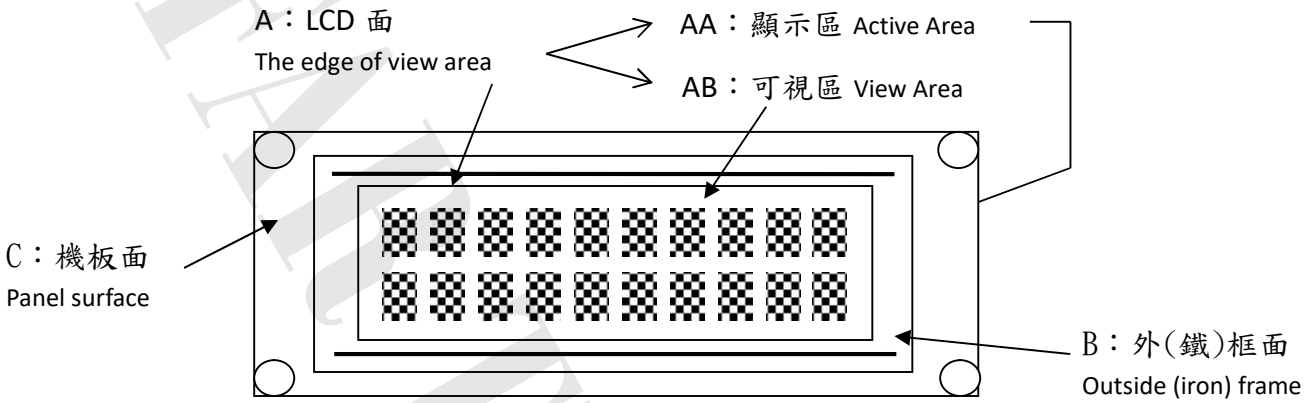
5-4 電性測試 Electrical Testing：
5-4-1 有背光之產品需關燈並在 5~300Lux±3%下檢驗。
The products with backlight should be tested at 5~300±3% Lux.

5-4-2 無背光之產品需開燈並在 60~300Lux±3%白色日光燈下檢驗。
Products without backlight need to be turned on and tested under 60~300 ± 3% LUX white fluorescent lamps .

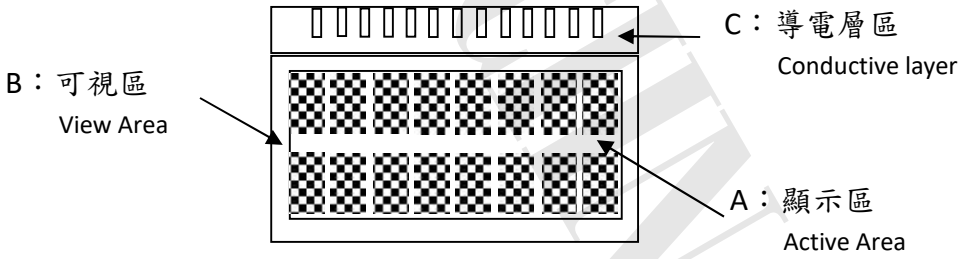
5-5 檢查視角依產品視角方向。
Check the viewing angle according to the product viewing angle.

5-6 其不良現象檢視區域 Bad phenomenon View area

5-6-1 適用種類 Applicable category：COB、TFT



5-6-2 適用種類 Applicable category：COG、TAB、TN



COG

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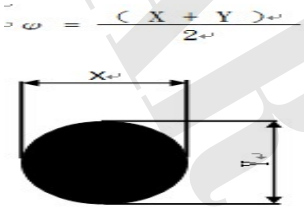
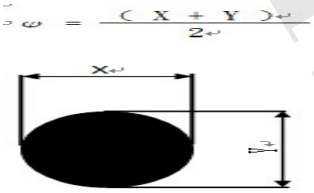
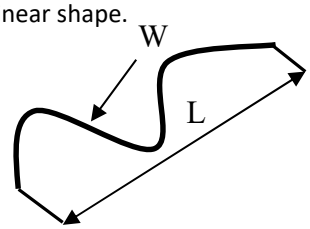
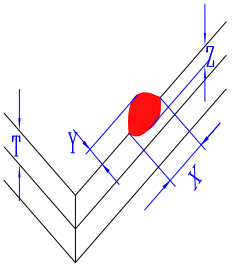
<tr><td>編號
No.</td><td>檢驗項目
Item</td><td colspan="2">檢驗內容及判定標準
Inspection Content & Standard</td><td>區域
Zone</td><td>類別
Category</td><td>缺陷等級
Level</td></tr>
<tr><td>1</td><td>點類(一)
Dot(1)</td><td>黑點、刺傷…等圓狀
Black dot、Stab…and other round shape
  </td><td>兩點距離須超過 5 ㎜
Two points have to be ≧ 5 mm<table><tr><td>φ (㎜)</td><td>允收數
Acceptance Qty</td></tr><tr><td>ϕ ≦ 0.1</td><td>無視 Ignore</td></tr><tr><td>0.1 < ϕ ≦ 0.25</td><td>3</td></tr><tr><td>0.25 < ϕ ≦ 0.3</td><td>1</td></tr><tr><td>ϕ > 0.3</td><td>0</td></tr></table></td><td>A
B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>2</td><td>點類(二)
Dot(2)</td><td>氣泡、凹凸點
Bubble、Uneven dots
  </td><td>兩點距離須超過 5 ㎜
Two points have to be ≧ 5 mm<table><tr><td>φ (㎜)</td><td>允收數
Acceptance Qty</td></tr><tr><td>ϕ ≦ 0.2</td><td>無視 Ignore</td></tr><tr><td>0.2 < ϕ ≦ 0.5</td><td>2</td></tr><tr><td>ϕ > 0.5</td><td>0</td></tr></table></td><td>A
B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>3</td><td>線類
Line</td><td>刮傷、毛屑…等線狀
Scratch、Fiber.. and other linear shape.
  </td><td><table><tr><td>L (㎜)</td><td>W (㎜)</td><td>允收數
Acceptance Qty</td></tr><tr><td>--</td><td>W ≦ 0.02</td><td>無視 Ignore</td></tr><tr><td>L ≦ 5</td><td>W ≦ 0.03</td><td>3</td></tr><tr><td>L ≦ 3</td><td>W ≦ 0.05</td><td>2</td></tr><tr><td>L > 5</td><td>W > 0.05</td><td>0</td></tr></table></td><td>A
B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>4</td><td>底色
Background color</td><td colspan="2">同批供貨不能有明顯色差
No obvious color difference allowed in same shipment.
(必要時與客端制定限度樣)
(According to the gold samples if necessary)</td><td>B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>5</td><td>FPC 外觀
FPC Appearance</td><td colspan="2">※ FPC 上刺傷導致線路無法導通 拒收
Stabbing on the FPC causes the line to fail to conduct
Reject
※ FPC 上髒污或是殘留異物以致線路無法導通 拒收
Dirty or residual foreign matter on the FPC makes the circuit unable to conduct
Reject
※ FPC 直角折痕、斷裂 拒收
FPC right-angle crease and fracture Reject</td><td>C</td><td>外觀
Appearance</td><td>主要
Major
AQL 0.4%</td></tr>
</table>

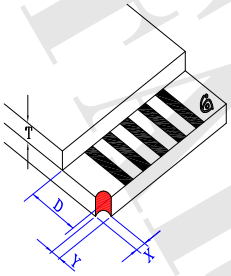
COG

6	點、線類 (三) Dot、Line (3)	※ 於全黑、白畫面下看見之區塊狀或線狀不良　拒收 There is a block or linear in the view area under the screen is whole black or white. Reject ※ 但依 2% ND Filter 遮蓋無視　允收 But after inspecting by 2% ND Filter without seeing block or linear, it is confirmed Acceptance	A	電訊 Electronics	次要 Minor AQL0.65%
7	點、線類 (四) Dot、Line (4)	畫面中顯示出現黑、白、亮、異色點或線狀 There is a black, white, bright or other dot or lines showing in the view area. ※ 依編號 1、3 之判定標準 According to the inspection standard: No. 1 and 3.	A	電訊 Electronics	次要 Minor AQL0.65%
8	缺字 Lack of characters	顯示時畫面缺少部份字元　拒收 Lacking part of characters in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
9	無動作 No reaction	顯示畫面一直處於起始畫面而無法進行切換　拒收 The display (view area) always show in the initial screen and can't be switched to others. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
10	無畫面 No display	通電後，完全無任何畫面顯示　拒收 After connecting to the power, there is no image. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
11	斷線 Broken line	顯示畫面中少直、橫線　拒收 There is a lack of vertical or horizontal lines in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%
12	CROSS TALK	顯示畫面時有局部之條紋或拖影 There are some stripes or shadow/smear showing in the view area. 拒收或與客端簽訂限度樣 Reject or inspect according to the golden sample	A	電訊 Electronics	次要 Minor AQL0.65%
13	I CON	顯示畫面缺少部份顯示圖案　拒收 Lack of partial ICON in the view area. Reject	A	電訊 Electronics	主要 Major AQL 0.4%

COG

<table>
<tr><td>14</td><td>深淺不一
Color difference</td><td>顯示畫面的對比，比其他顯示深或淺並依電氣規格(VOP)值判定
The color contrast of display is obviously lighter or darker than others and according to the VOP value in the electronics specification.
拒收或與客端簽訂限度樣
Reject or inspect according to the golden sample</td><td>A</td><td>電訊
Electronics</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>15</td><td>畫面異常
Abnormal screen</td><td>通電後畫面出現未定義之電訊不良現象　拒收
After connecting to the power, there is an undefined electronics appearance showing in the view area.
Reject</td><td>A</td><td>電訊
Electronics</td><td>主要
Major
AQL 0.4%</td></tr>
<tr><td>16</td><td>背光色不均
Uneven color of backlight</td><td>※ 點亮後 LED 有明暗不均現象依其均勻度判定　拒收
After lighting LEDs have brightness and darkness uneven the determined according to its uniformity.
Reject
※ 點亮後 LED 色澤不一致　拒收
LED color is inconsistent after lighting.
Reject</td><td>A</td><td>電訊
Electronics</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>17</td><td>亮度不足
Lack of brightness</td><td>波長、色座標、輝度與圖面標示定義不符　拒收
Wave length, chromatic coordinates, brightness don’t correspond to the definition of the drawing.
Reject</td><td>A</td><td>電訊
Electronics</td><td>主要
Major
AQL 0.4%</td></tr>
<tr><td>18</td><td>背光腳柱
Backlit foot post</td><td>斷裂、長度不一　拒收
Fracture, different length
Reject</td><td>--</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
<tr><td>19</td><td>破損
Damaged</td><td> 
</td><td>Y：破損寬 X：破損長
Y: Damaged width X: Damaged length
<table><tr><th>Y</th><th>X</th><th>判定
Determination</th></tr><tr><td>Y ≦1.0</td><td>-- --</td><td>允收
Acceptance</td></tr><tr><td>未進入可視區
Did not enter the viewing area</td><td>≦1/8 玻璃該邊長
≦1/8 The side length of the glass</td><td>允收
Acceptance</td></tr><tr><td>進入可視區
Enter the viewing area</td><td>-- --</td><td>拒收
Reject</td></tr></table></td><td>B</td><td>外觀
Appearance</td><td>次要
Minor
AQL0.65%</td></tr>
</table>

COG

<table>
<tr>
<td>20</td>
<td>角崩
Corner collapse</td>
<td>  </td>
<td>Y：破損寬 X：破損長
Y: Damaged width X: Damaged length
<table>
<tr><th>Y</th><th>X</th><th>判定
Determination</th></tr>
<tr><td>≦1/3D</td><td>-- --</td><td>允收
Acceptance</td></tr>
<tr><td>1/3D < Y ≦ D</td><td>≦1/8 玻璃邊長
≦1/8 The side length of the glass</td><td>允收
Acceptance</td></tr>
<tr><td>> D</td><td>-- --</td><td>拒收
Reject</td></tr>
</table></td>
<td>C</td>
<td>外觀
Appearance</td>
<td>次要
Minor
AQL0.65%</td>
</tr>
<tr>
<td>21</td>
<td>尺寸量測
Size Measurement</td>
<td>未依圖面上標示 拒收
No correspond to the indication on the drawing.
Reject</td>
<td>ALL</td>
<td>外觀
Appearance</td>
<td>主要
Major
AQL 0.4%</td>
</tr>
<tr>
<td>22</td>
<td>其他
Other</td>
<td>如發現有上述未定義之不良則與客端簽訂限度樣
If there is another undefined defective situation. It will be listed as others. The inspection standard is according to the golden sample.</td>
<td>ALL</td>
<td>電訊
Electronics
外觀
Appearance</td>
<td>次要
Minor
AQL0.65%</td>
</tr>
</table>