

BLC8G09XS-400AVT

Power LDMOS transistor

Rev. 2 — 24 November 2017

AMMPLION

Product data sheet

1. Product profile

1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 791 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in an asymmetrical Doherty production test circuit.

$V_{DS} = 32\text{V}$; $I_{Dq} = 880\text{ mA}$ (main); $V_{GS(amp)peak} = 0.8\text{ V}$, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	791 to 821	32	93	17.2	46	-34 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

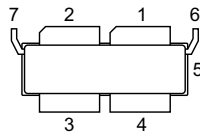
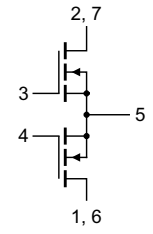
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 791 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		 <p>aaa-014884</p>
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC8G09XS-400AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[1]	225	°C
T_{case}	case temperature	operating	[1]	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 32\text{ V}; I_{Dq} = 880\text{ mA (main)};$ $V_{GS(amp)peak} = 0,5\text{ V}; T_{case} = 80\text{ °C}$		
		$P_L = 93\text{ W}$	0.27	k/W
		$P_L = 117\text{ W}$	0.24	k/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 32\text{ V}; I_D = 880\text{ mA}$	-	2.1	-	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	37	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 11\text{ A}$	-	14.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	92	151	$\text{m}\Omega$
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 350\text{ mA}$	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 32\text{ V}; I_D = 2000\text{ mA}$	-	2.1	-	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	56	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 17.5\text{ A}$	-	22	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 12.25\text{ A}$	-	61	99	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; $f_1 = 791\text{ MHz}; f_2 = 821\text{ MHz}$; RF performance at $V_{DS} = 32\text{ V}; I_{Dq} = 880\text{ mA}$ (main); $V_{GS(amp)peak} = 0.8\text{ V}; T_{case} = 25\text{ °C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 93\text{ W}$	16	17	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 93\text{ W}$	-	-16	-12	dB
η_D	drain efficiency	$P_{L(AV)} = 93\text{ W}$	42	46	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 93\text{ W}$	-	-33	-29	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; $f = 791\text{ MHz}$; RF performance at $V_{DS} = 32\text{ V}; I_{Dq} = 880\text{ mA}$ (main); $V_{GS(amp)peak} = 0.8\text{ V}; T_{case} = 25\text{ °C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 791 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)} = 120\text{ W}$	6.0	6.6	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)} = 120\text{ W}$	470	540	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC8G09XS-400AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 32\text{ V}$; $I_{Dq} = 880\text{ mA}$; $V_{GS(amp)peak} = 0.8\text{ V}$; $f = 791\text{ MHz}$; $P_L = 170\text{ W}$ (5 dB OBO); 1-carrier W-CDMA. Test signal: 3GPP test model 1; 1 to 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF per carrier

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{Dq} = 1300\text{ mA}$ (main); $V_{DS} = 32\text{ V}$; pulsed CW ($t_p = 100\text{ }\mu\text{s}$; $\delta = 10\%$).

f (MHz)	Z _S [1] (Ω)	Z _L [1] (Ω)	P _L [2] (W)	η _D [2] (%)	G _p [2] (dB)
Maximum power load					
800	2.8 – j2.6	1.7 – j1.3	280	60.4	18.0
810	2.8 – j2.7	1.7 – j1.3	280	60.6	17.9
820	2.8 – j3.1	1.7 – j1.3	280	60.5	17.9
869	2.9 – j3.7	1.7 – j1.7	270	61.3	17.5
890	3.1 – j3.9	1.3 – j1.5	270	56.0	16.7
920	3.8 – j4.1	1.3 – j1.5	280	57.6	16.7
940	4.0 – j4.7	1.4 – j1.5	280	58.9	16.6
960	4.2 – j4.9	1.3 – j1.5	285	59.4	16.5
Maximum drain efficiency load					
800	2.8 – j2.6	2.7 – j2.6	218	69.7	19.5
810	2.8 – j2.7	3.2 – j2.4	200	69.8	19.8
820	2.8 – j3.1	3.2 – j2.4	200	69.5	19.7
869	2.9 – j3.7	4.0 – j2.9	170	69.4	19.4
890	3.1 – j3.9	3.6 – j2.0	190	70.2	19.2
920	3.8 – j4.1	3.7 – j1.3	190	72.1	19.1
940	4.0 – j4.7	3.8 – j1.3	185	72.3	19.0
960	4.2 – j4.9	3.0 – j1.2	210	71.8	18.6

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; $I_{Dq} = 1900 \text{ mA (peak)}$; $V_{DS} = 32 \text{ V}$; pulsed CW ($t_p = 100 \mu\text{s}$; $\delta = 10 \%$).

f	Z _S [1]	Z _L [1]	P _L [2]	η _D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
800	2.3 – j4.3	1.0 – j1.5	430	58.0	16.4
810	2.3 – j4.4	1.0 – j1.5	430	58.0	16.4
820	2.7 – j4.7	1.0 – j1.5	430	58.0	16.3
869	2.9 – j5.5	1.0 – j1.5	420	57.8	15.8
890	3.2 – j5.9	1.0 – j1.5	420	58.6	15.6
920	3.8 – j6.3	1.0 – j1.5	425	59.5	15.5
940	4.5 – j6.9	0.9 – j1.6	425	56.4	14.8
960	4.8 – j7.0	0.9 – j1.6	425	56.8	14.7
Maximum drain efficiency load					
800	2.3 – j4.3	2.4 – j2.7	265	69.6	18.5
810	2.3 – j4.4	2.3 – j2.2	305	70.0	18.2
820	2.7 – j4.7	2.3 – j2.2	305	69.8	18.1
869	2.9 – j5.5	2.8 – j2.5	255	69.4	17.6
890	3.2 – j5.9	2.5 – j1.9	285	69.9	17.3
920	3.8 – j6.3	2.6 – j1.5	280	71.5	17.2
940	4.5 – j6.9	2.7 – j1.5	275	71.4	16.9
960	4.8 – j7.0	2.6 – j1.2	270	71.6	16.8

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At 3 dB gain compression.

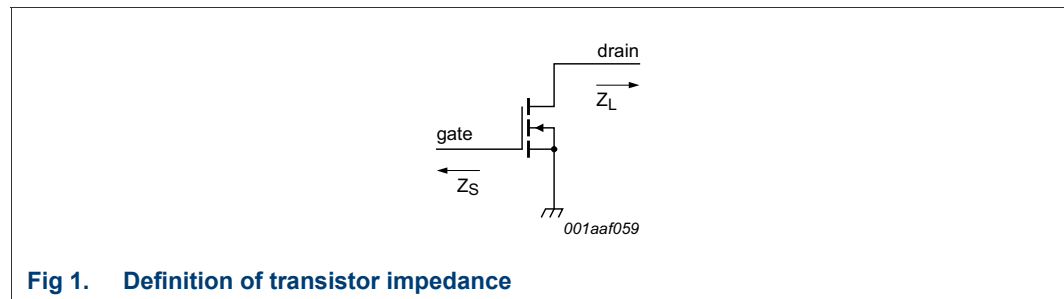


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; $I_{Dq} = 1300$ mA (main); $V_{DS} = 32$ V; pulsed CW ($t_p = 100$ μ s; $\delta = 10$ %).

f	Z _S [1]	Z _L [1]	P _{L(3dB)} [2]	η_D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
869	3.1 – j3.9	2.0 – j1.6	215	41.8	19.5
890	3.0 – j4.1	1.9 – j1.2	215	42.3	19.7

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At P_{L(AV)} = 93 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; $I_{Dq} = 1300$ mA (main); $V_{DS} = 32$ V; pulsed CW ($t_p = 100$ μ s; $\delta = 10$ %).

f	Z _S [1]	Z _L [1]	P _{L(3dB)} [2]	η_D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
869	3.1 – j3.9	4.9 – j1.7	120	59.2	21.5
890	3.0 – j4.1	4.8 – j1.5	120	59.5	21.4

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At P_{L(AV)} = 93 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; $I_{Dq} = 1900$ mA (peak); $V_{DS} = 32$ V; pulsed CW ($t_p = 100$ μ s; $\delta = 10$ %).

f	Z _S [1]	Z _L [1]	P _{L(3dB)} [2]	η_D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
869	3.3 – j5.1	1.3 – j1.9	315	33.4	18.3
890	3.5 – j5.5	1.2 – j1.6	320	34.0	18.4

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At P_{L(AV)} = 93 W.

Table 14. Off-state impedances of peak device

f	Z _{off}
(MHz)	(Ω)
800	3.8 + j2.9
810	3.9 + j2.8
820	4.1 + j2.8
869	4.6 + j2.0
890	4.7 + j1.5
920	4.7 + j0.8
940	4.4 + j0.3
960	4.1 + j0.1

7.4 Test circuit

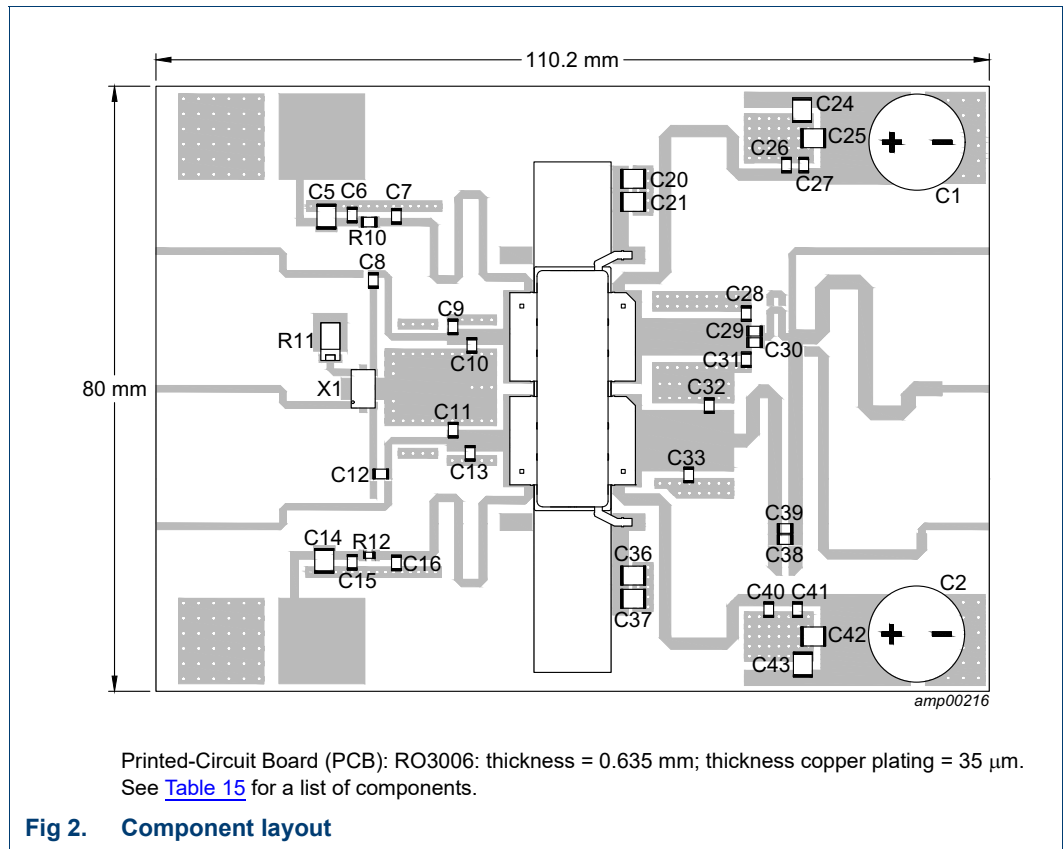


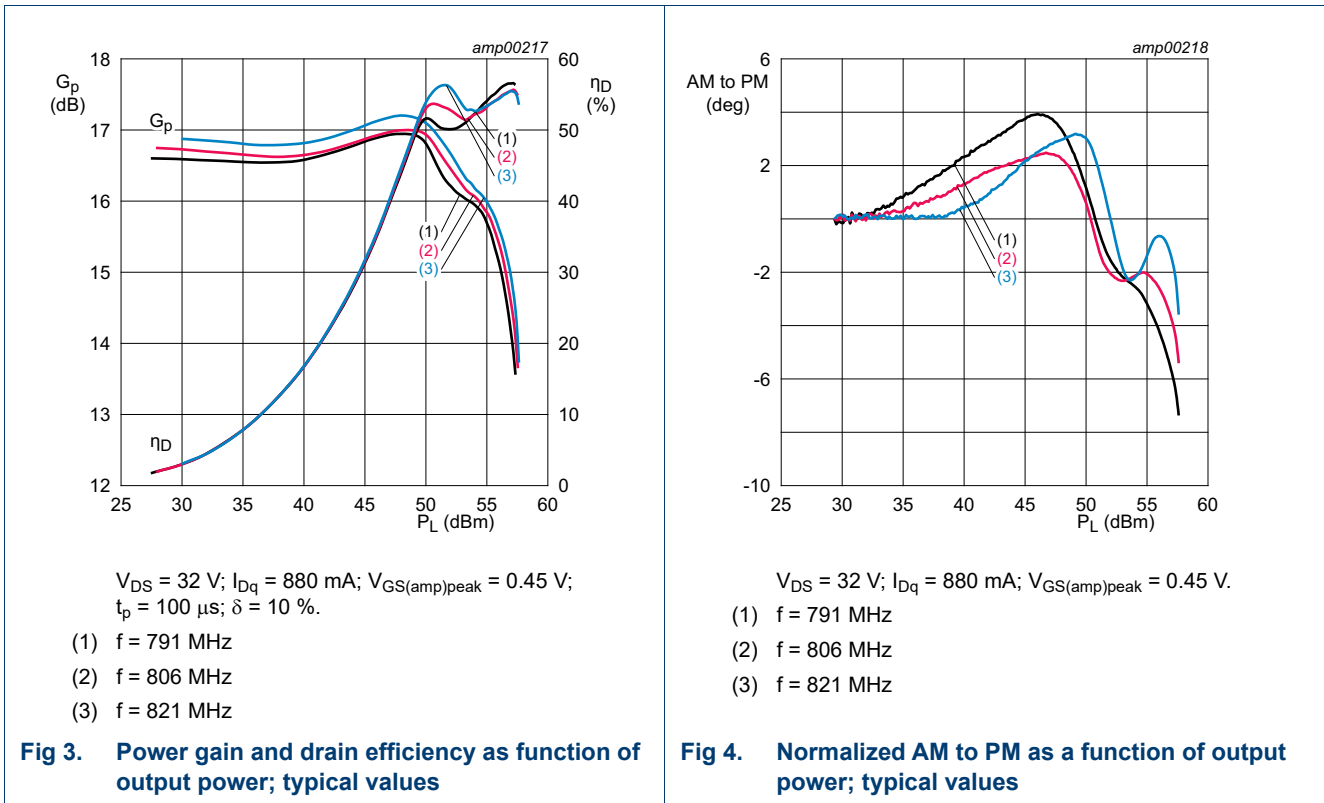
Table 15. List of components

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C2	electrolytic capacitor	470 μF , 63 V	
C5, C14, C20, C21, C24, C25, C36, C37, C42, C43	multilayer ceramic chip capacitor	4.7 μF , 50 V	SMD 1210, Murata, GRM32ER71H475KA88L
C6, C15, C27, C41	multilayer ceramic chip capacitor	100 nF, 50 V	SMD 0805, Murata
C7, C8, C12, C16, C23, C26, C27, C34, C40	multilayer ceramic chip capacitor	82pF	SMD 0805, Murata Hi-Q
C9, C11, C32	multilayer ceramic chip capacitor	6.8 pF	SMD 0805, Murata Hi-Q
C10, C32	multilayer ceramic chip capacitor	5.1 pF	SMD 0805, Murata Hi-Q
C28	multilayer ceramic chip capacitor	5.6 pF	SMD 0805, Murata Hi-Q
C29, C30	multilayer ceramic chip capacitor	100 pF	SMD 0805, Murata Hi-Q
C31	multilayer ceramic chip capacitor	4.3 pF	SMD 0805, Murata Hi-Q
C33	multilayer ceramic chip capacitor	12 pF	SMD 0805, Murata Hi-Q
C38, C39	multilayer ceramic chip capacitor	68 pF	SMD 0805, Murata Hi-Q
R10, R12	resistor	2.0 Ω , 1 %	SMD 0805
R11	resistor	50 Ω , 25 W	Anaren, C16A50Z4
X1	hybrid coupler	2 dB	Anaren Xinger III, X3C20F1-02S

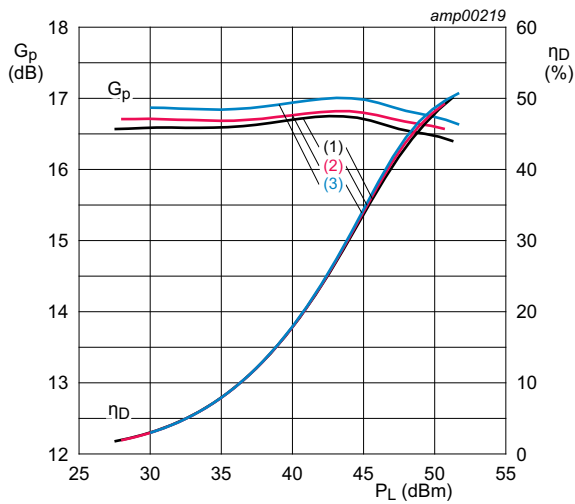
7.5 Graphical data

7.5.1 Pulsed CW



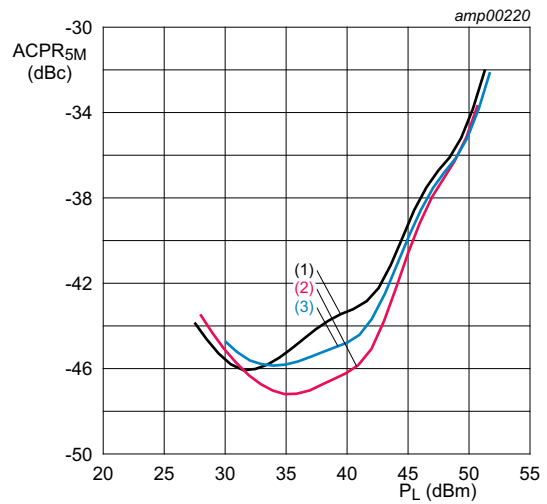
7.5.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



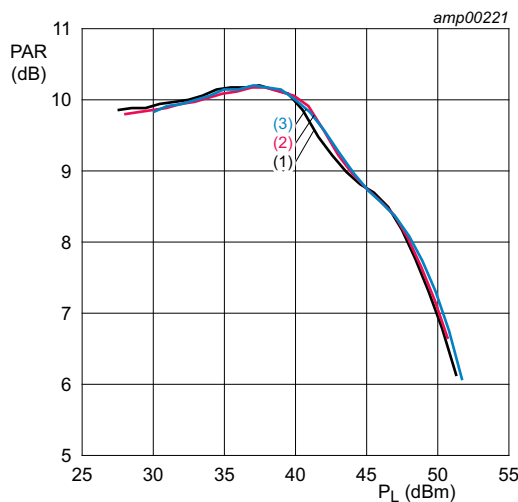
$V_{DS} = 32\text{ V}; I_{Dq} = 880\text{ mA}; V_{GS(amp)peak} = 0.45\text{ V}.$
 (1) $f = 791\text{ MHz}$
 (2) $f = 806\text{ MHz}$
 (3) $f = 821\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 880\text{ mA}; V_{GS(amp)peak} = 0.45\text{ V}.$
 (1) $f = 791\text{ MHz}$
 (2) $f = 806\text{ MHz}$
 (3) $f = 821\text{ MHz}$

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

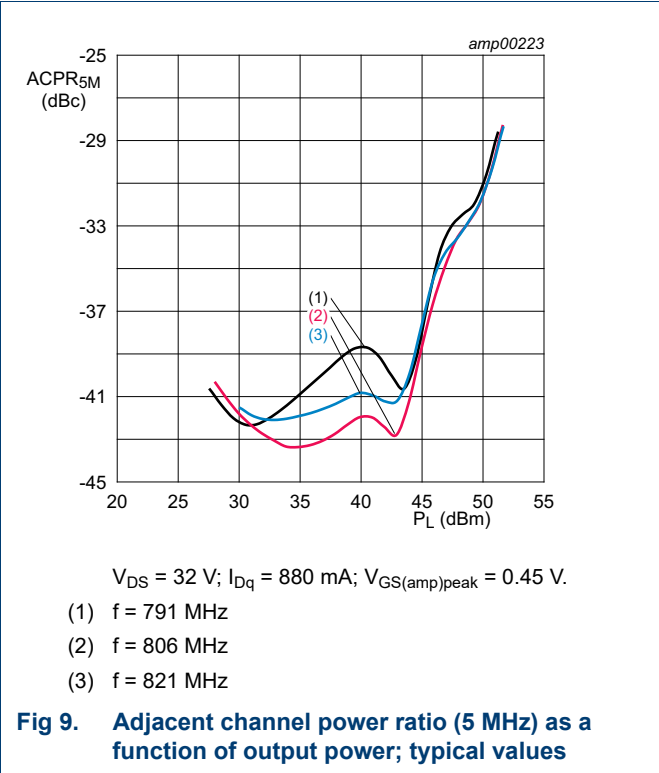
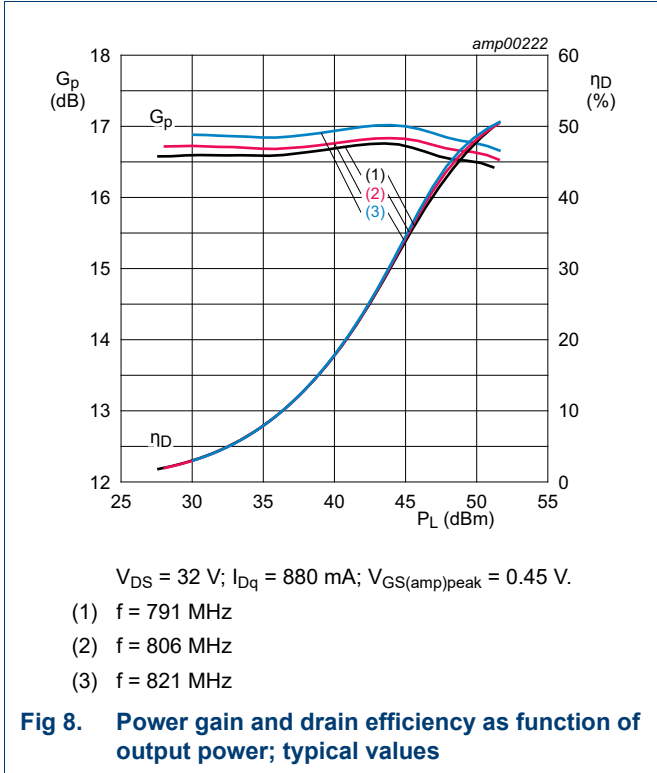


$V_{DS} = 32\text{ V}; I_{Dq} = 880\text{ mA}; V_{GS(amp)peak} = 0.45\text{ V}.$
 (1) $f = 791\text{ MHz}$
 (2) $f = 806\text{ MHz}$
 (3) $f = 821\text{ MHz}$

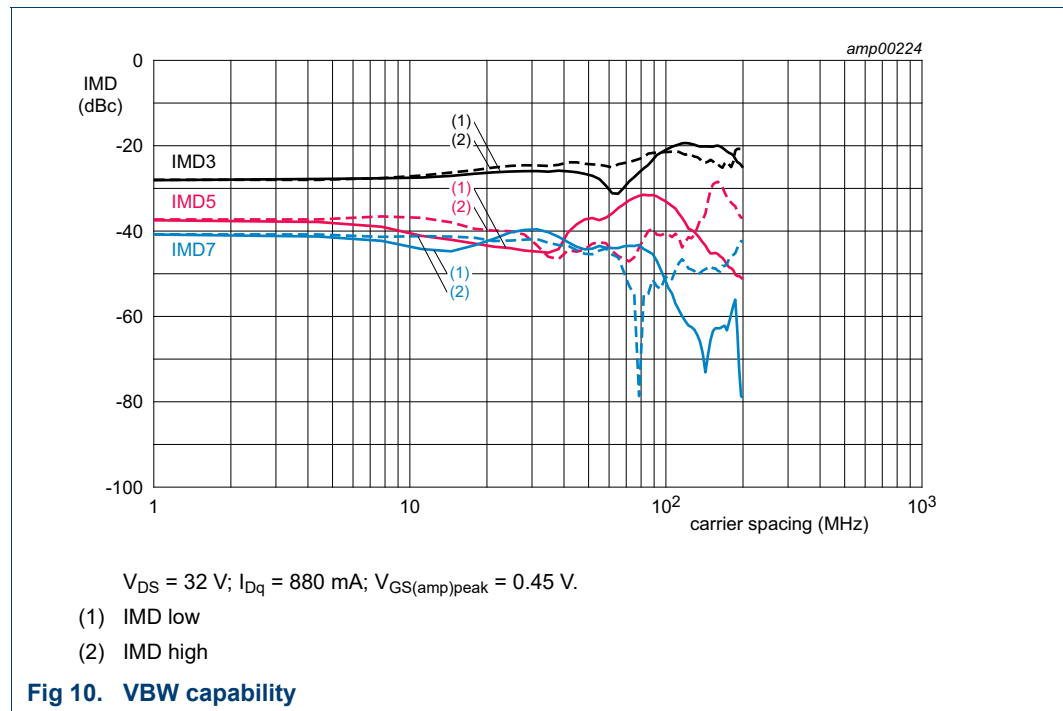
Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.5.3 2-Carrier W-CDMA

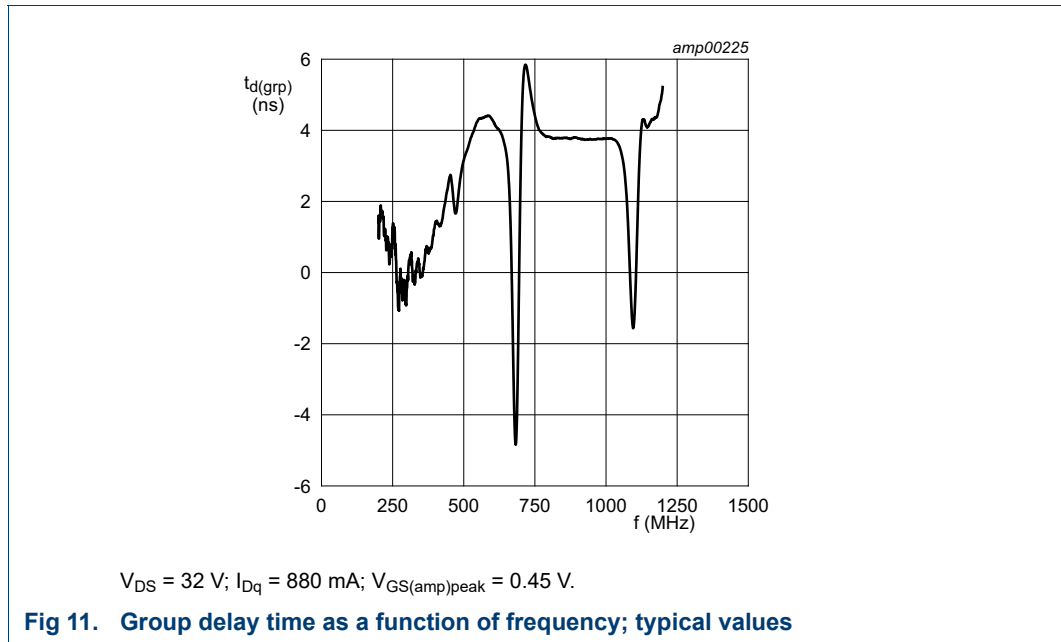
Test signal: 3GPP test model 1; 1 to 64 DPCH (46 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



7.5.4 2-Tone VBW



7.5.5 Group delay



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-4

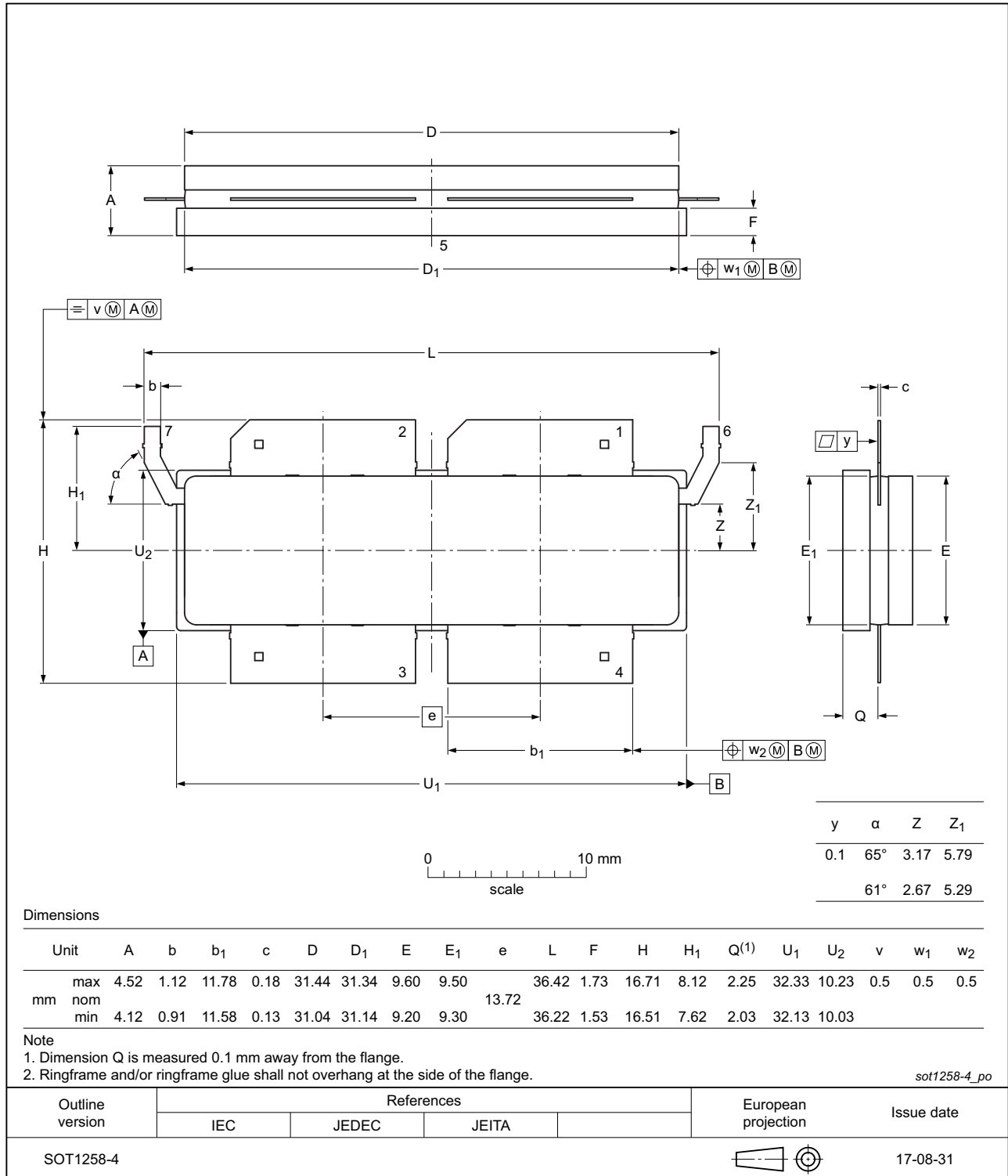


Fig 12. Package outline SOT1258-4

9. Handling information


CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

- [1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC8G09XS-400AVT v.2	20171124	Product data sheet	-	BLC8G09XS-400AVT v.1
Modifications:	<ul style="list-style-type: none">• Table 2 on page 2: changed simplified version drawing SOT1258-7 to SOT1258-4• Table 3 on page 2: changed version SOT1258-7 to SOT1258-4• Figure 2 on page 7: updated figure• Figure 12 on page 12: changed package outline drawing SOT1258-7 to SOT1258-4			
BLC8G09XS-400AVT v.1	20170421	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

12.2 Definitions

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