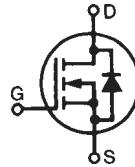


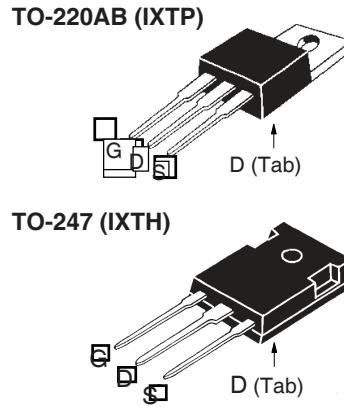
TrenchT4™
Power MOSFET
IXTP340N04T4
IXTH340N04T4
 $V_{DSS} = 40V$
 $I_{D25} = 340A$
 $R_{DS(on)} \leq 1.9m\Omega$

N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Rectifier



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $175^\circ C$	40	V
V_{DGR}	$T_J = 25^\circ C$ to $175^\circ C$, $R_{GS} = 1M\Omega$	40	V
V_{GSM}	Transient	± 15	V
I_{D25}	$T_c = 25^\circ C$	340	A
I_{LRMS}	Lead Current Limit, RMS	160	A
I_{DM}	$T_c = 25^\circ C$, Pulse Width Limited by T_{JM}	700	A
I_A	$T_c = 25^\circ C$	170	A
E_{AS}	$T_c = 25^\circ C$	1.2	J
I_A	$T_c = 25^\circ C$	340	A
E_{AS}	$T_c = 25^\circ C$	500	mJ
P_D	$T_c = 25^\circ C$	480	W
T_J		-55 ... +175	$^\circ C$
T_{JM}		175	$^\circ C$
T_{stg}		-55 ... +175	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
M_d	Mounting Torque	1.13 / 10	m/lb.in
Weight	TO-220	3	g
	TO-247	6	g

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	40		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.0		V
I_{GSS}	$V_{GS} = \pm 15V$, $V_{DS} = 0V$		± 200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 150^\circ C$		5	μA
			750	μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 100A$, Notes 1, 2		1.9	$m\Omega$



G = Gate D = Drain
 S = Source Tab = Drain

Features

- International Standard Packages
- $175^\circ C$ Operating Temperature
- High Current Handling Capability
- Avalanche Rated
- Fast Intrinsic Rectifier
- Low $R_{DS(on)}$

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC-DC Converters & Off-Line UPS
- Primary-Side Switch
- High Current Switching Applications

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 60\text{A}$, Note 1	110	180	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$	13	nF	
C_{oss}		1850	pF	
C_{rss}		1226	pF	
R_{GI}	Gate Input Resistance	1.1	Ω	
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 3\Omega$ (External)	23	ns	
t_r		55	ns	
$t_{d(off)}$		113	ns	
t_f		40	ns	
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$	256	nC	
Q_{gs}		64	nC	
Q_{gd}		86	nC	
R_{thJC}	TO-220	0.50	$^\circ\text{C}/\text{W}$	
R_{thCS}	TO-247	0.21	$^\circ\text{C}/\text{W}$	

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$		340	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}		1360	A
V_{SD}	$I_F = 100\text{A}$, $V_{GS} = 0\text{V}$, Note 1		1.4	V
t_{rr}	$I_F = 150\text{A}$, $V_{GS} = 0\text{V}$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 30\text{V}$	43	ns	
I_{RM}		10	A	
Q_{RM}		210	nC	

Notes: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

2. On through-hole packages, $R_{DS(on)}$ Kelvin test contact location must be 5mm or less from the package body.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

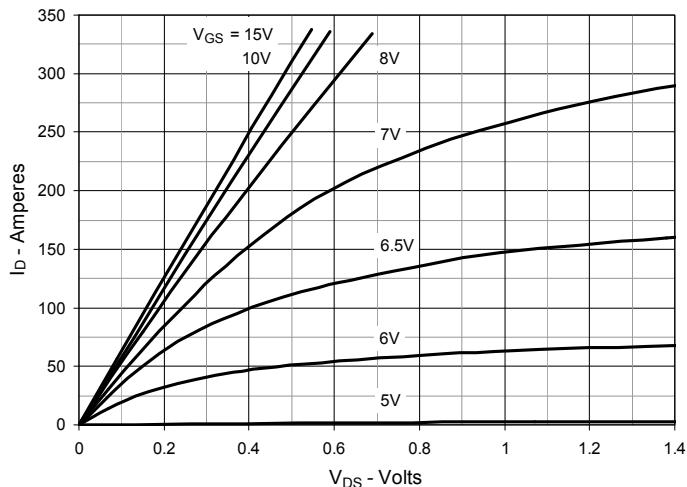
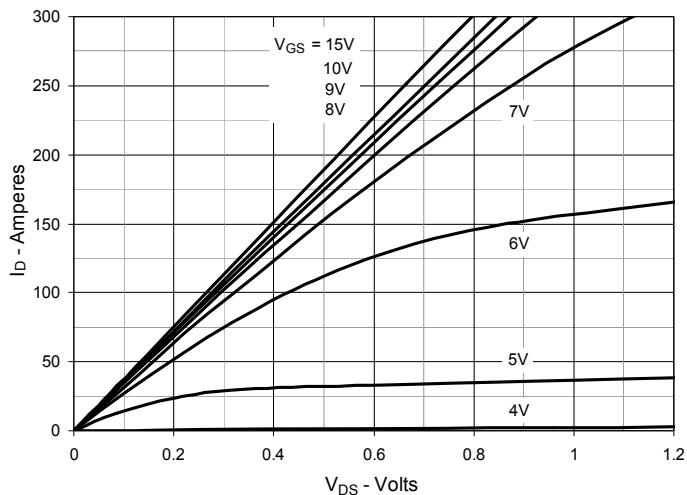
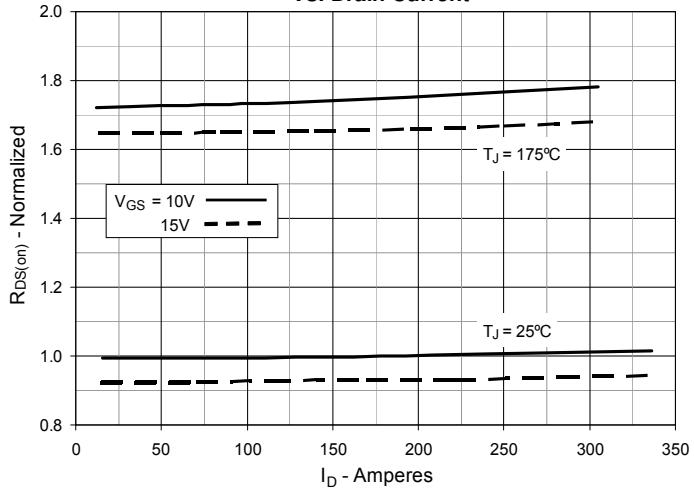
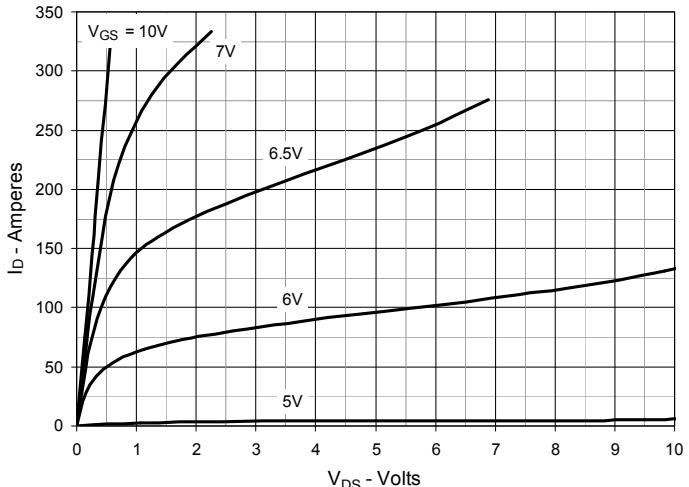
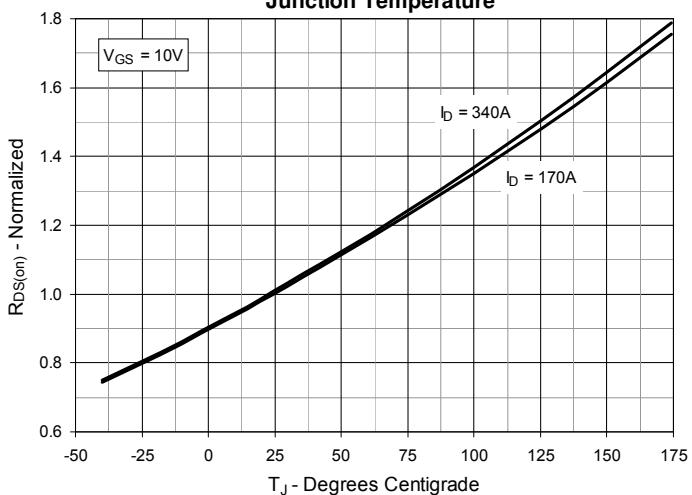
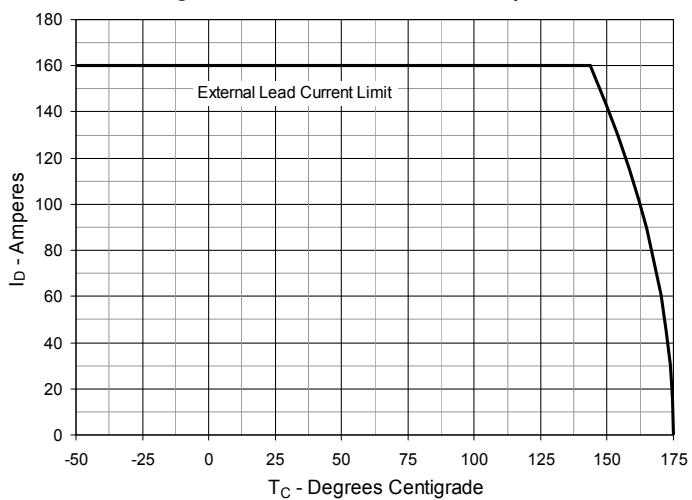
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 150^\circ\text{C}$

Fig. 5. Normalized $R_{DS(on)}$ to $I_D = 170\text{A}$ vs. Drain Current

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 4. Normalized $R_{DS(on)}$ to $I_D = 170\text{A}$ Value vs. Junction Temperature

Fig. 6. Drain Current vs. Case Temperature


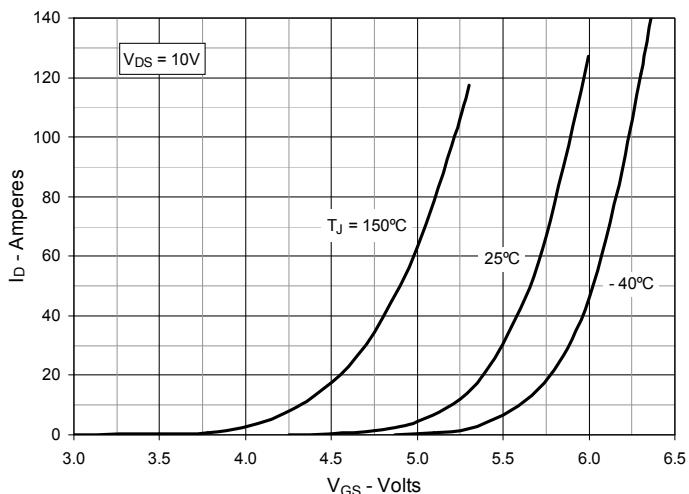
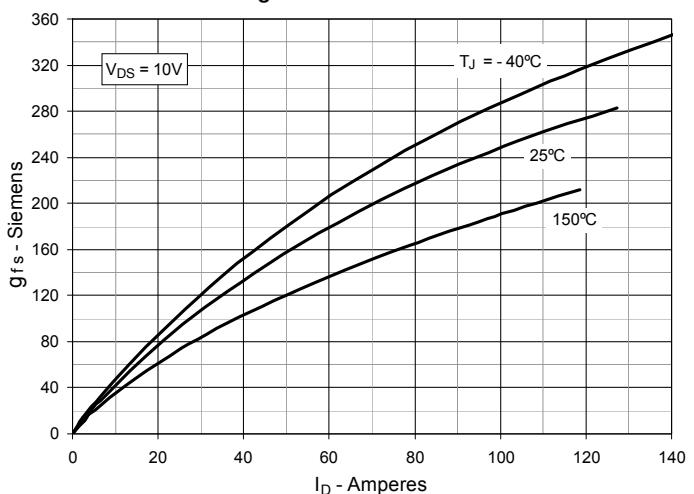
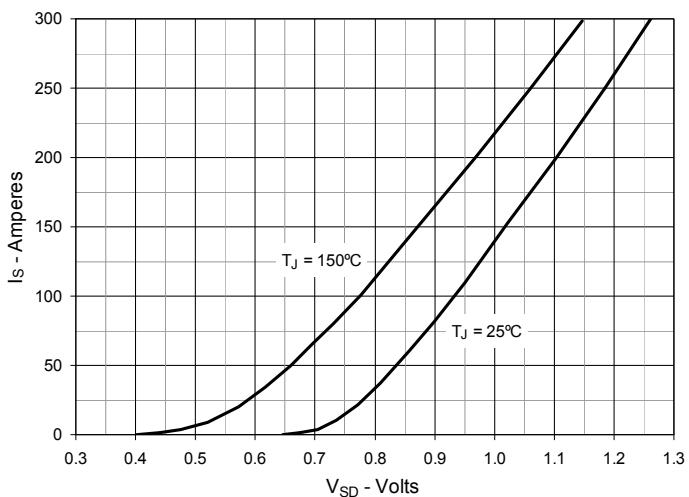
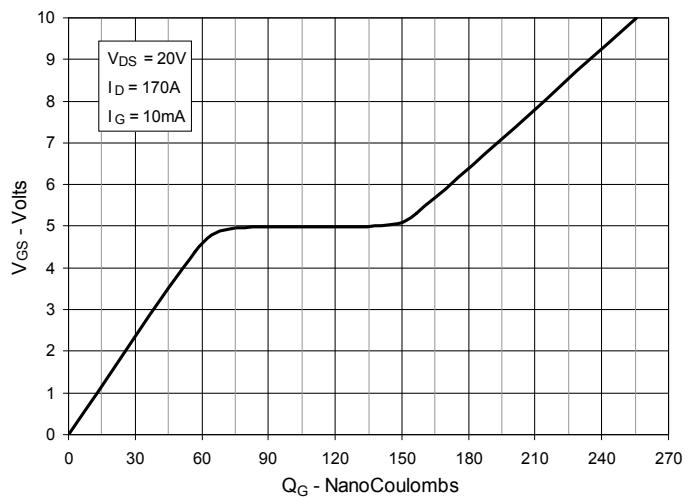
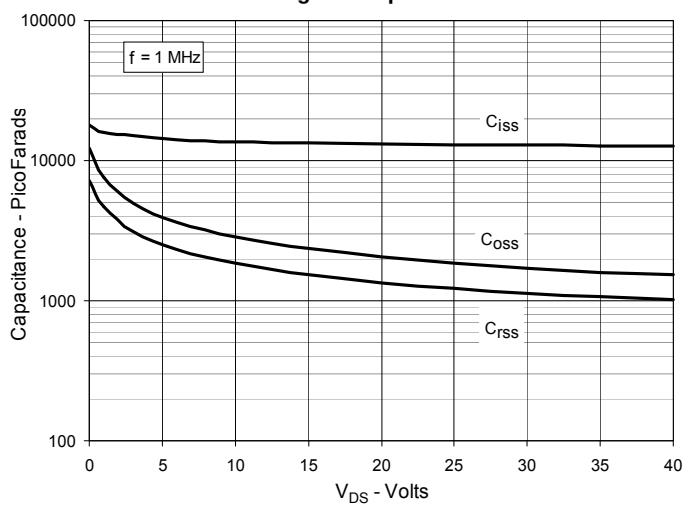
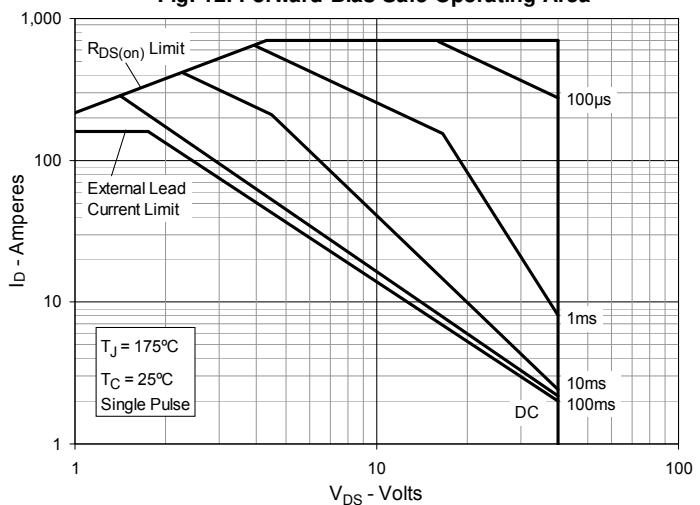
Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

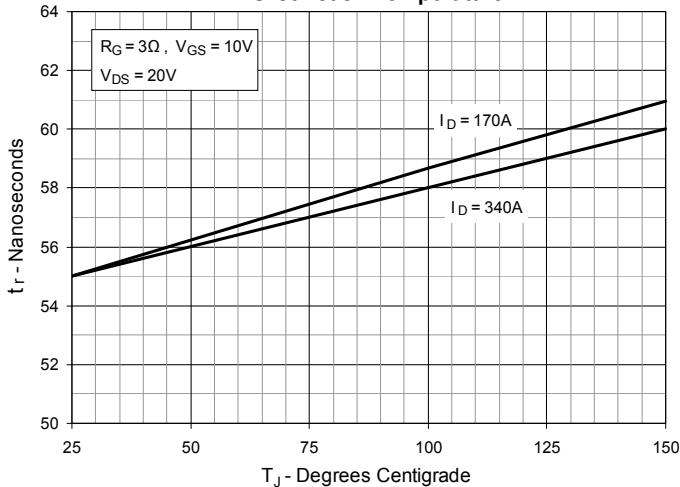


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

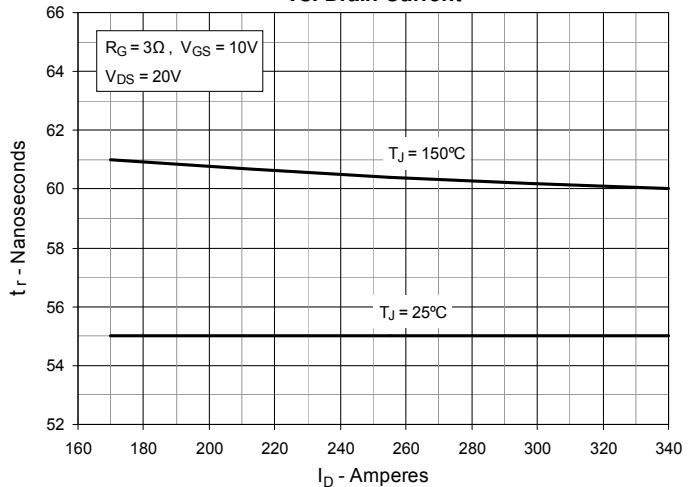


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

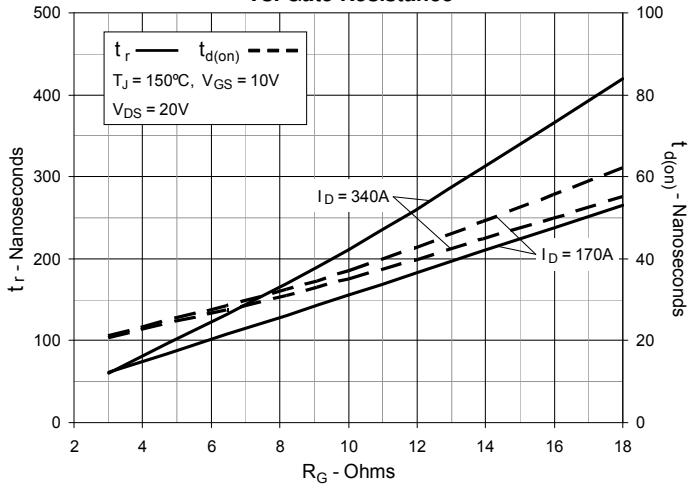


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

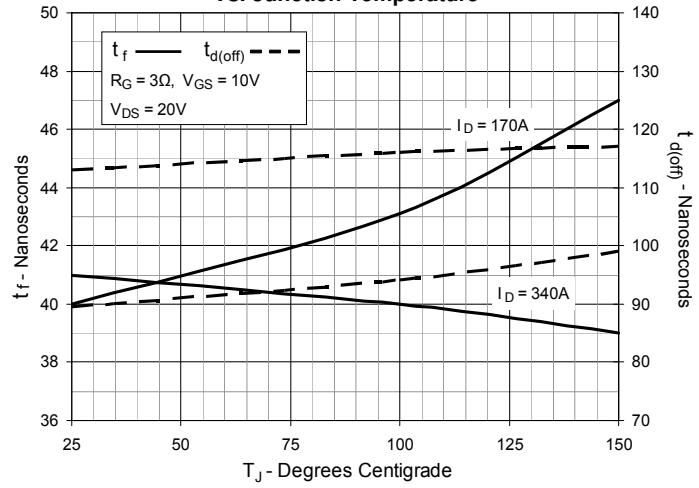


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

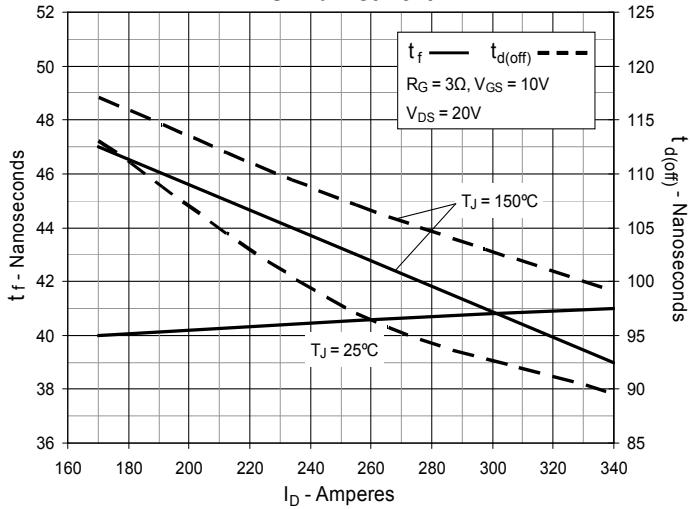


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

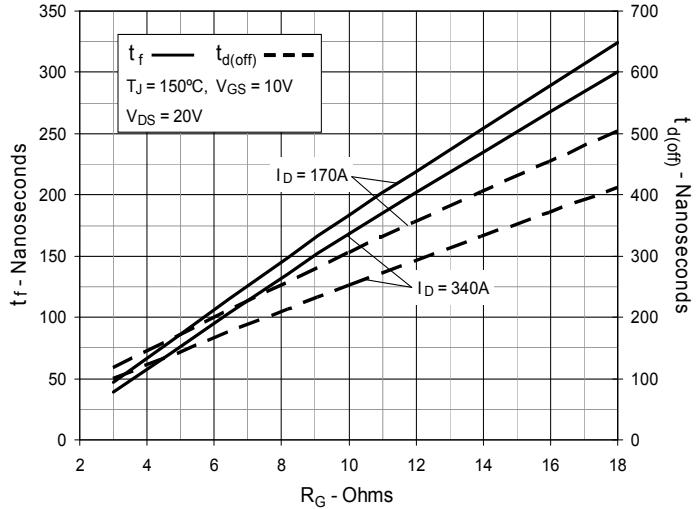
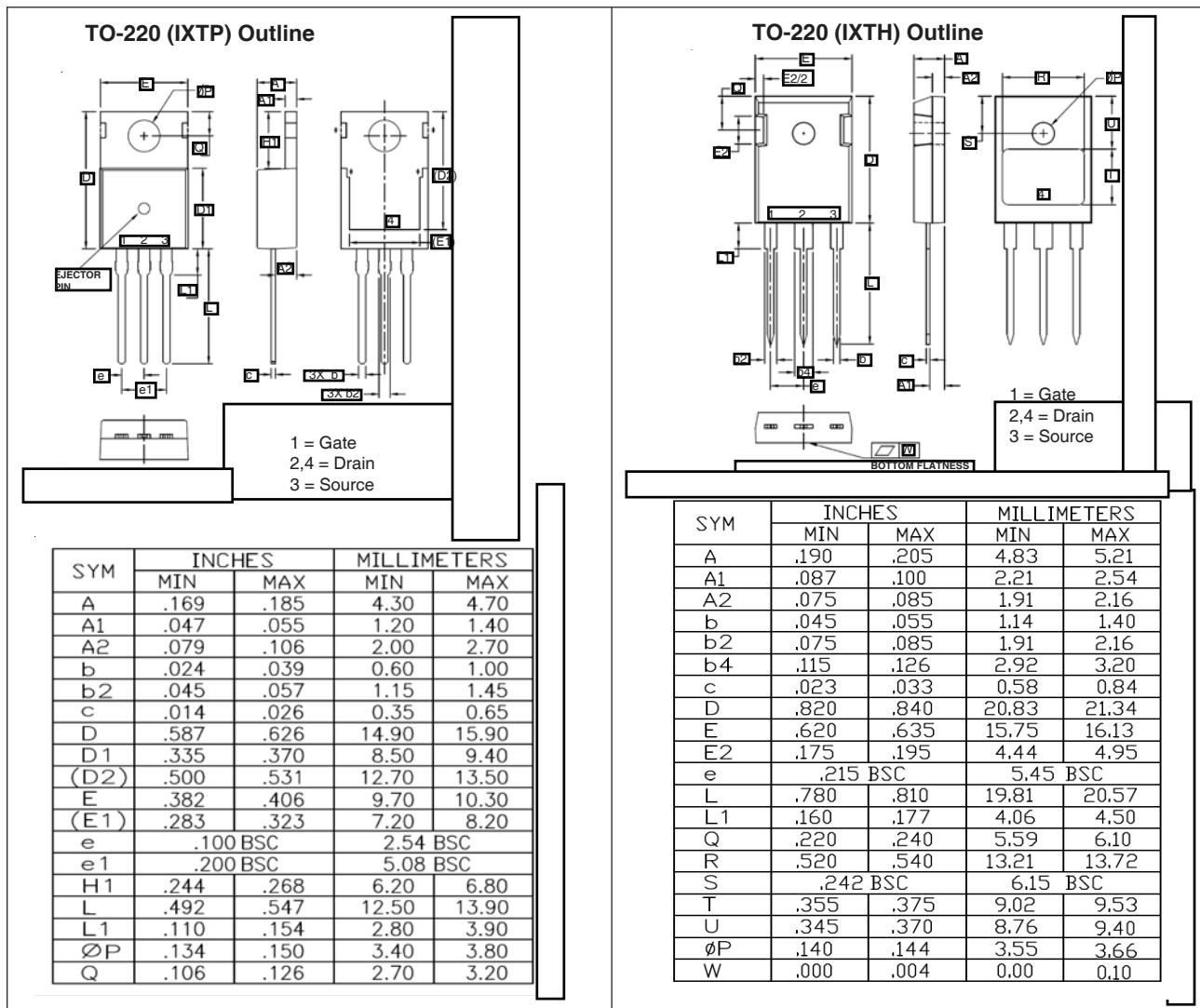
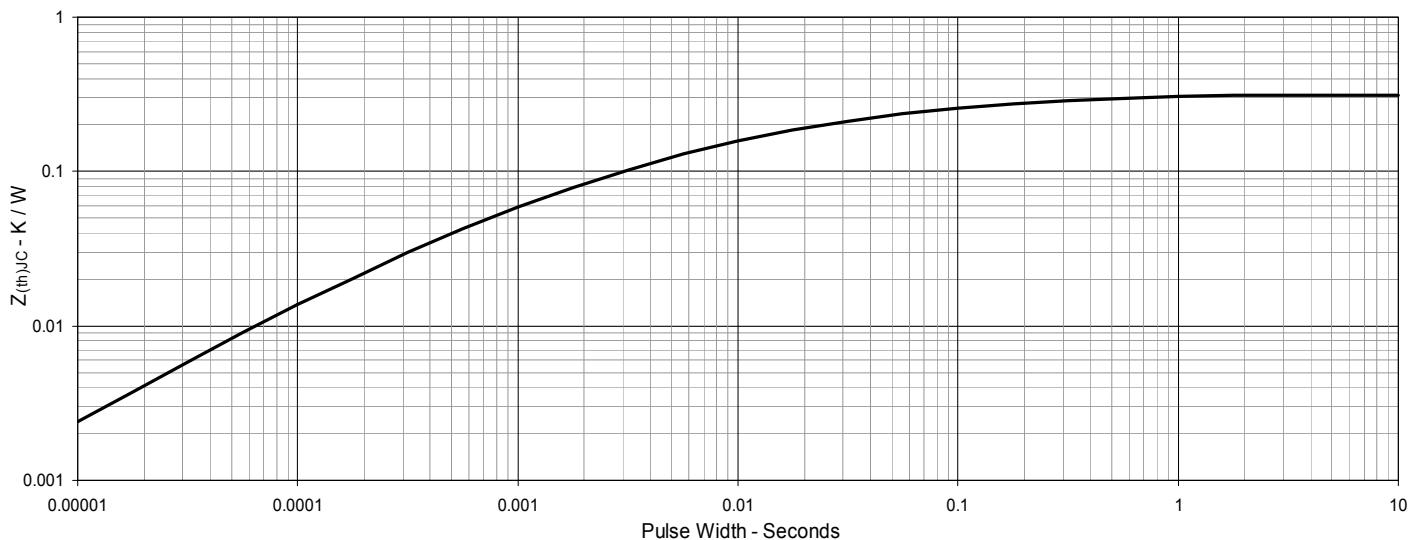


Fig. 19. Maximum Transient Thermal Impedance



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