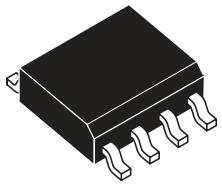
LCP1511D

Application Specific Discretes
A.S.D.™

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

FEATURES

- DUAL PROGRAMMABLE TRANSIENT SUPPRESSOR.
- WIDE NEGATIVE FIRING VOLTAGE RANGE : V_{MGL} = -80V max.
- LOW DYNAMIC SWITCHING VOLTAGES : V_{FP} and V_{DGL}.
- LOW GATE TRIGGERING CURRENT : I_{GT} = 5mA max.
- PEAK PULSE CURRENT : I_{PP} = 30A for 10/1000µs surge.
- HOLDING CURRENT : I_H = 150mA.

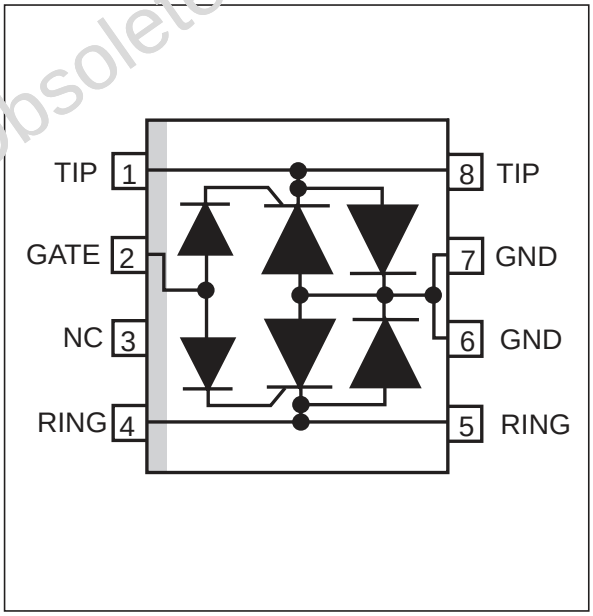


SO-8

DESCRIPTION

This device has been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.
Positive overloads are clipped with 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.
This component presents a very low gate trigge-ring current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase.
A particular attention has been given to the internal wire bonding. The “4-point” configuration ensures reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt), especially for very fast transients.

SCHEMATIC DIAGRAM



COMPLIES WITH THE FOLLOWING STANDARDS

CCITT K20 :	10/700µs 5/310µs	1kV 25A
VDE 0433 :	10/700µs 5/310µs	2kV 38A (*)
VDE 0878 :	1.2/50µs 1/20µs	1.5kV 40A
I3124 :	0.5/700µs 0.2/310µs	1kV 25A
FCC part 68 :	2/10µs 2/10µs	2.5kV 170A (*)
BELLCORE TR-NWT-001089 :	2/10µs 2/10µs	2.5kV 170A (*)

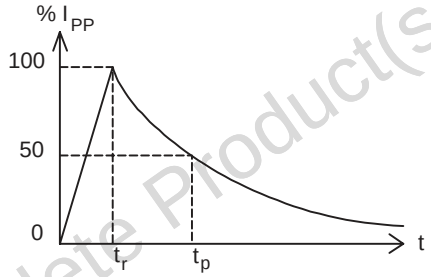
(*) with series resistors or PTC.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current (see note 1)	10/1000µs 5/310µs 2/10µs	30 38 170	A
I_{TSM}	Non repetitive surge peak on-state current (F = 50Hz)	t_p = 10ms t = 1s	8 3.5	A
I_{GSM}	Maximum gate current (half sine wave tp = 10ms)		2	A
V_{MLG} V_{MGL}	Maximum voltage LINE / GROUND Maximum voltage GATE / LINE		-100 -80	V
T_{stg} T_j	Storage temperature range Maximum junction temperature		- 55 to + 150 150	°C
T_L	Maximum lead temperature for soldering during 10s		260	°C

Note 1 : Pulse waveform :

10/1000µs	t_r=10µs	t_p=1000µs
5/310µs	t_r=5µs	t_p=310µs
2/10µs	t_r=2µs	t_p=10µs

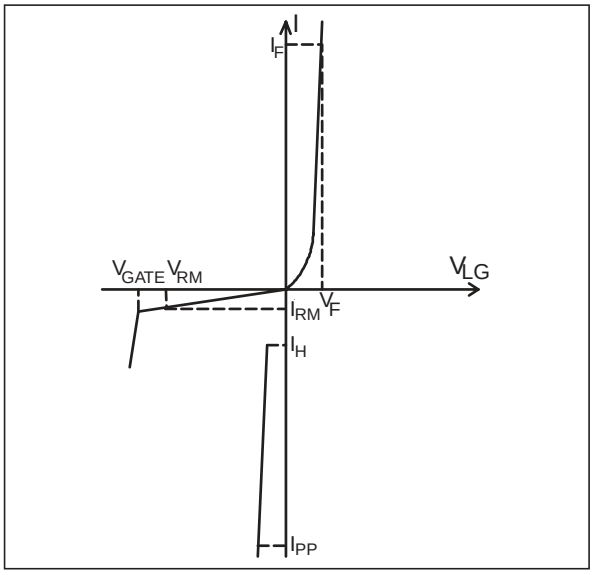


THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction to ambient	170	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RM}	Reverse leakage current LINE/GND
I_{RG}	Reverse leakage current GATE/LINE
V_{RM}	Reverse voltage LINE/GND
V_F	Forward drop voltage LINE/GND
V_{GT}	Gate triggering voltage
V_{FP}	Peak forward voltage LINE/GND
V_{DGL}	Dynamic switching voltage GATE/LINE
V_{GATE}	GATE/GND voltage
V_{LG}	LINE/GND voltage
C	Off-state capacitance LINE/GND



1 - PARAMETERS RELATED TO THE DIODE LINE/GND (T_{amb} = 25 °C)

Symbol	Test conditions	Maximum	Unit
V_F	I_F=5A t_p=500µs	3	V
V_{FP}	10/700µs 1.5kV R_p=10Ω 1.2/50µs 1.5kV R_p=10Ω (see note 1) 2/10µs 2.5kV R_p=62Ω	5 7 12	V

Note 1 : See test circuit 2 for V_{FP}; R_p is the protection resistor located on the line card.

2 - PARAMETERS RELATED TO THE PROTECTION THYRISTOR (T_{amb} = 25°C)

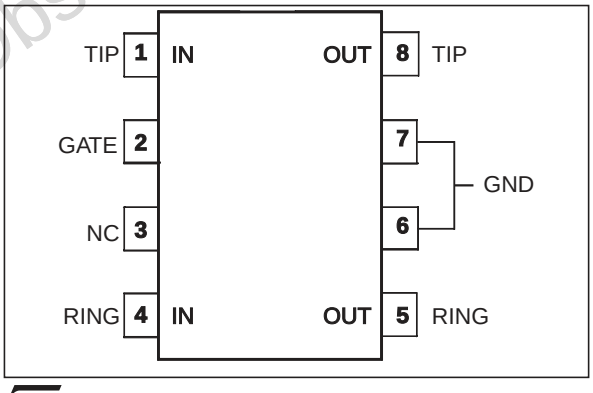
Sym-bol	Test conditions	Min.	Max.	Unit
I_{GT}	$V_{GND/LINE}$ = -48V	0.2	5	mA
I_H	V_{GATE} =-48V (see note 2)	150		mA
V_{GT}	at I_{GT}		2.5	V
I_{RG}	T_c=25°C V_{RG} =-75V T_c=70°C V_{RG} =-75V		5 50	µA
V_{DGL}	VGATE= -48V (see note 3) 10/700µs 1.5kV Rp=10Ω I_{PP}=30A 1.2/50µs 1.5kV Rp=10Ω I_{PP}=30A 2/10µs 2.5kV Rp=62Ω I_{PP}=38A		 10 20 25	V

Note 2 : See the functional holding current (I_H) test circuit 2.

3 - PARAMETERS RELATED TO DIODE AND PROTECTION THYRISTOR (T_{amb} = 25 °C)

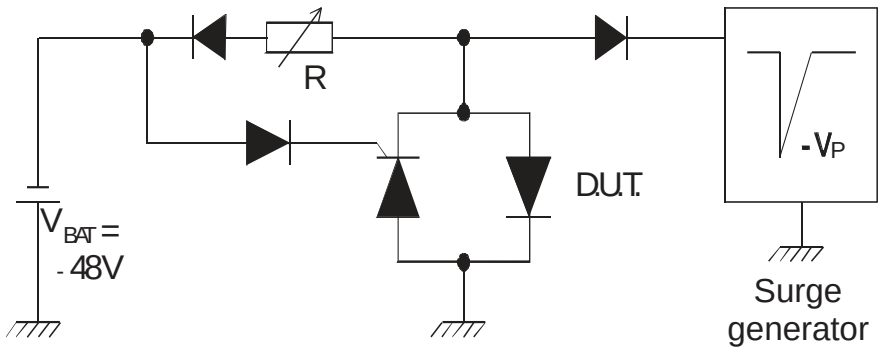
Sym-bol	Test conditions	Maximum	Unit
I_{RM}	T_c=25°C $V_{GATE/LINE}$ = -1V V_{RM} =-75V T_c=70°C $V_{GATE/LINE}$ = -1V V_{RM} =-75V	5 50	µA

APPLICATION NOTE



In order to take advantage of the “4 point” structure of the LCP, the TIP and RING lines go across the device. In such case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast transients.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT 1 : GO-NO GO TEST

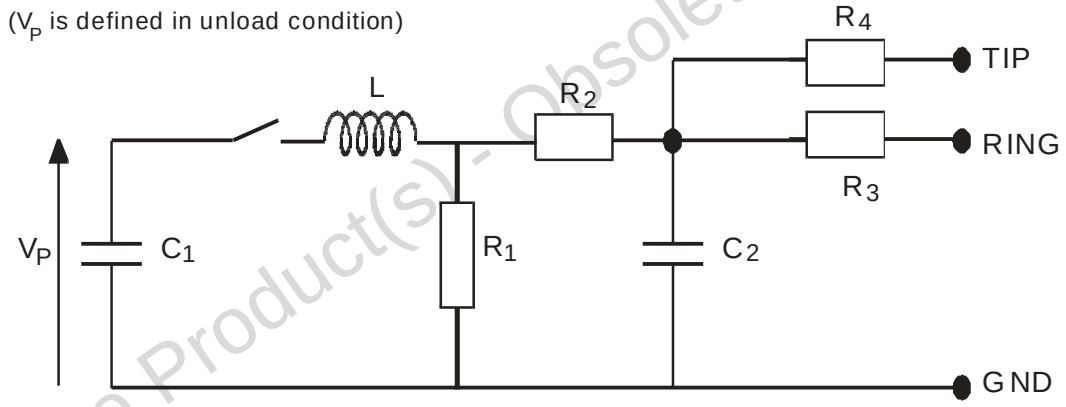


This is a GO-NO GO test which allows to confirm the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE :

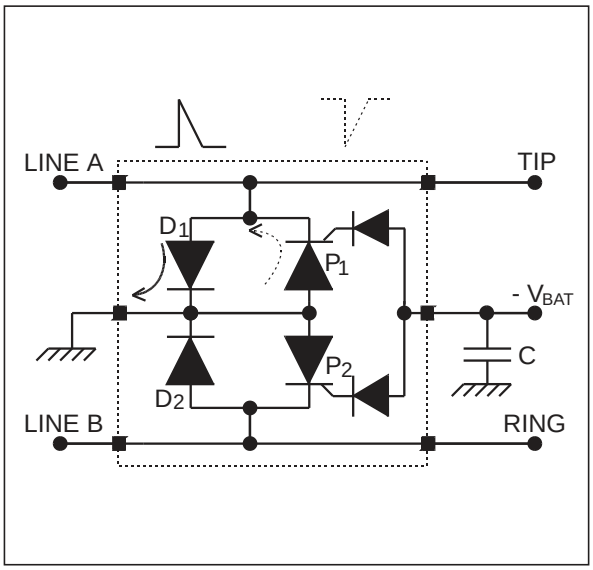
- Adjust the current level at the I_H value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current : I_{PP} = 10A, 10/1000µs.
- The D.U.T. will come back to the off-state within a duration of 50ms max.

TEST CIRCUIT 2 FOR V_{FP} AND V_{DGL} PARAMETERS



Pulse (µs)		V_p	C_1	C_2	L	R_1	R_2	R_3	R_4	I_{PP}	R_p
t_r	t_p	(V)	(µF)	(nF)	(µH)	(Ω)	(Ω)	(Ω)	(Ω)	(A)	(Ω)
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

FUNCTIONAL DESCRIPTION



LINE A PROTECTION :

– For positive surges versus GND, the diode D1 will conduct.

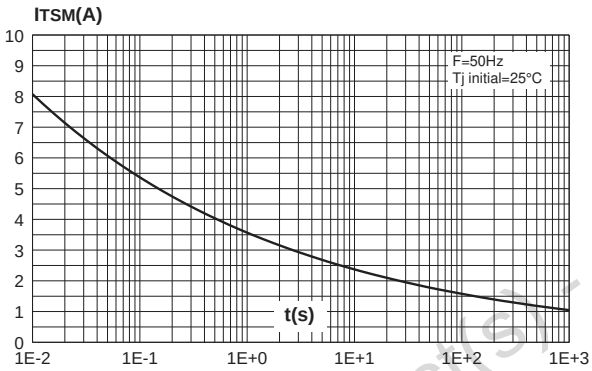
– For negative surges versus GND, the protection device P1 will trigger at a voltage fixed by the $-V_{BAT}$ reference.

LINE B PROTECTION :

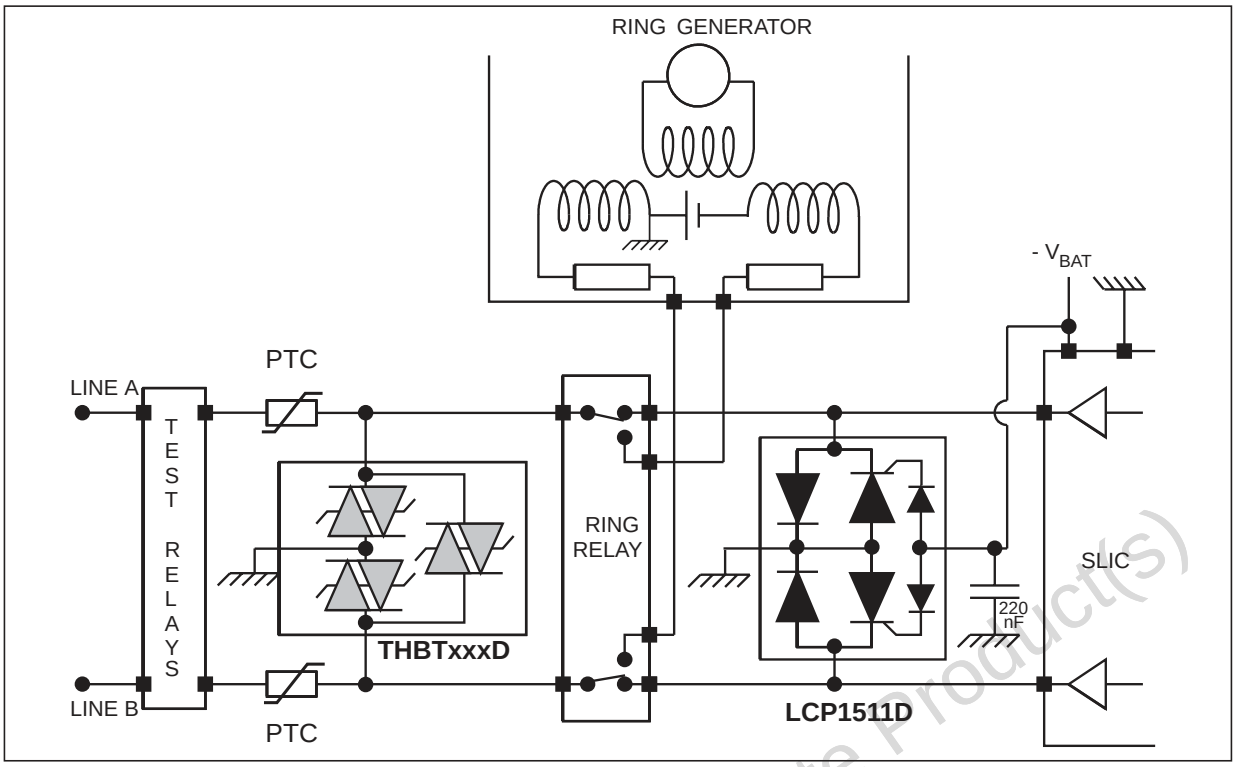
– For surges on line B, the operating mode is the same, D2 or P2 is activated.

It is recommended to add a capacitor (C=220nF) close to the gate of the LCP, in order to speed up the triggering.

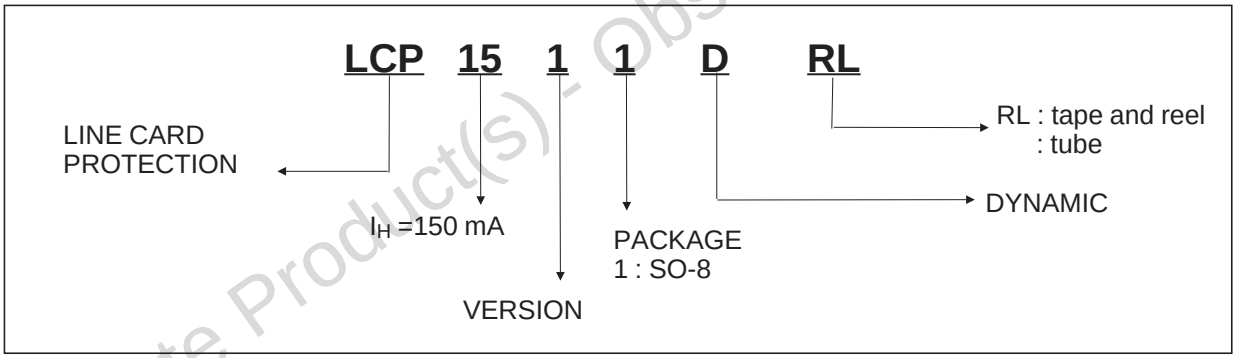
Surge peak current versus overload duration.



APPLICATION CIRCUIT : typical SLIC protection concept



ORDER CODE

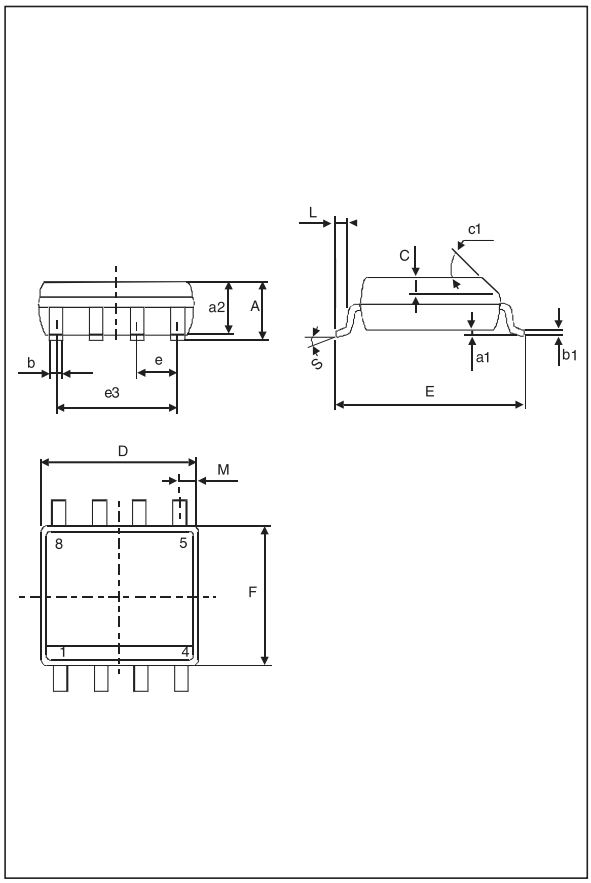


MARKING

Package	Type	Marking
SO-8	LCP1511D	CP151D

PACKAGE MECHANICAL DATA

SO-8 Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C		0.50			0.020	
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

Weight = 0.08 g.

Packaging : Product supplied in antistatic tubes or tape and reel .