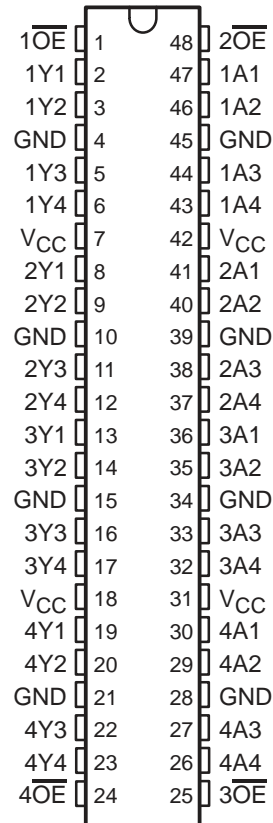


SN54AHC16240, SN74AHC16240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS326G – MARCH 1996 – REVISED JANUARY 2000

- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16240 . . . WD PACKAGE
SN74AHC16240 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16240 devices are 16-bit buffers and line drivers designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. They provide inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC16240 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z



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 **TEXAS
INSTRUMENTS**

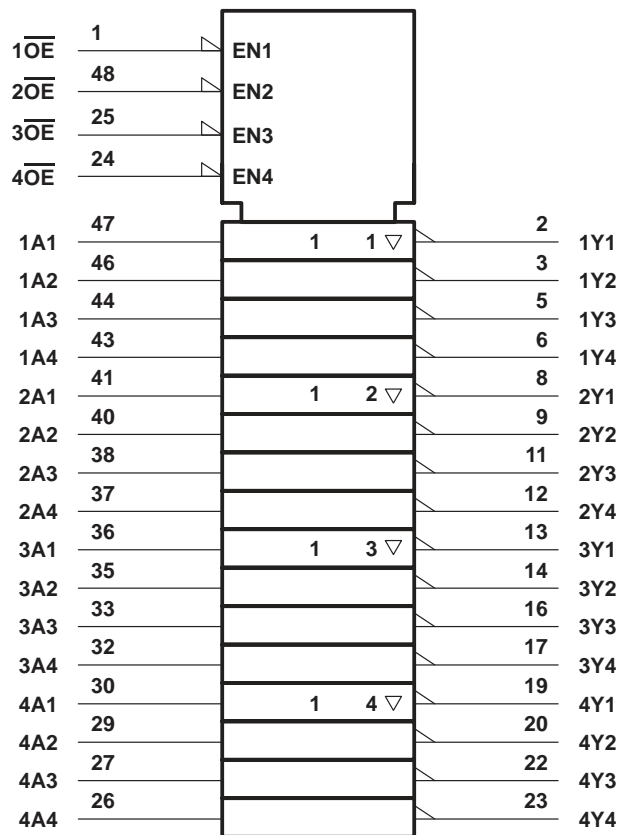
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SN54AHC16240, SN74AHC16240
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

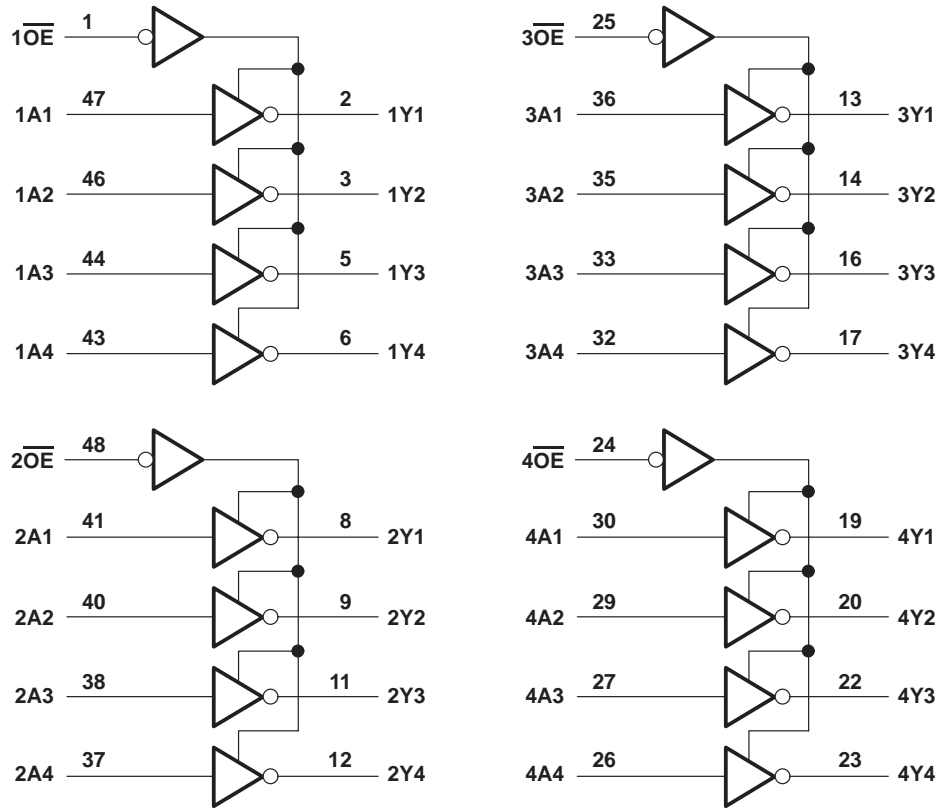
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through each V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN54AHC16240, SN74AHC16240

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCLS326G – MARCH 1996 – REVISED JANUARY 2000

recommended operating conditions (see Note 3)

		SN54AHC16240		SN74AHC16240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5		V
		$V_{CC} = 3\text{ V}$		2.1		
		$V_{CC} = 5.5\text{ V}$		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5		V
		$V_{CC} = 3\text{ V}$		0.9		
		$V_{CC} = 5.5\text{ V}$		1.65		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50		μA
		$V_{CC} = 3.3 \pm 0.3\text{ V}$		-4		
		$V_{CC} = 5 \pm 0.5\text{ V}$		-8		
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50		μA
		$V_{CC} = 3.3 \pm 0.3\text{ V}$		4		
		$V_{CC} = 5 \pm 0.5\text{ V}$		8		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \pm 0.3\text{ V}$		100		ns/V
		$V_{CC} = 5 \pm 0.5\text{ V}$		20		
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^{\circ}\text{C}$			SN54AHC16240		SN74AHC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	2 V	1.9	2	1.9	1.9	V			
		3 V	2.9	3	2.9	2.9				
		4.5 V	4.4	4.5	4.4	4.4				
	$I_{OH} = -4\ \text{mA}$	3 V	2.58		2.48	2.48				
		4.5 V	3.94		3.8	3.8				
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	2 V		0.1	0.1	0.1	V			
		3 V		0.1	0.1	0.1				
		4.5 V		0.1	0.1	0.1				
	$I_{OL} = 4\ \text{mA}$	3 V		0.36	0.5	0.44				
		4.5 V		0.36	0.5	0.44				
I_I	$V_I = V_{CC}$ or GND	0 V to 5.5 V		± 0.1	$\pm 1^*$	± 1	μA			
I_{OZ}	$V_O = V_{CC}$ or GND, $V_I (\text{OE}) = V_{IL}$ or V_{IH}	5.5 V		± 0.25	± 2.5	± 2.5	μA			
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4	40	40	μA			
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10		10	pF		
C_o	$V_O = V_{CC}$ or GND	5 V		3.5				pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0\text{ V}$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54AHC16240, SN74AHC16240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS326G – MARCH 1996 – REVISED JANUARY 2000

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF	5.3*	8.4*		1*	10*	1	10	ns
t _{PHL}				5.3*	8.4*	1*	10*	1	10		
t _{PZH}	\overline{OE}	Y	C _L = 15 pF	6.6*	10.6*		1*	12.5*	1	12.5	ns
t _{PZL}				6.6*	10.6*	1*	12.5*	1	12.5		
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF	7.8*	11.5*		1*	12.5*	1	12.5	ns
t _{PLZ}				7.8*	11.5*	1*	12.5*	1	12.5		
t _{PLH}	A	Y	C _L = 50 pF	7.8	11.9*		1	13.5	1	13.5	ns
t _{PHL}				7.8	11.9	1	13.5	1	13.5		
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	9.1	14.1		1	16	1	16	ns
t _{PZL}				9.1	14.1	1	16	1	16		
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	10.3	14		1	16	1	16	ns
t _{PLZ}				10.3	14	1	16	1	16		
t _{sk(o)}			C _L = 50 pF			1.5**				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF	3.6*	6*		1*	7*	1	6.5	ns
t _{PHL}				3.6*	6*	1*	7*	1	6.5		
t _{PZH}	\overline{OE}	Y	C _L = 15 pF	4.7*	7.3*		1*	8.5*	1	8.5	ns
t _{PZL}				4.7*	7.3*	1*	8.5*	1	8.5		
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF	5.2*	7.2*		1*	8.5*	1	8.5	ns
t _{PLZ}				5.2*	7.2*	1*	8.5*	1	8.5		
t _{PLH}	A	Y	C _L = 50 pF	5.1	8		1	9	1	8.5	ns
t _{PHL}				5.1	8	1	9	1	8.5		
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	6.2	9.3		1	10.5	1	10.5	ns
t _{PZL}				6.2	9.3	1	10.5	1	10.5		
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	6.7	9.2		1	10.5	1	10.5	ns
t _{PLZ}				6.7	9.2	1	10.5	1	10.5		
t _{sk(o)}			C _L = 50 pF			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

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SN54AHC16240, SN74AHC16240
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC16240			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

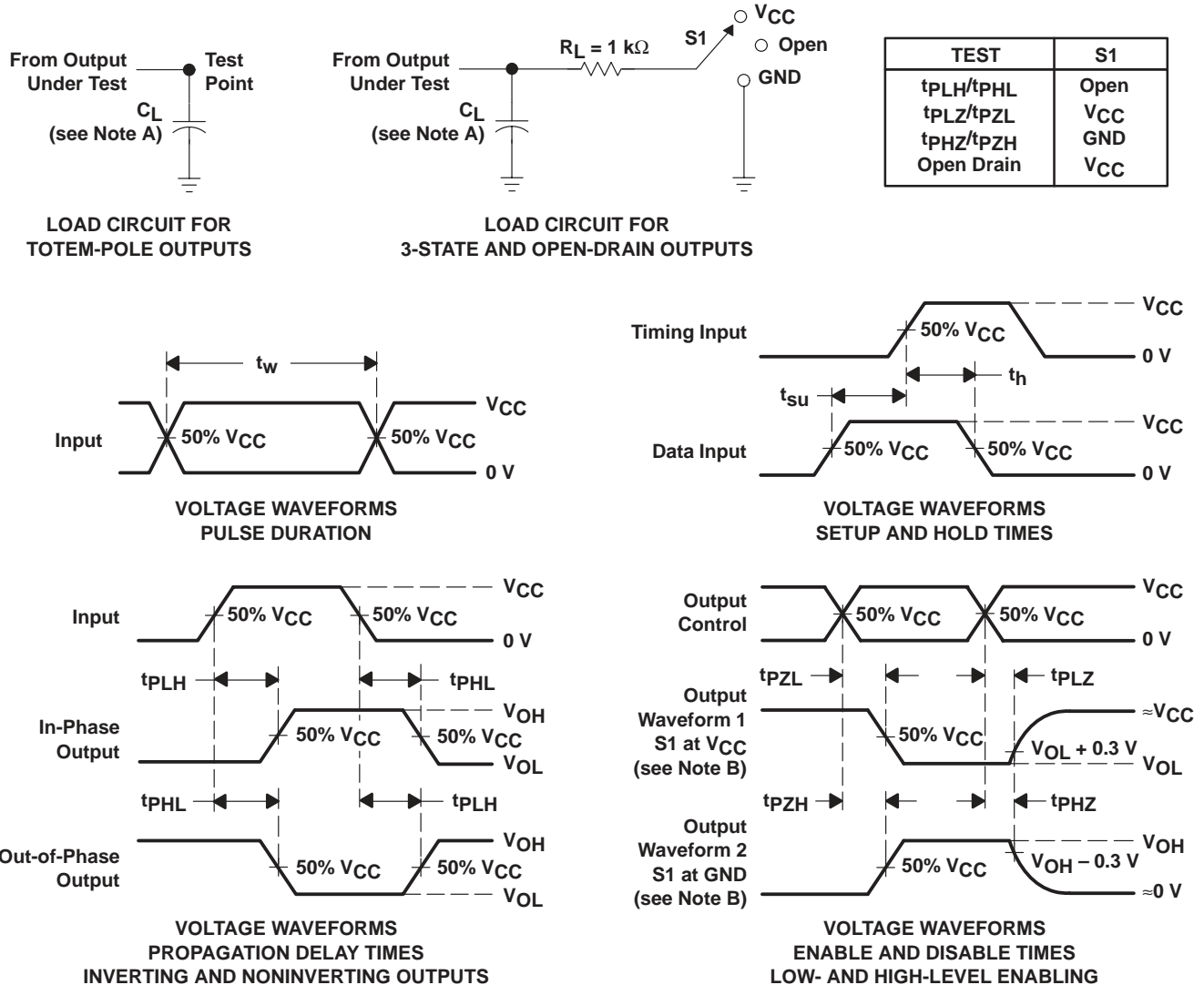
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC16240DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16240	Samples
SN74AHC16240DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE240	Samples
SN74AHC16240DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16240	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16240DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AHC16240DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16240DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AHC16240DGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0

TUBE

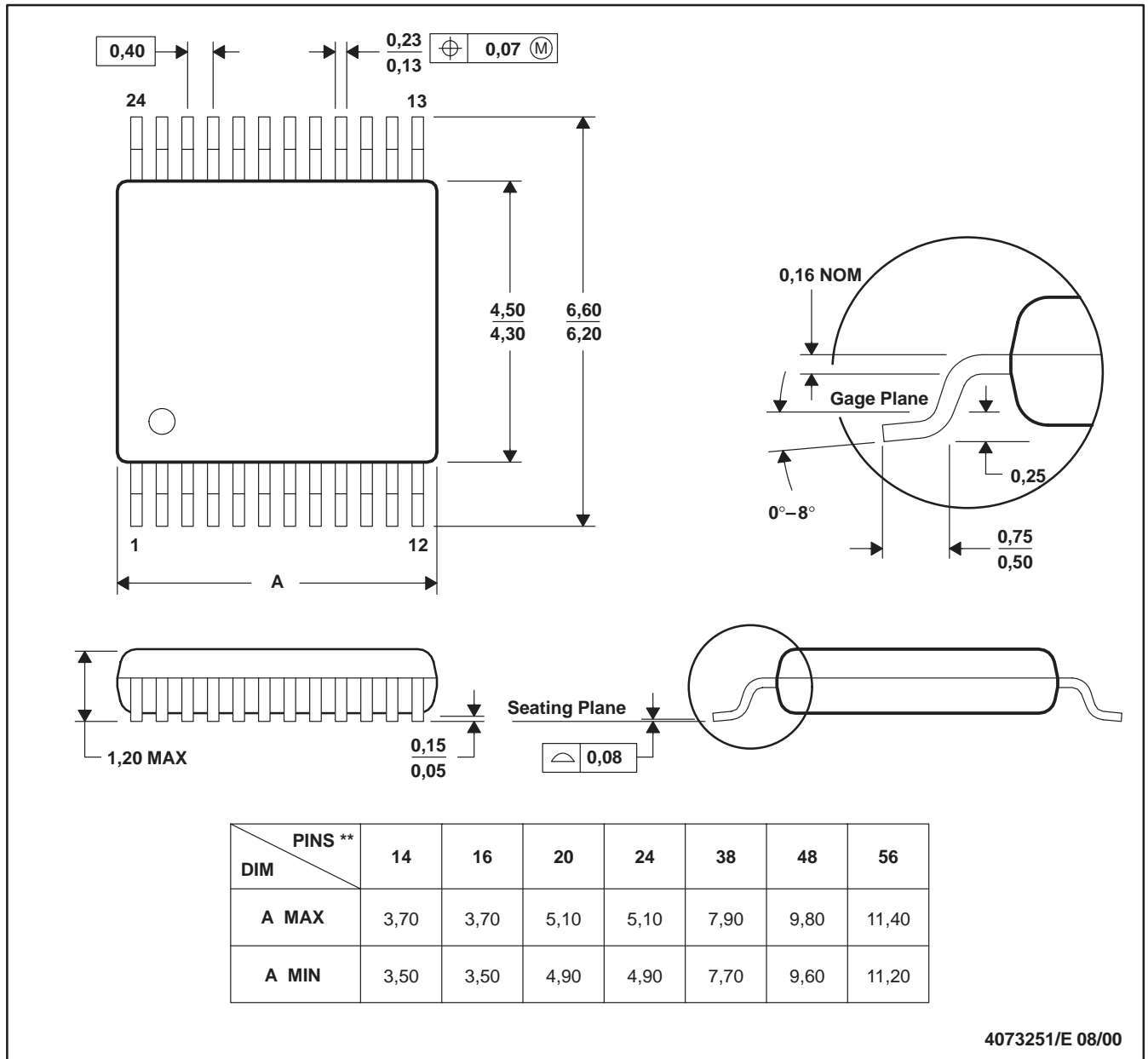

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC16240DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

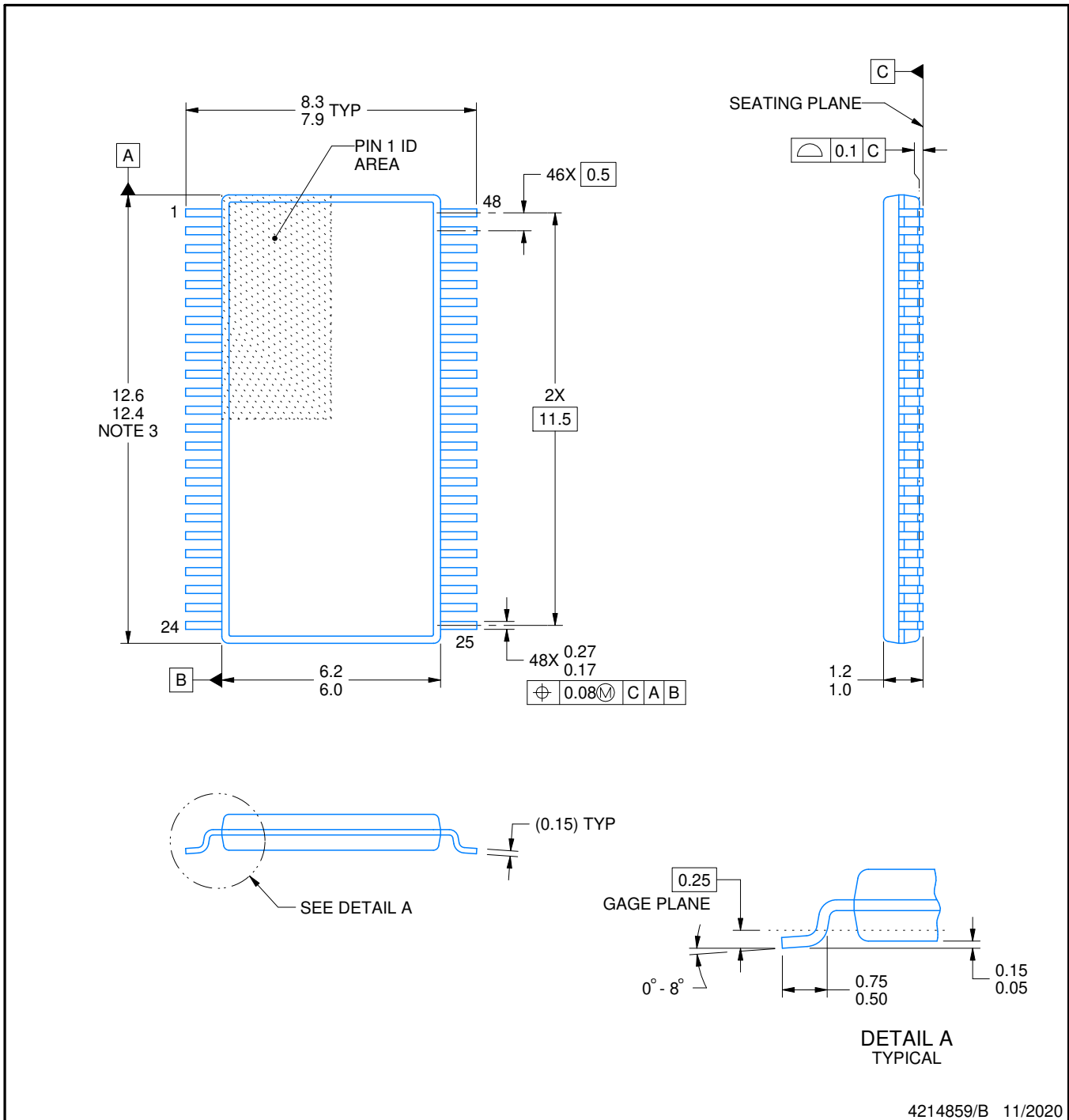
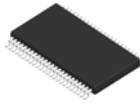
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

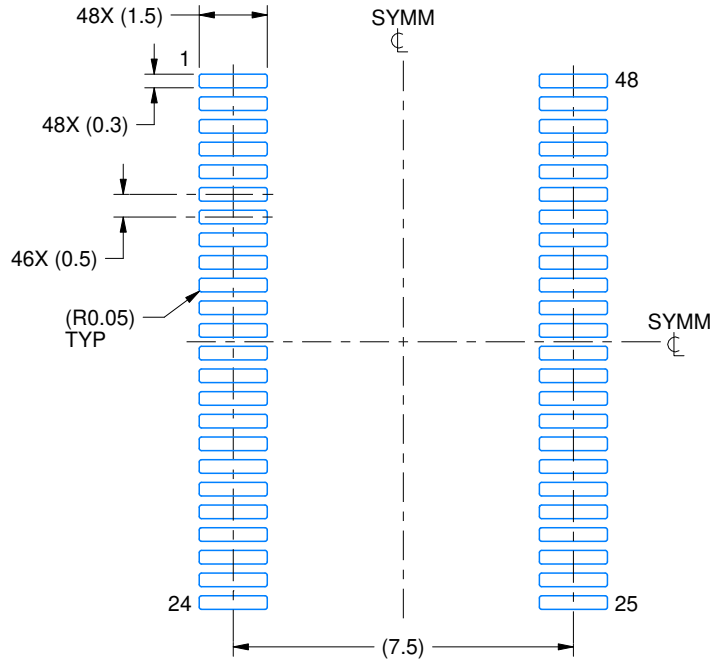
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

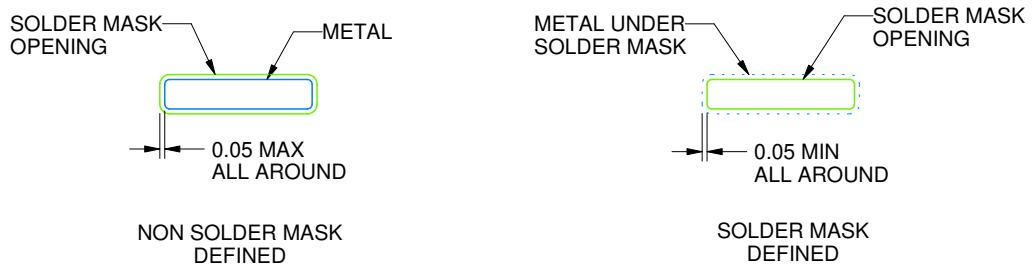
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

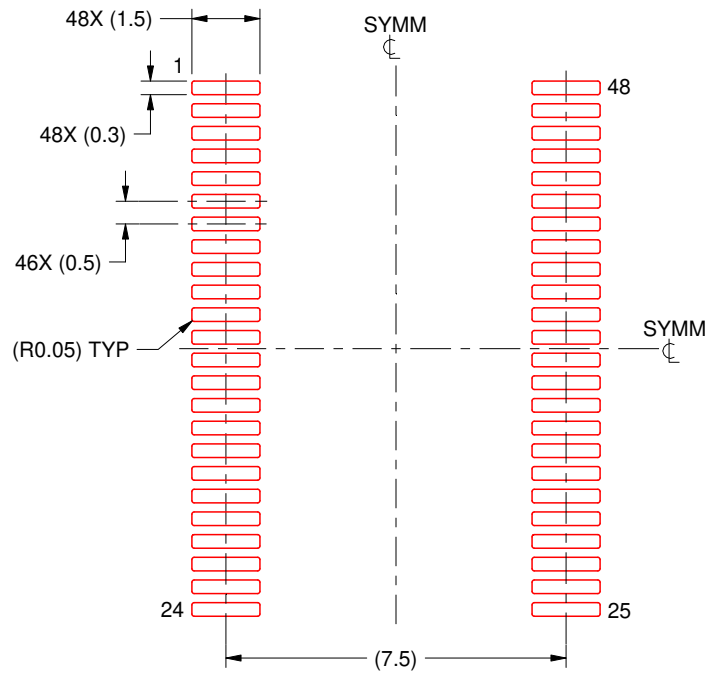
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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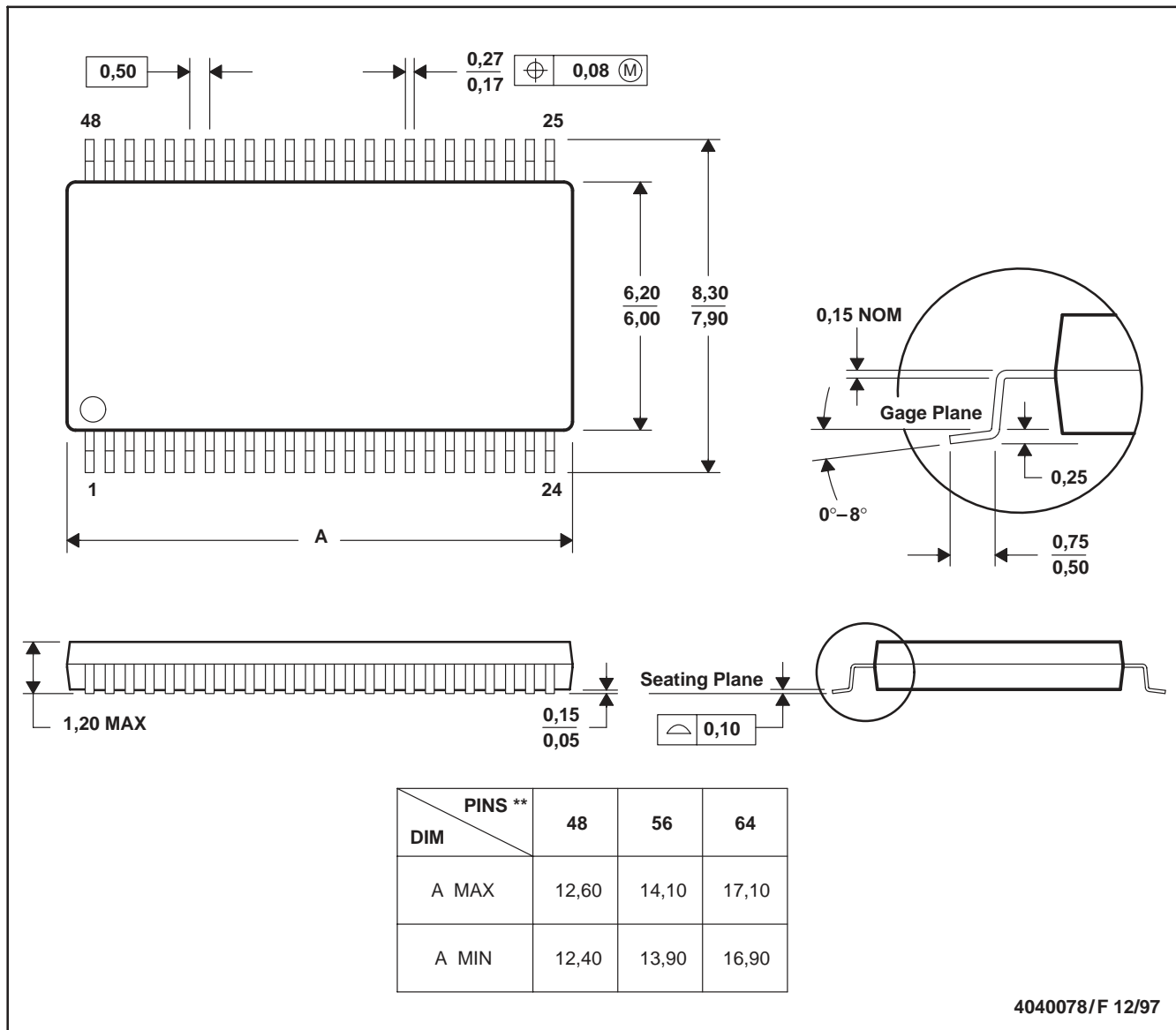
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

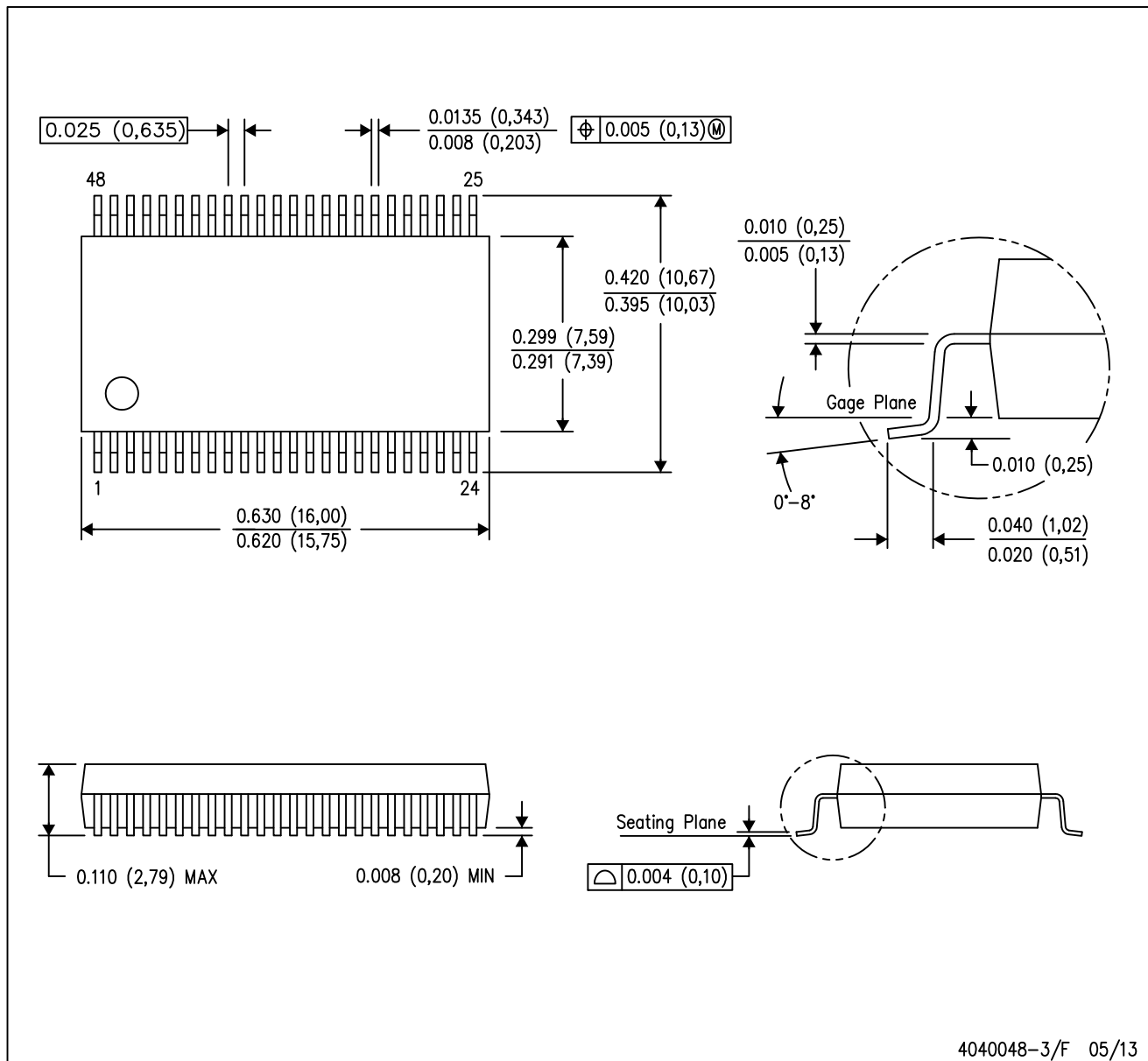


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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