

74F153 Dual 4-Input Multiplexer

General Description

The F153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the F153 can generate any two functions of three variables.

Features

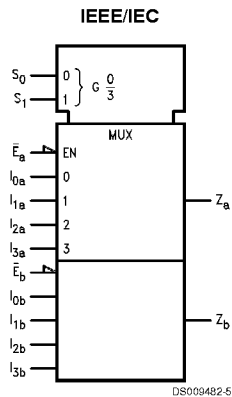
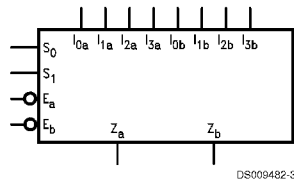
- Guaranteed 4000V minimum ESD protection

Ordering Code:

Commercial	Package Number	Package Description
74F153PC	N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
74F153SC (Note 1)	M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F153SJ (Note 1)	M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ

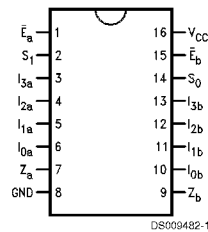
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols



Connection Diagram

Pin Assignment for DIP and SOIC



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 μA –0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 μA –0.6 mA
S_0, S_1	Common Select Inputs	1.0/1.0	20 μA –0.6 mA
\bar{E}_a	Side A Enable Input (Active LOW)	1.0/1.0	20 μA –0.6 mA
\bar{E}_b	Side B Enable Input (Active LOW)	1.0/1.0	20 μA –0.6 mA
Z_a	Side A Output	50/33.3	–1 mA/20 mA
Z_b	Side B Output	50/33.3	–1 mA/20 mA

Functional Description

The F153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a, \bar{E}_b) which can be used to strobe the outputs independently. When the Enables (\bar{E}_a, \bar{E}_b) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are as follows:

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

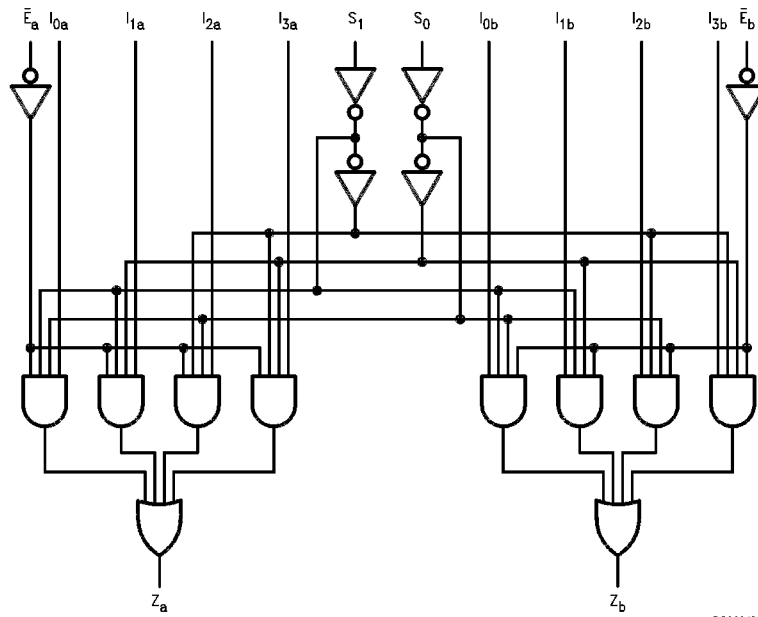
The F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	\bar{E}	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW
X = Immaterial

Logic Diagram



DS009482-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature	
under Bias	-55°C to +125°C
Junction Temperature	
under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to	
Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}

3-STATE Output -0.5V to +5.5V
 Current Applied to Output
 in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature
 Commercial 0°C to +70°C
 Supply Voltage
 Commercial +4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

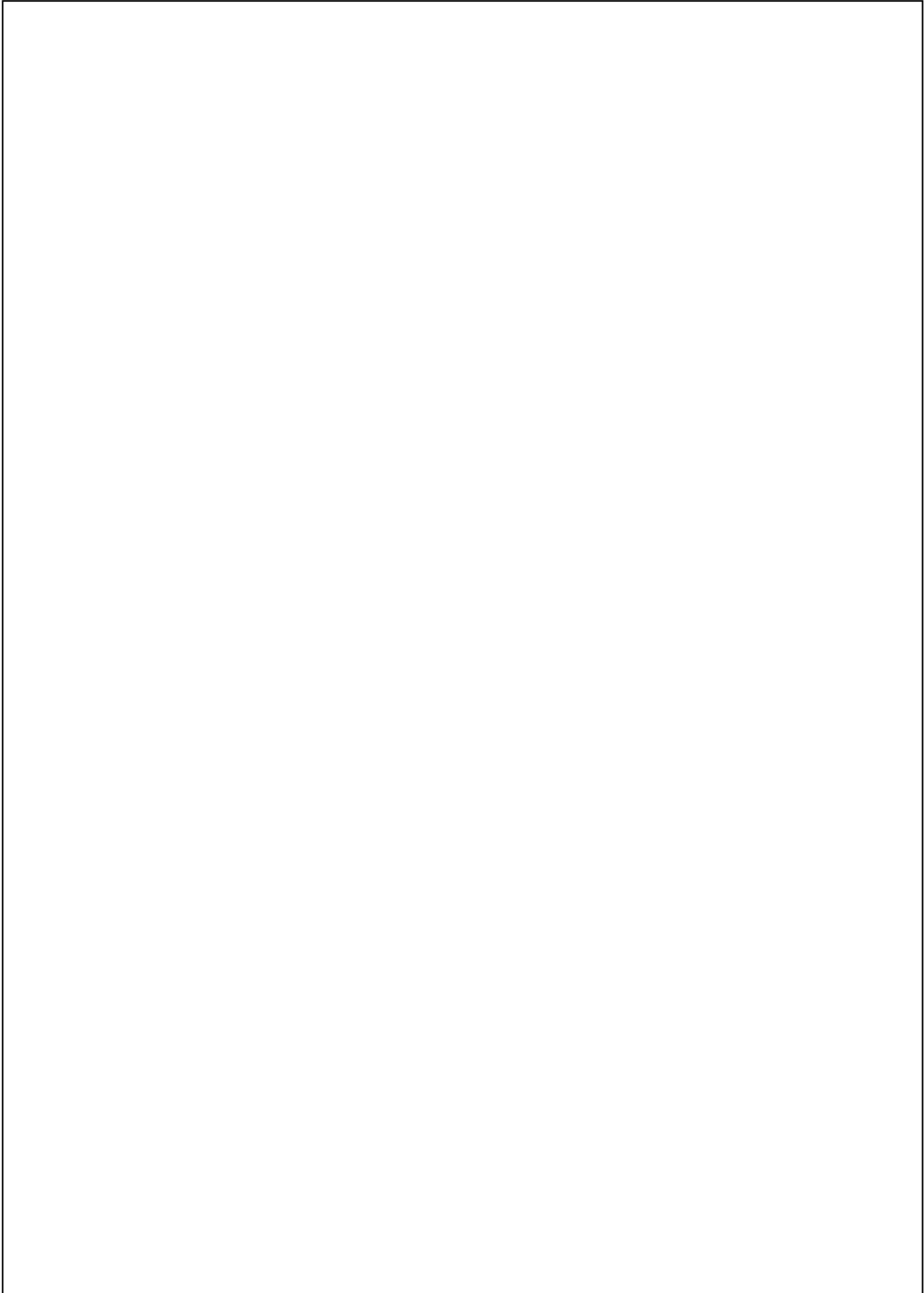
Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

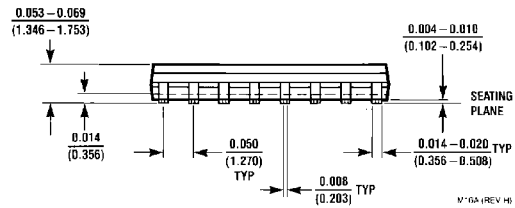
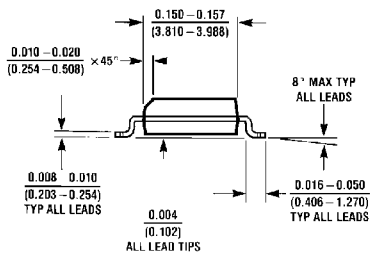
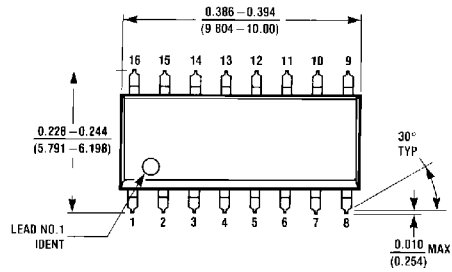
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		5% V _{CC}	2.7				I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCL}	Power Supply Current		12	20	mA	Max	V _O = LOW

AC Electrical Characteristics

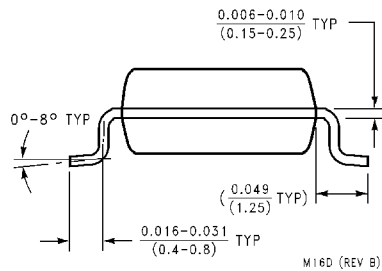
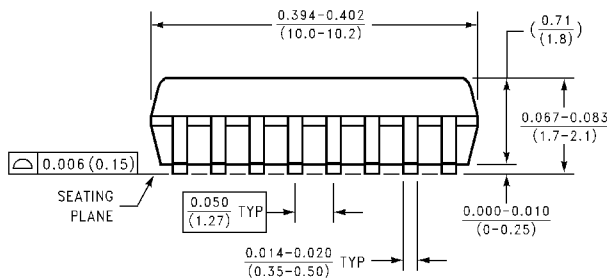
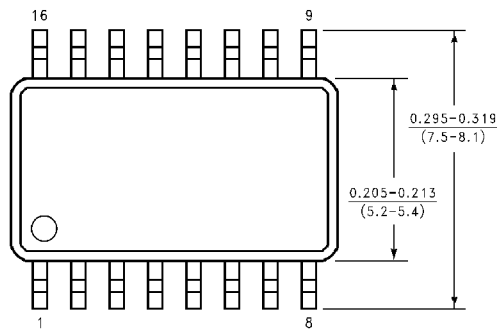
Symbol	Parameter	74F					Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	4.5	8.1	10.5	4.5	12.0	ns
t _{PHL}	S _n to Z _n	3.5	7.0	9.0	3.5	10.5	
t _{PLH}	Propagation Delay	4.5	7.1	9.0	4.5	10.5	ns
t _{PHL}	\bar{E}_n to Z _n	3.0	5.7	7.0	2.5	8.0	
t _{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	8.0	ns
t _{PHL}	I _n to Z _n	2.5	5.1	6.5	2.5	7.5	



Physical Dimensions inches (millimeters) unless otherwise noted

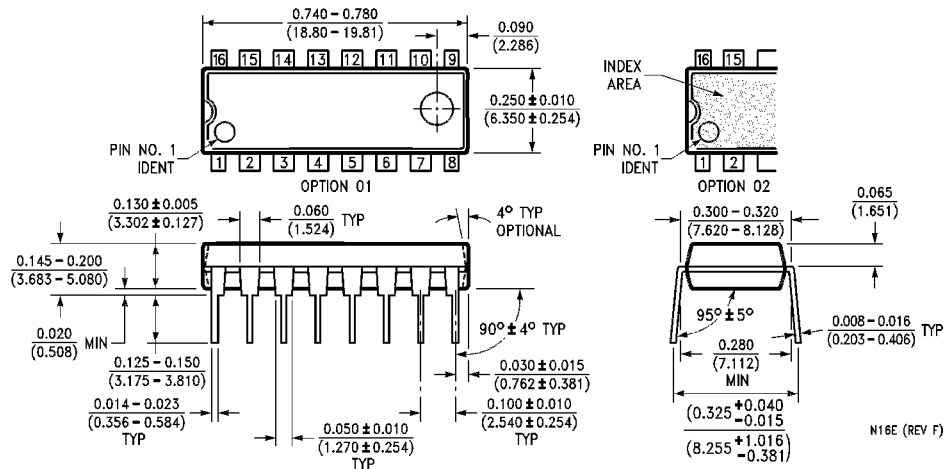


**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M16A**



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N16E**

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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