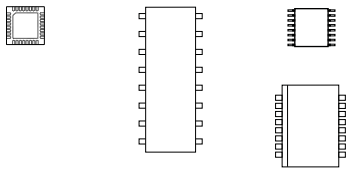
Serial-Input Constant-Current Latched LED Drivers with Open LED Detection

Features and Benefits

- 3.0 to 5.5 V logic supply range
- Schmitt trigger inputs for improved noise immunity
- Power-On Reset (POR)
- Up to 90 mA constant-current sinking outputs
- LED open circuit detection
- Low-power CMOS logic and latches
- High data input rate
- 20 ns typical staggering delay on the outputs
- Internal UVLO and thermal shutdown (TSD) circuitry

Packages:

28 pin QFN (suffix ET)
16 and 24 pin DIP (suffix A)
16 and 24 pin TSSOP (suffix LP)
16 and 24 pin SOIC (suffix LW)



Not to scale

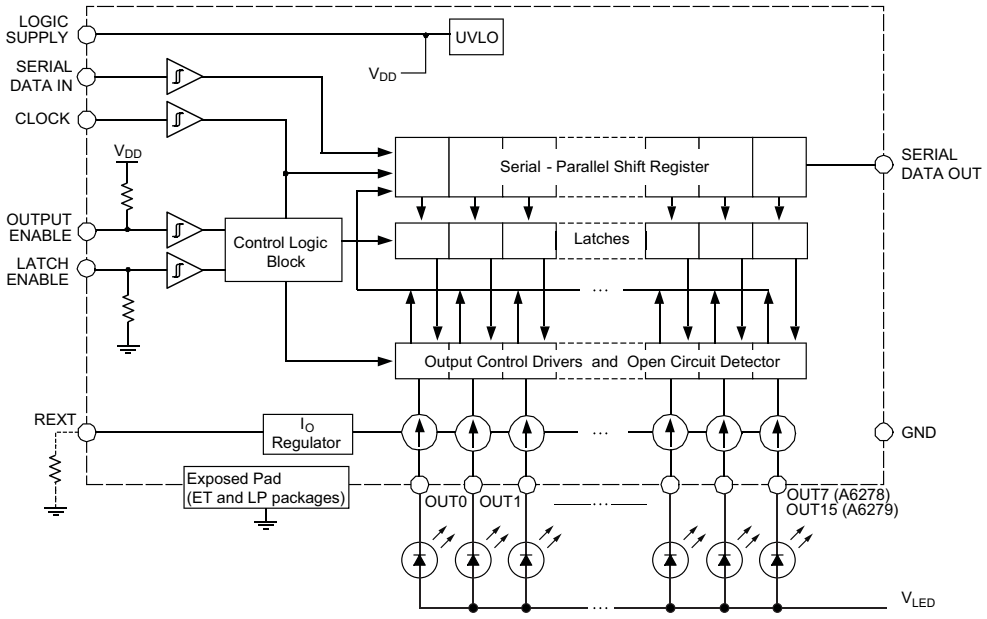
Description

The A6278 and A6279 devices are specifically designed for LED display applications. Each of these BiCMOS devices includes a CMOS shift register, accompanying data latches, and NPN constant-current sink drivers. The A6278 contains 8 sink drivers, while there are 16 in the A6279.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 or 5 V logic supply, typical serial data-input rates can reach up to 25 MHz. The LED drive current is determined by the user's selection of a single resistor. A CMOS serial data output permits cascading between multiple devices in applications requiring additional drive lines. Open LED connections can be detected and signaled back to the host microprocessor through the SERIAL DATA OUT pin.

Four package styles are provided: a QFN surface mount, 0.90 mm overall height nominal (A6279 only); a DIP (type A) for through-hole applications; and for leaded surface-mount, an SOIC (type LW) and a TSSOP with exposed thermal pad (type LP). All package styles for the A6278 are electrically identical to each other, as are the A6279 package styles. All packages are lead (Pb) free, with 100% matte tin plated leadframes.

Functional Block Diagram



Selection Guide

Part Number	Packing	Package Type	Terminals	LED Drive Lines
A6278EA-T[1]	25 pieces per tube	DIP	16	8
A6278ELPTR-T[1]	4000 pieces per 13-in. reel	TSSOP with exposed thermal pad		
A6279ELPTR-T	4000 pieces per 13-in. reel	TSSOP with exposed thermal pad	24	16
A6279ELWTR-T[2]	1000 pieces per 13-in. reel	SOICW		
A6279EETTR-T	1500 pieces per 7-in. reel	MLP surface mount	28	16

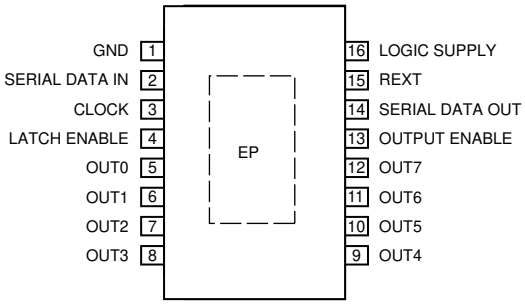
[1]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 1, 2010. Deadline for receipt of LAST TIME BUY orders is April 30, 2011. Recommended substitute: A6279.
[2]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 3, 2010. Deadline for receipt of LAST TIME BUY orders is October 29, 2010. Recommended substitute: A6279.

Absolute Maximum Ratings

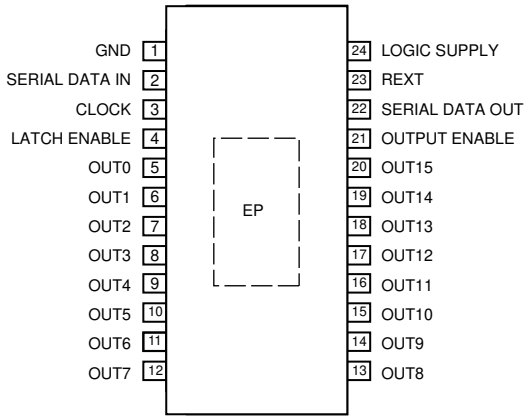
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
LOGIC SUPPLY Voltage Range	V_{DD}			–	–	7.0	V
Load Supply Voltage Range	V_{LED}			–0.5	–	17	V
OUTx Current (any single output)	I_O			–	–	90	mA
Ground Current	I_{GND}	A6278		–	–	750	mA
		A6279		–	–	1475	mA
Logic Input Voltage Range	V_I			–0.4		V_{DD} + 0.4	V
Operating Temperature Range (E)	T_A			–40	–	85	°C
Junction Temperature	T_J			–	–	150	°C
Storage Temperature Range	T_S			–55	–	150	°C

Pin-out Diagrams

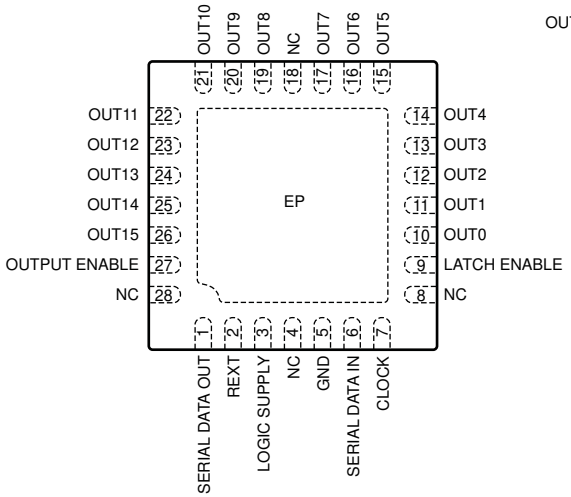
Package A, LW, LP
16-pin



Package A, LW, LP
24-pin



Package ET



Terminal List Table

Number			Name	Function
A, LW, LP		ET		
A6278	A6279	A6279		
1	1	5	GND	Reference terminal for logic ground and power ground
2	2	6	SERIAL DATA IN	Serial-data input to the shift-register
3	3	7	CLOCK	Clock input terminal; data is shifted on the rising edge of the clock.
4	4	9	LATCH ENABLE	Data strobe input terminal; serial data is latched with a high-level input
5 TO 12	5 TO 20	10 to 26	OUT*x*	Current-sinking output terminals
13	21	27	OUTPUT ENABLE	(Active low) Set low to enable output drivers; set high to turn OFF (blank) all output drivers
14	22	1	SERIAL DATA OUT	CMOS serial-data output; for cascading to the next device (to that device SERIAL DATA IN pin); for reading OCD bits.
15	23	2	REXT	An external resistor at this terminal establishes the output current for all of the sink drivers.
16	24	3	LOGIC SUPPLY	(V_{DD}) Logic supply voltage (typically 3.3 or 5.0 V)
–	–	4, 8, 18, 28	NC	No connection
–	–	–	EP	LP and ET packages only; exposed thermal pad for heat dissipation

OPERATING CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Unit
ELECTRICAL CHARACTERISTICS valid at T_A = 25°C, V_{DD} = 3.0 to 5.5 V, unless otherwise noted						
LOGIC SUPPLY Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
Undervoltage Lockout	$V_{DD(UV)}$	V_{DD} = 0.0 → 5.0 V	2.4	–	2.85	V
		V_{DD} = 5.0 → 0.0 V	2.15	–	2.55	V
Output Current (any single output)	I_O	V_{CE} = 0.7 V, R_{EXT} = 225 Ω	64.2	75.5	86.8	mA
		V_{CE} = 0.7 V, R_{EXT} = 470 Ω	34.1	40.0	45.9	mA
		V_{CE} = 0.6 V, R_{EXT} = 3900 Ω	4.25	5.0	5.75	mA
Output Current Matching (difference between any two outputs at the same V_{CE})	ΔI_O	$V_{CE(A)}$ = $V_{CE(B)}$ = 0.7 V, R_{EXT} = 225 Ω	–	±1.0	±6.0	%
		$V_{CE(A)}$ = $V_{CE(B)}$ = 0.7 V, R_{EXT} = 470 Ω	–	±1.0	±6.0	%
		$V_{CE(A)}$ = $V_{CE(B)}$ = 0.6 V, R_{EXT} = 3900 Ω	–	±1.0	±6.0	%
Output Leakage Current	I_{CEX}	V_{OH} = 15 V	–	1.0	5.0	µA
Logic Input Voltage	V_{IH}		0.7V_{DD}	–	V_{DD}	V
	V_{IL}		GND	–	0.3V_{DD}	V
Logic Input Voltage Hysteresis	V_{Ihys}	All digital inputs	200	–	400	mV
SERIAL DATA OUT Voltage	V_{OL}	I_{OL} = 500 µA	–	–	0.4	V
	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	–	–	V
Input Resistance	R_I	OUTPUT ENABLE input, Pull Up	150	300	600	kΩ
		LATCH ENABLE input, Pull Down	100	200	400	kΩ
LOGIC SUPPLY Current	$I_{DD(OFF)}$	R_{EXT} = open, V_{OE} = 5 V	–	–	1.4	mA
		R_{EXT} = 470 Ω, V_{OE} = 5 V	–	–	5.0	mA
		R_{EXT} = 225 Ω, V_{OE} = 5 V	–	–	8.0	mA
	$I_{DD(ON)}$	R_{EXT} = 3900 Ω, V_{OE} = 0 V	–	–	3.0	mA
		R_{EXT} = 470 Ω, V_{OE} = 0 V	–	–	18.0	mA
		R_{EXT} = 225 Ω, V_{OE} = 0 V	–	–	32.0	mA
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	°C
Open LED Detection Threshold	$V_{CE(ODC)}$	I_O > 5 mA, V_{CE} ≥ 0.6 V	–	0.30	–	V
SWITCHING CHARACTERISTICS valid at T_A = 25°C, V_{DD} = V_{IH} = 3.0 to 5.5 V, V_{CE} = 0.7 V, V_{IL} = 0 V, R_{EXT} = 470 Ω, I_O = 40 mA, V_{LED} = 3 V, R_{LED} = 58 Ω, C_{LED} = 10 pF, unless otherwise noted						
CLOCK Pulse Width	t_{high}, t_{low}	Normal Mode	20	–	–	ns
SERIAL DATA IN Setup Time	$t_{SU(D)}$		10	–	–	ns
SERIAL DATA IN Hold Time	$t_{H(D)}$		10	–	–	ns
LATCH ENABLE Setup Time	$t_{SU(LE)}$		20	–	–	ns
LATCH ENABLE Hold Time	$t_{H(LE)}$		20	–	–	ns
OUTPUT ENABLE Set Up Time	$t_{SU(OE)}$		40	–	–	ns
OUTPUT ENABLE Hold Time	$t_{H(OE)}$		20	–	–	ns
OUTPUT ENABLE Pulse Width	$t_{W(OE)}$		1200	–	–	ns
CLOCK to SERIAL DATA OUT Propagation Delay Time	$t_{P(DO)}$		30	–	–	ns
OUTPUT ENABLE to OUT0 Propagation Delay Time	$t_{P(OE)}$		–	75	–	ns
Staggering Delay (between consecutive outputs)	t_D		10	20	40	ns
Total Delay Time (15 × t_D)	t_{Dtotal}		–	300	–	ns
CLOCK Pulse Width	t_{high}, t_{low}	Test Mode, V_{DD} = 4.5 to 5.5 V	20	–	–	ns
SERIAL DATA IN Setup Time	$t_{SU(D)}$		20	–	–	ns
SERIAL DATA IN Hold Time	$t_{H(D)}$		20	–	–	ns
LATCH ENABLE Setup Time	$t_{SU(LE)}$		40	–	–	ns
LATCH ENABLE Hold Time	$t_{H(LE)}$		20	–	–	ns
OUTPUT ENABLE Set Up Time	$t_{SU(OE)}$		40	–	–	ns
OUTPUT ENABLE Hold Time	$t_{H(OE)}$		20	–	–	ns
OUTPUT ENABLE Pulse Width*	$t_{W(OE)}$		2.0	–	–	us
CLOCK to SERIAL DATA OUT Propagation Delay Time	$t_{P(DO)}$		30	–	–	ns
OUTPUT ENABLE to OUT0 Propagation Delay Time	$t_{P(OE)}$		–	75	–	ns
Staggering Delay (between consecutive outputs)	t_D		10	20	40	ns
Total Delay Time (15 × t_D)	t_{Dtotal}		–	300	–	ns
Output Fall Time	t_f	90% to 10% voltage	–	75	150	ns
Output Rise Time	t_r	10% to 90% voltage	–	75	150	ns

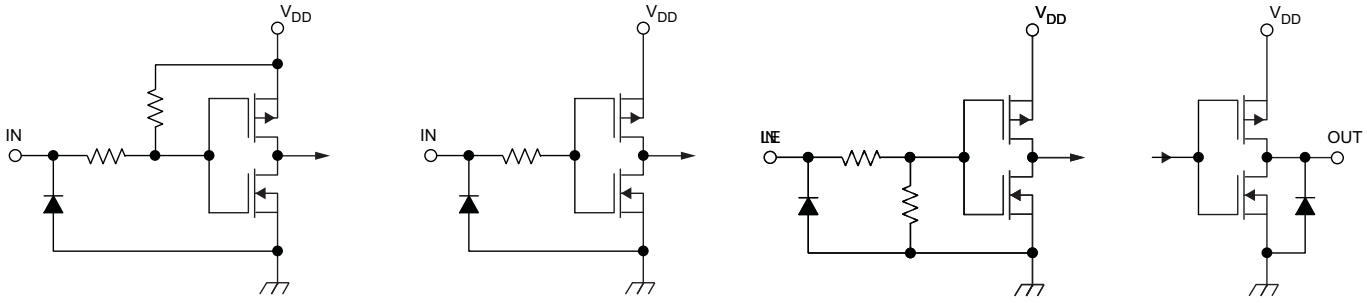
*See LED Open Circuit Detection (Test) mode timing diagram.

Truth Table

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Out	Latch Enable Input	Latch Contents	Output Enable Input	Output Contents
		I_0 I_1 I_2 … I_{n-1} I_n			I_0 I_1 I_2 … I_{n-1} I_n		I_0 I_1 I_2 … I_{n-1} I_n
H	↑	H R_0 R_1 … R_{n-2} R_{n-1}	R_{n-1}				
L	↑	L R_0 R_1 … R_{n-2} R_{n-1}	R_{n-1}				
X	↓	R_0 R_1 R_2 … R_{n-1} R_n	R_n				
		X X X … X X	X	L	R_0 R_1 R_2 … R_{n-1} R_n		
		P_0 P_1 P_2 … P_{n-1} P_n	P_n	H	P_0 P_1 P_2 … P_{n-1} P_n	L	P_0 P_1 P_2 … P_{n-1} P_n
					X X X … X X	H	H H H … H H

L = Low logic (voltage) level
H = High logic (voltage) level
X = Don't care
P = Present state
R = Previous state
n = 7 for the A6278, n = 15 for the A6279

Inputs and Outputs Equivalent Circuits



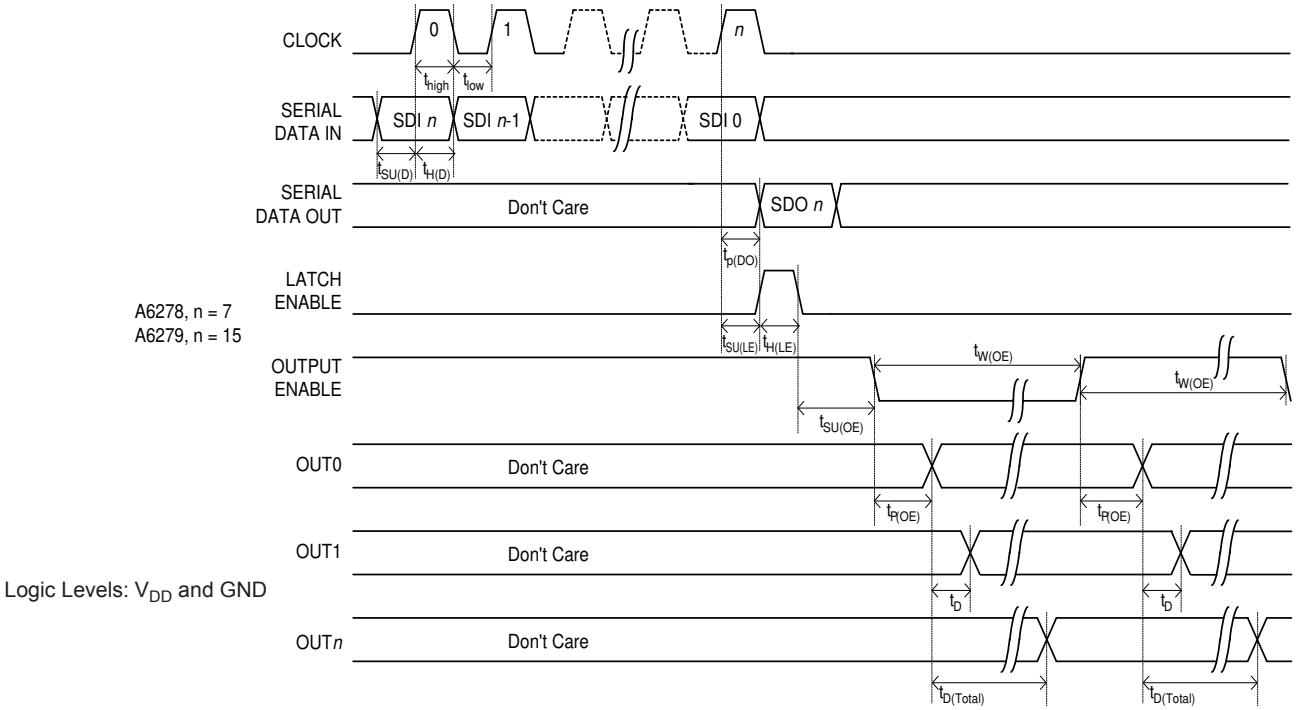
OUTPUT ENABLE (active low)

CLOCK and SERIAL DATA IN

LATCH ENABLE

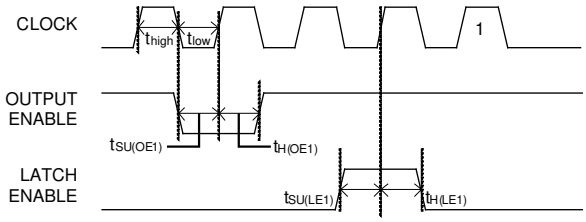
SERIAL DATA OUT

Normal Mode Timing Requirements

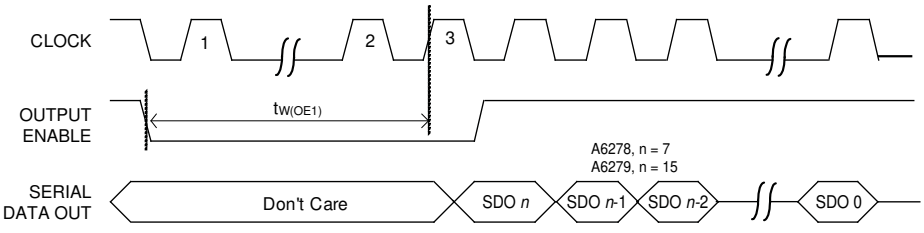


LED Open Circuit Detection (Test) Mode Timing Requirements

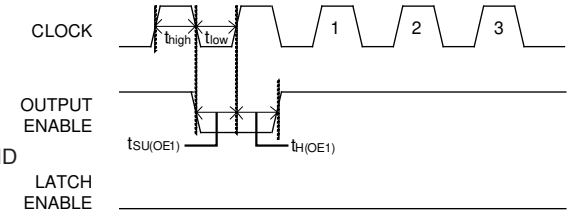
(A) To enter LED OCD mode, a minimum of one CLOCK pulse is required after LATCH ENABLE is brought back low.



(B) To output the latched error code, OUTPUT ENABLE must be held low a minimum of 3 CLOCK cycles.



(C) When returning to Normal mode, a minimum of three CLOCK pulses is required after OUTPUT ENABLE is brought back high.



Functional Description

Normal Mode

Serial data present at the SERIAL DATA IN input is transferred to the shift register on the logic 0-to-logic 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the register shifts data towards the SERIAL DATA OUT pin. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

Data present in any register is transferred to the respective latch when the LATCH ENABLE input is high (serial-to-parallel conversion). The latches continue to accept new data as long as the LATCH ENABLE input is held high.

Applications where the latches are bypassed (LATCH ENABLE tied high) will require that the OUTPUT ENABLE input be high during serial data entry. When the OUTPUT ENABLE input is high, the output sink drivers are disabled (OFF).

The data stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input active (low), the outputs are controlled by the state of their respective latches.

LED Open Circuit Detection (Test) Mode

The LED Open Circuit Detection (OCD) mode, or *Test* mode, is entered by clocking in the LED OCD mode initialization sequence on the OUTPUT ENABLE (OE) and LATCH ENABLE (LE) pins. In Normal mode, the OE and LE pins do not change states while the CLOCK signal is cycling. The initialization sequence is shown in panel A of the LED OCD timing requirements diagram on page 7.

Note: Each step event during mode sequencing happens on the leading edge of the CLOCK signal. Five step events (CLOCK pulses) are required to enter OCD mode and five step events are required to return to Normal mode.

A pattern, such as all highs, should first be loaded into the registers and latched leaving LE low. The device is then sequenced into LED OCD mode. It should be noted that data is still being sent through the shift registers while entering the LED OCD mode. However, this data is not latched when the LE pin goes high and sees a CLOCK pulse during the initialization sequence.

Open circuit detection does not take place until the sequence in Panel B on page 7 is performed. During this sequence, the OE pin must be held low for a minimum of 2 µs ($t_{W(OE1)}$) to ensure proper settling of the output currents and be given a minimum of three CLOCK pulses. During the period that the OE pin is low (active), OCD testing begins. The V_{CE} voltage on each of the output pins is compared to the Open LED Detection Theshold, $V_{CE(OCD)}$. If the V_{CE} of an enabled output is lower than $V_{CE(OCD)}$, an error bit value of 0 is set in the corresponding shift register. A value of 1 will be set if no error is detected. If a particular output is not enabled, a 0 will be set. The error codes are summarized in the following table:

Output State Test Condition Error Code Meaning

Output State	Test Condition	Error Code	Meaning
OFF	N/A	0	N/A
ON	$V_{CE} < V_{CE(OCD)}$	0	Open/TSD
	$V_{CE} \geq V_{CE(OCD)}$	1	Normal

After the testing process, setting the OE pin high causes the shift registers to latch the error code data where it can then be clocked out of the SERIAL DATA OUT pin. The OCD latching sequence (OE low, 3 CLOCK pulses, OE high as shown in panel B of the LED OCD timing diagram) can then be repeated if necessary to look for intermittent contact problems.

The state of the outputs can be programmed with new data at any time while in LED OCD mode (the same as in Normal mode). This allows specific patterns to be tested for open circuits. The pattern that is latched will then be tested during the OCD latching sequence and the resulting bit values can be clocked out of the SERIAL DATA OUT pin.

Note: LED Open Circuit Detection will not work properly if the current is being externally limited by resistors to within the set current limit for the device.

To return to Normal mode, perform the clocking sequence shown in panel C of the timing diagram on the OE and LE pins.

Constant Current (R_{EXT})

The A6278 and A6279 allow the user to set the magnitude of the constant current to the LEDs. Once set, the current remains constant regardless of the LED voltage variation, the supply voltage variation, or other circuit parameters that could otherwise affect LED current. The output current is determined by the value of an external current-control resistor (R_{EXT}). The relationship of these parameters is shown in figure 1. Typical characteristics for output current and V_{CE} are shown in figure 2 for common values of R_{EXT}.

Figure 1. Output Current versus Current Control Resistance
T_A= 25°C, V_{CE} = 0.7 V

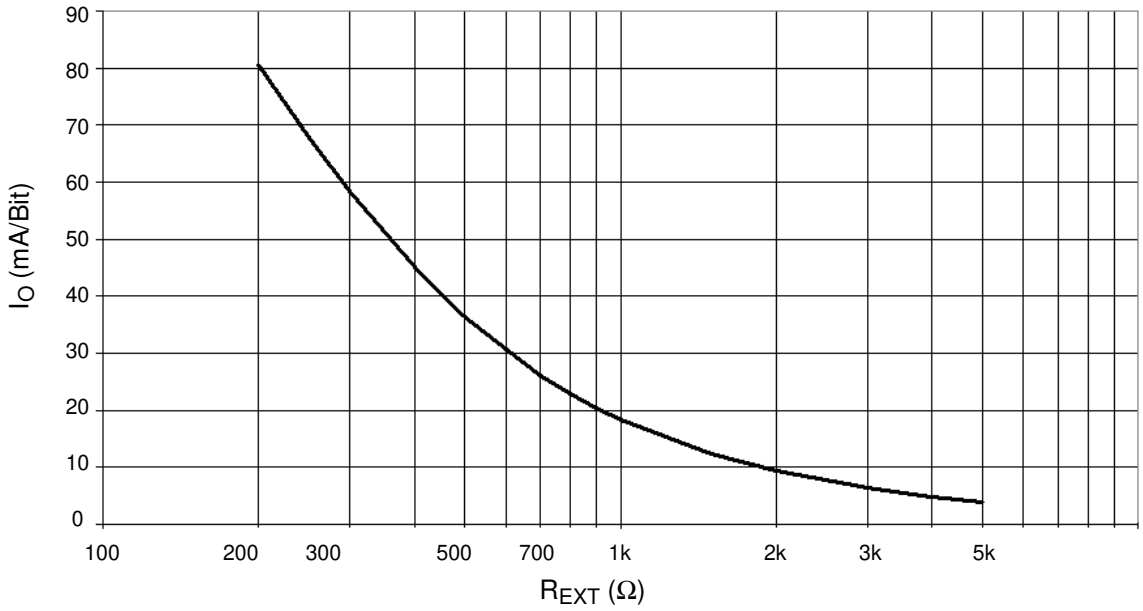
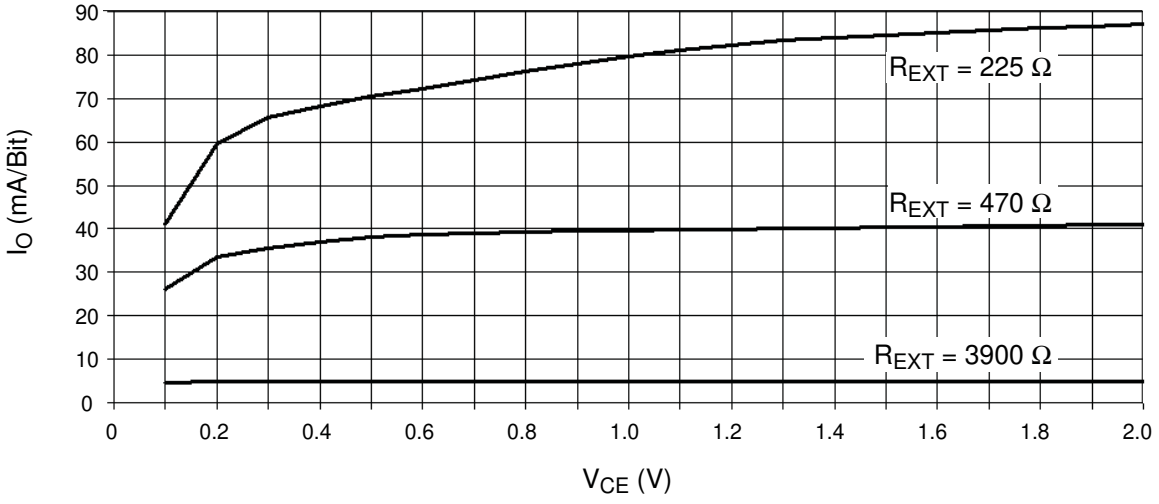


Figure 2. Output Current versus Device Voltage Drop
T_A= 25°C



Undervoltage Lockout

The A6278 and A6279 include an internal under-voltage lockout (UVLO) circuit that disables the outputs in the event that the logic supply voltage drops below a minimum acceptable level. This feature prevents the display of erroneous information, a necessary function for some critical applications.

Upon recovery of the logic supply voltage after a UVLO event, and on power-up, all internal shift registers and latches are set to 0. The A6278/A6279 is then in Normal mode.

Output Staggering Delay

The A6278/A6279 has a 20 ns delay between each output. The staggering of the outputs reduces the in-rush of currents onto the power and ground planes. This aids in power supply decoupling and EMI/EMC reduction.

The output staggering delay occurs under the following conditions:

- OUTPUT ENABLE is pulled low
- OUTPUT ENABLE is held low and LATCH ENABLE is pulled high
- OUTPUT ENABLE is held low, LATCH ENABLE is held high, and CLOCK is pulled high

The 20 ns delays are cumulative across all the outputs. Under any of the above conditions, the state of OUT0 gets set after a typical propagation delay, $t_{P(OE)}$. OUT1 will get set 20 ns after OUT0, and so forth. In the A6279, OUT15 will get set after 300 ns (15 × 20 ns) plus $t_{P(OE)}$.

Note: The maximum CLOCK frequency is reduced in applications where both the OUTPUT ENABLE pin is held low and the LATCH ENABLE pin is held high continuously, and the outputs change state on the CLOCK edges. The staggering delay could cause spurious output responses at CLOCK speeds greater than 1 MHz.

Thermal Shutdown

When the junction temperature of the A6278/A6279 reaches the thermal shutdown temperature threshold, T_{JTSD} (165°C typical), the outputs are shut off until the junction temperature cools down below the recovery threshold, $T_{JTSD} - T_{JTSDhys}$ (15°C typical). The shift register and output latches will remain active during a TSD event. Therefore, there is no need to reset the data in the output latches.

In LED OCD mode, if the junction temperature reaches the Thermal Shut Down threshold, the outputs will turn off, as in Normal mode operation. However, all of the shift registers will be set with 0, the error bit value.

Application Information

Load Supply Voltage (V_{LED})

These devices are designed to operate with driver voltage drops (V_{CE}) of 0.7 to 3V, with an LED forward voltage, V_F, of 1.2 to 4.0 V. If higher voltages are dropped across the driver, package power dissipation will increase significantly. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage, V_{LED}, or to set any series voltage dropping, V_{DROP}, according to the following formula:

$$V_{DROP} = V_{LED} - V_F - V_{CE},$$

with $V_{DROP} = I_O \times R_{DROP}$ for a single driver or for a Zener diode (V_Z), or for a series string of diodes (approximately 0.7 V per diode) for a group of drivers (see figure 3). If the available voltage source, V_{LED}, will cause unacceptable power dissipation and series resistors or diodes are undesirable, a voltage regulator can be used to provide supply voltages.

For reference, typical LED forward voltages are:

LED Type	V_F (V)
White	3.5 to 4.0
Blue	3.0 to 4.0
Green	1.8 to 2.2
Yellow	2.0 to 2.1
Amber	1.9 to 2.65
Red	1.6 to 2.25
Infrared	1.2 to 1.5

Pattern Layout

This device has a common logic ground and power ground terminal, GND. For the LP package, the GND pin should be tied to the exposed metal pad, EP, allowing the ground plane copper to be used to dissipate heat. If the ground pattern layout contains large common mode resistance, and the voltage between the system ground and the LATCH ENABLE, OUTPUT ENABLE, or CLOCK terminals exceeds 2.5 V (because of switching noise), these devices may not work properly.

Package Power Dissipation (P_D)

The maximum allowable package power dissipation based on package type is determined by:

$$P_{D(max)} = (150 - T_A) / R_{\theta JA},$$

where $R_{\theta JA}$ is the thermal resistance of the package, determined experimentally. Power dissipation levels based on the package are shown in the Package Thermal Characteristics section (see page 14).

The actual package power dissipation is determined by:

$$P_{D(act)} = DC \times (V_{CE} \times I_O \times 16) + (V_{DD} \times I_{DD}),$$

where DC is the duty cycle. The value *16* represents the maximum number of available device outputs for the A6279, used for the worst-case scenario (displaying all 16 LEDs; this would be *8* for the A6278).

When the load suppy voltage, V_{LED}, is greater than 3 to 5 V, and $P_{D(act)} > P_{D(max)}$, an external voltage reducer (V_{DROP}) must be used (see figure 3).

Reducing the percent duty cycle, DC, will also reduce power dissipation. Typical results are shown on the following pages.

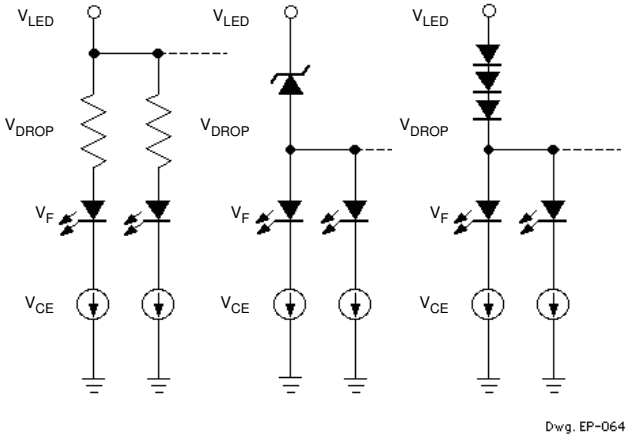
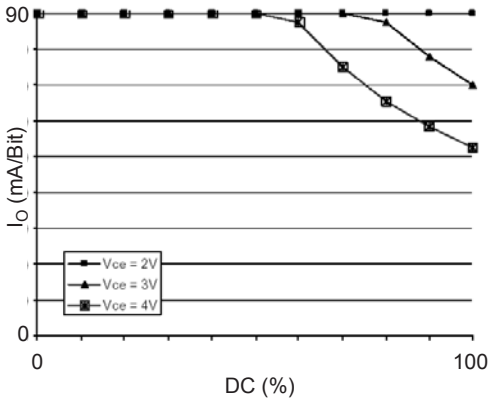


Figure 3. Typical appplications for voltage drops

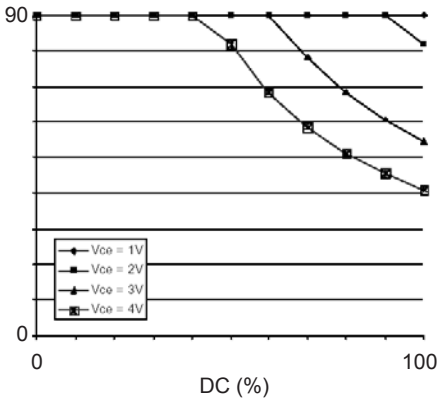
Allowable Output Current versus Duty Cycle, A6278

V_{DD} = 5 V

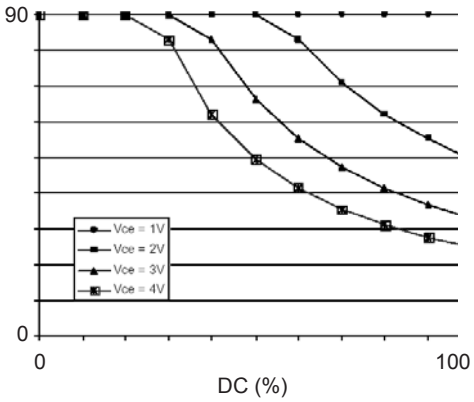
A Package, T_A = 25°C



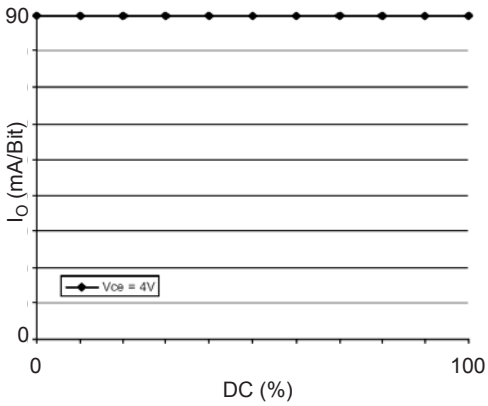
A Package, T_A = 50°C



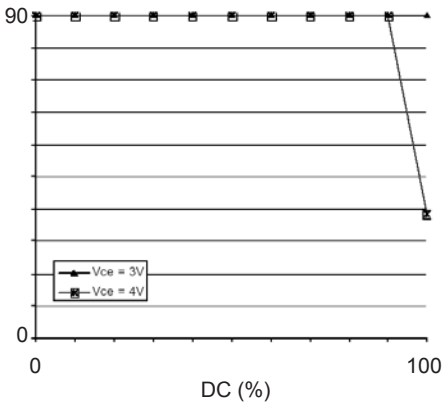
A Package, T_A = 85°C



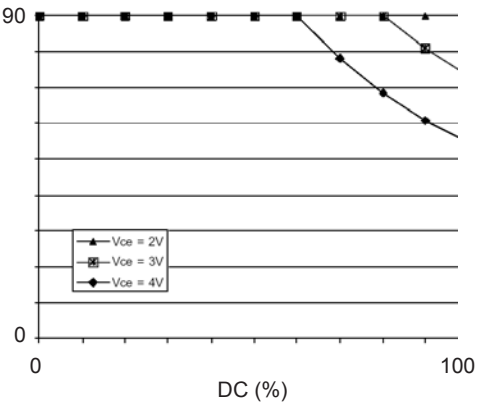
LP Package, T_A = 25°C



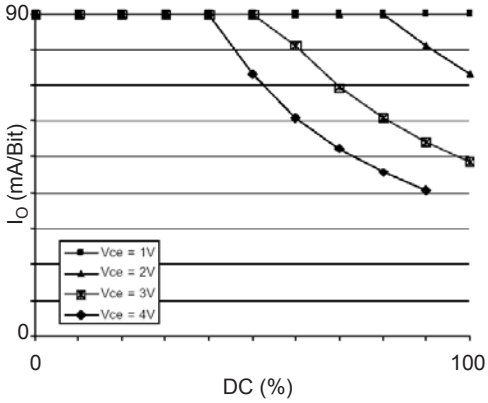
LP Package, T_A = 50°C



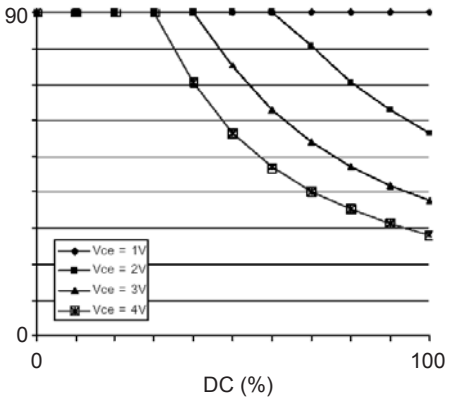
LP Package, T_A = 85°C



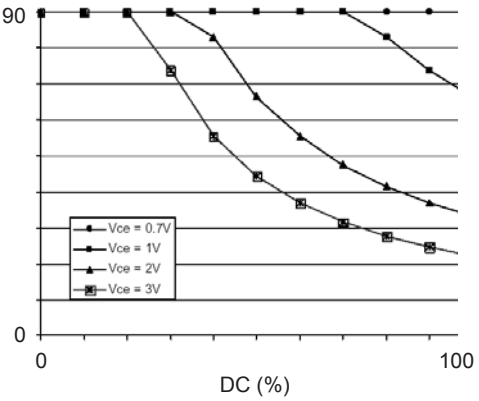
LW Package, T_A = 25°C



LW Package, T_A = 50°C



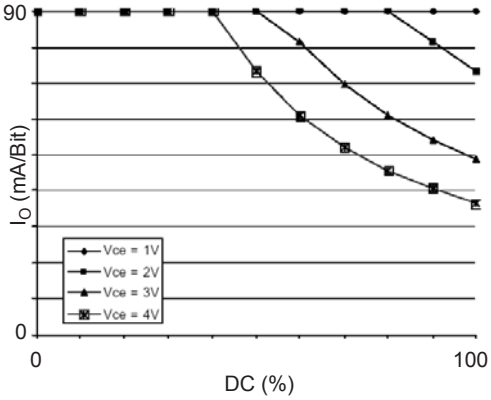
LW Package, T_A = 85°C



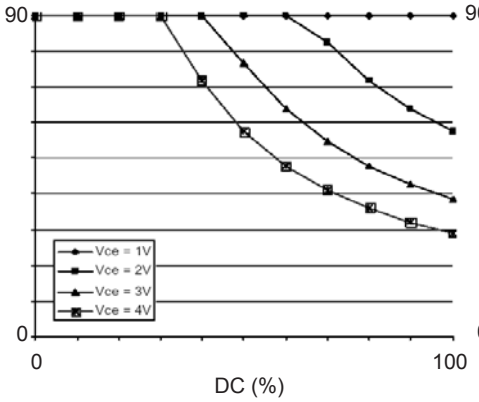
Allowable Output Current versus Duty Cycle, A6279

V_{DD} = 5 V

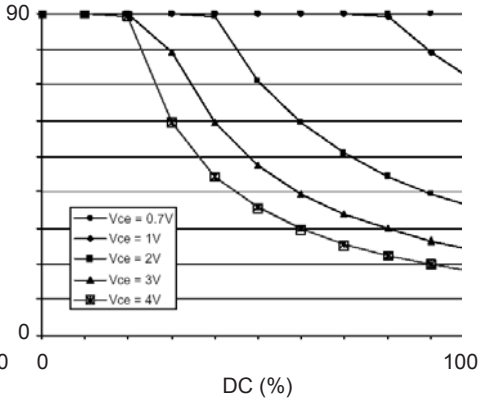
A Package, T_A = 25°C



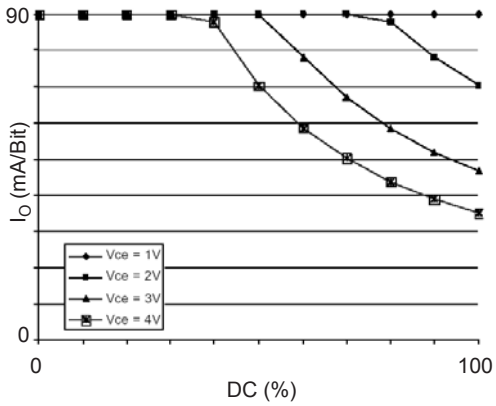
A Package, T_A = 50°C



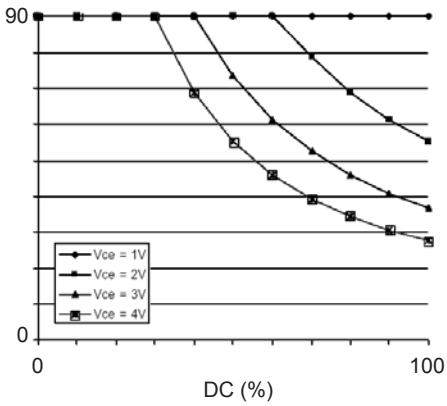
A Package, T_A = 85°C



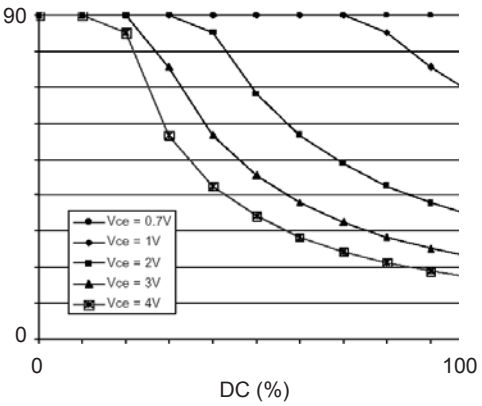
LP Package, T_A = 25°C



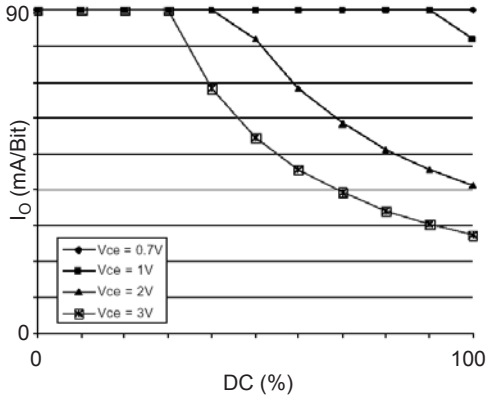
LP Package, T_A = 50°C



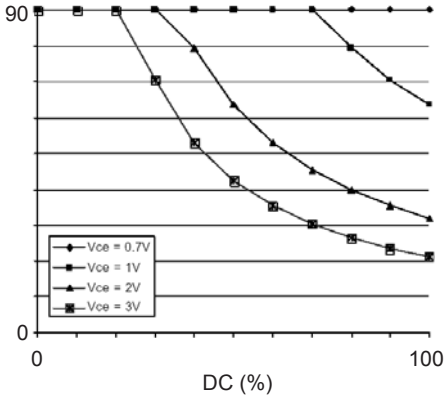
LP Package, T_A = 85°C



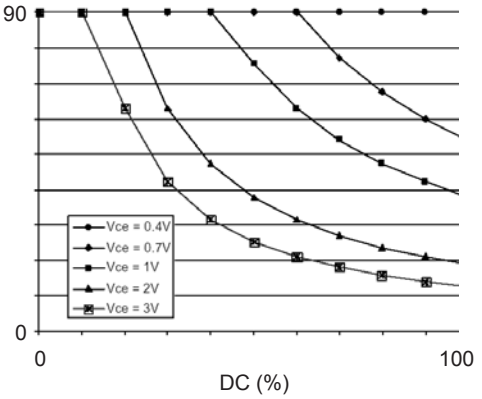
LW Package, T_A = 25°C



LW Package, T_A = 50°C



LW Package, T_A = 85°C

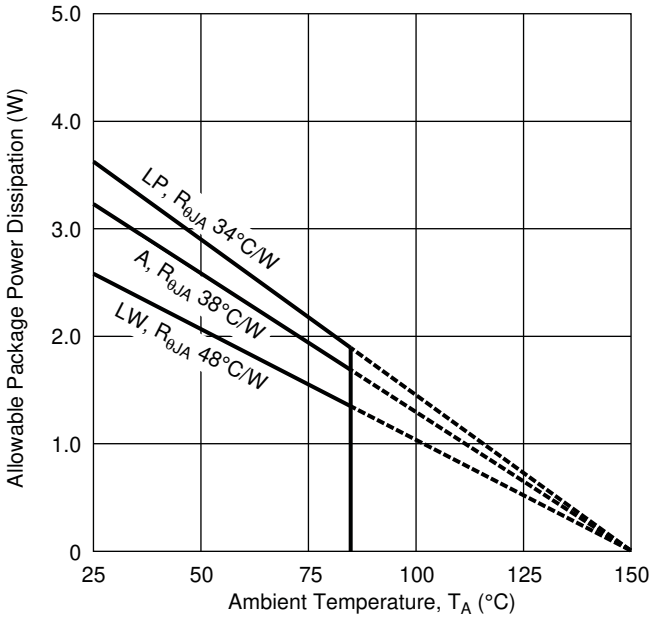


Package Thermal Characteristics

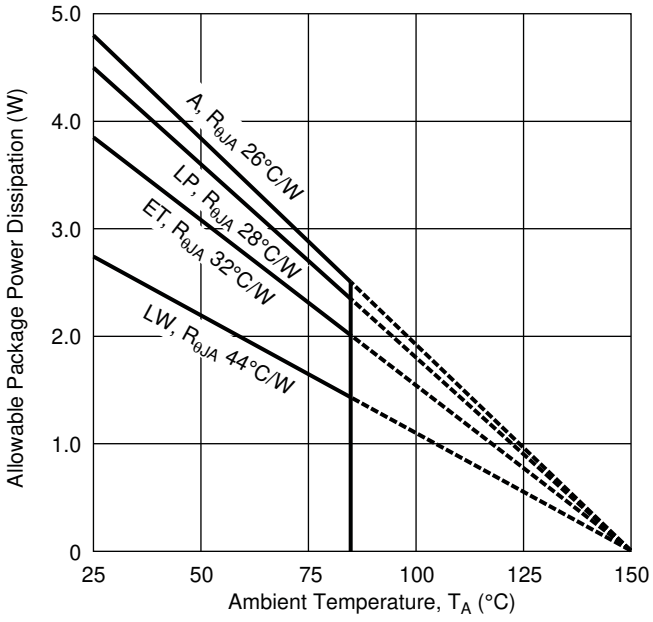
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	A package, 16-pin, measured on 4-layer board based on JEDEC standard	38	°C/W
		A package, 24-pin, measured on 4-layer board based on JEDEC standard	26	°C/W
		LP package, 16-pin, measured on 4-layer board based on JEDEC standard	34	°C/W
		LP package, 24-pin, measured on 4-layer board based on JEDEC standard	28	°C/W
		LW package, 16-pin, measured on 4-layer board based on JEDEC standard	48	°C/W
		LW package, 24-pin, measured on 4-layer board based on JEDEC standard	44	°C/W
		ET package, 24-pin, measured on 4-layer board based on JEDEC standard	32	°C/W

*Additional thermal information is available on the Allegro Web site.

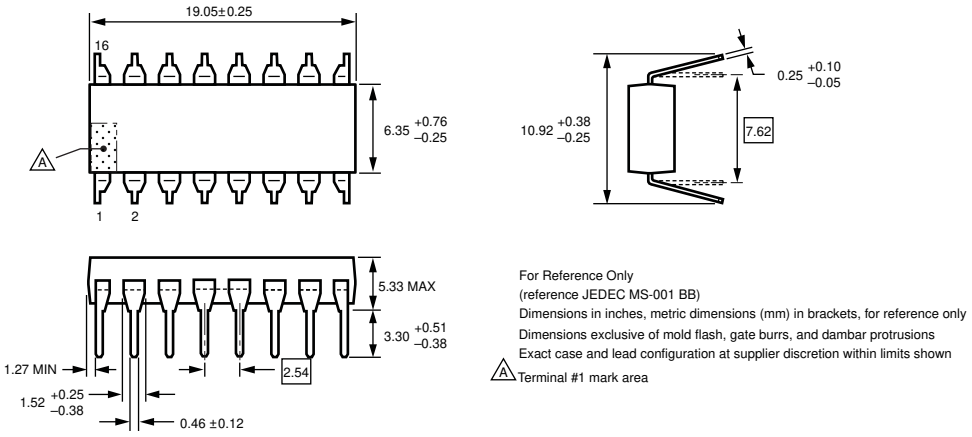
A6278



A6279

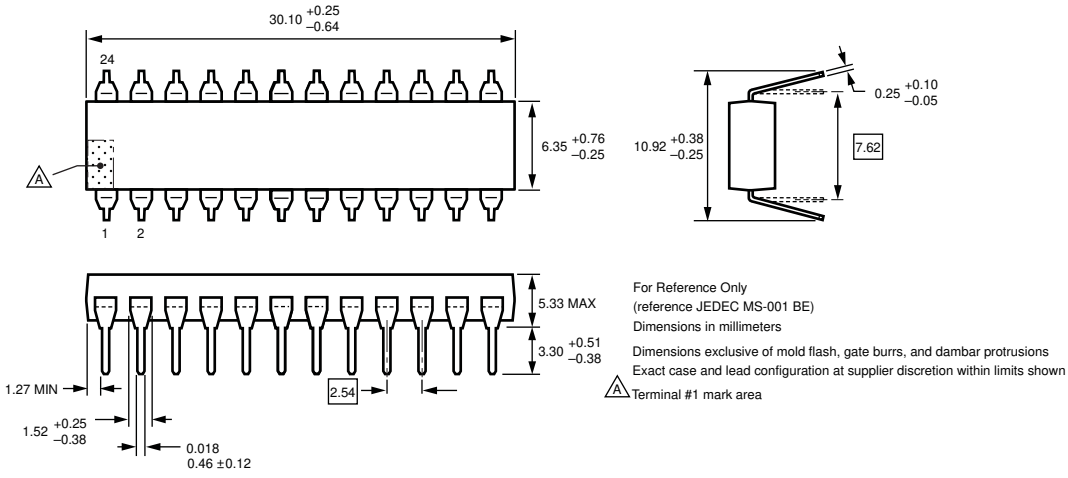


Package A, 16-pin DIP (A6278)



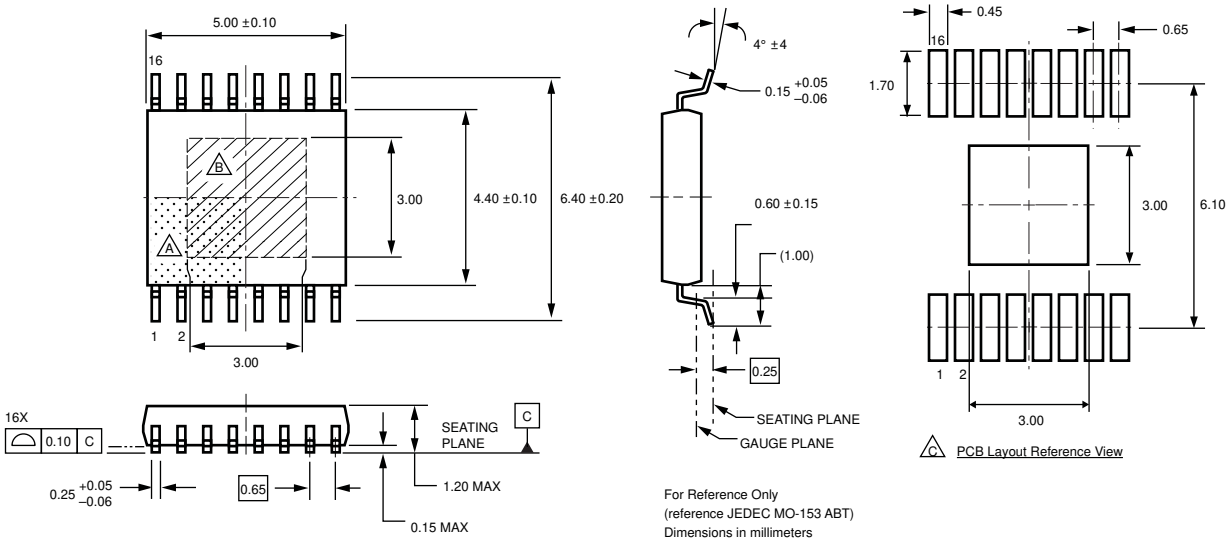
For Reference Only
(reference JEDEC MS-001 BB)
Dimensions in inches, metric dimensions (mm) in brackets, for reference only
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

Package A, 24-pin DIP (A6279)



For Reference Only
(reference JEDEC MS-001 BE)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

Package LP, 16-pin TSSOP with Exposed Thermal Pad (A6278)



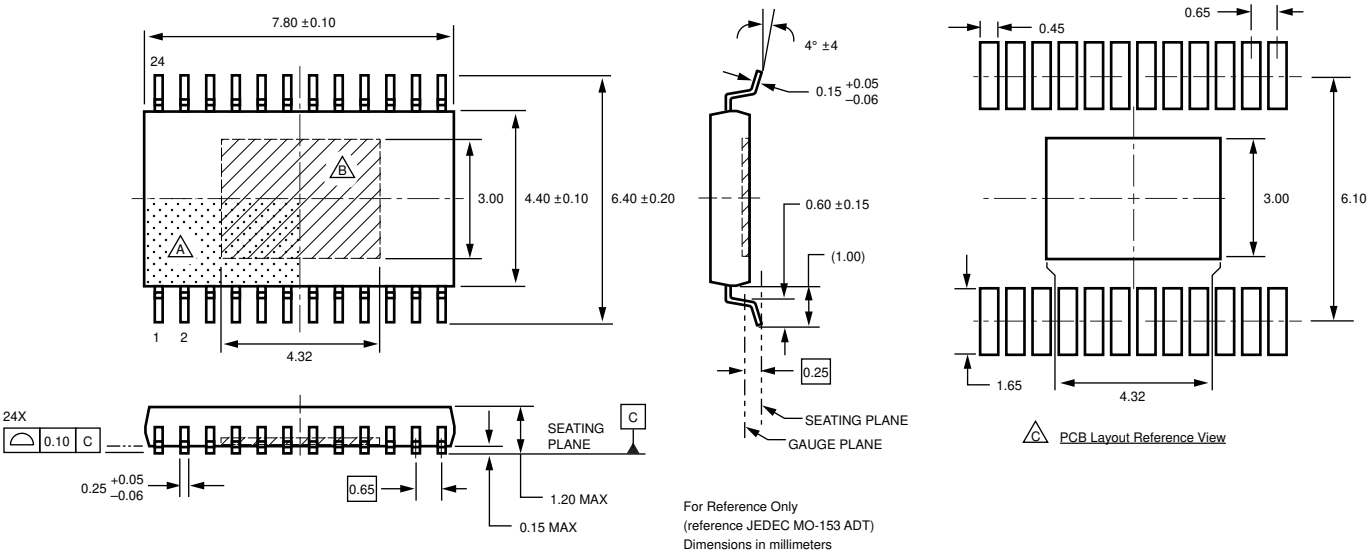
For Reference Only
(reference JEDEC MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LP, 24-pin TSSOP with Exposed Thermal Pad (A6279)



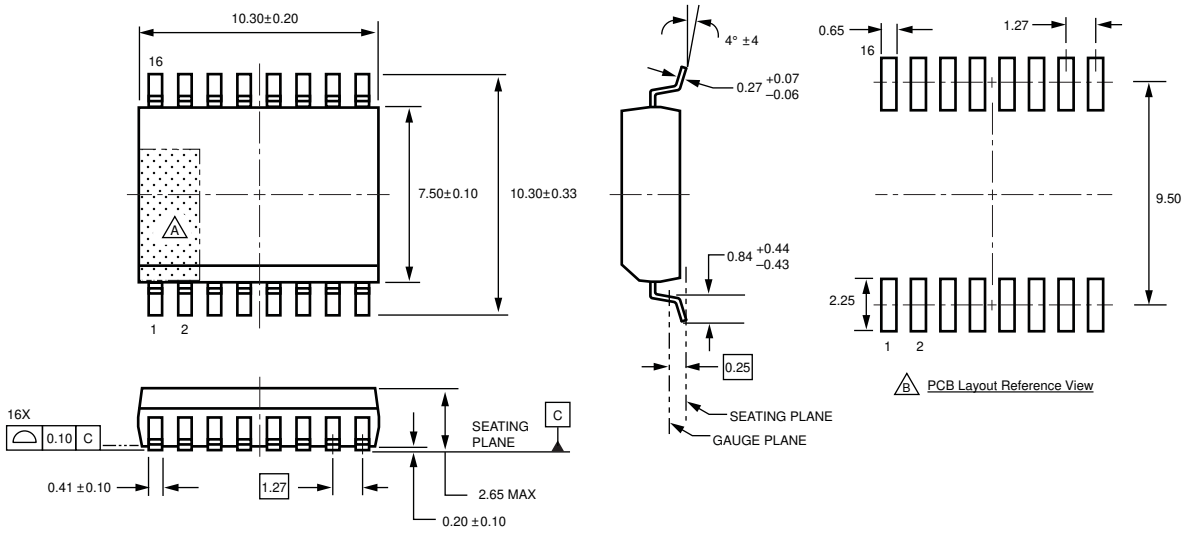
For Reference Only
(reference JEDEC MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LW, 16-pin SOIC (A6278)

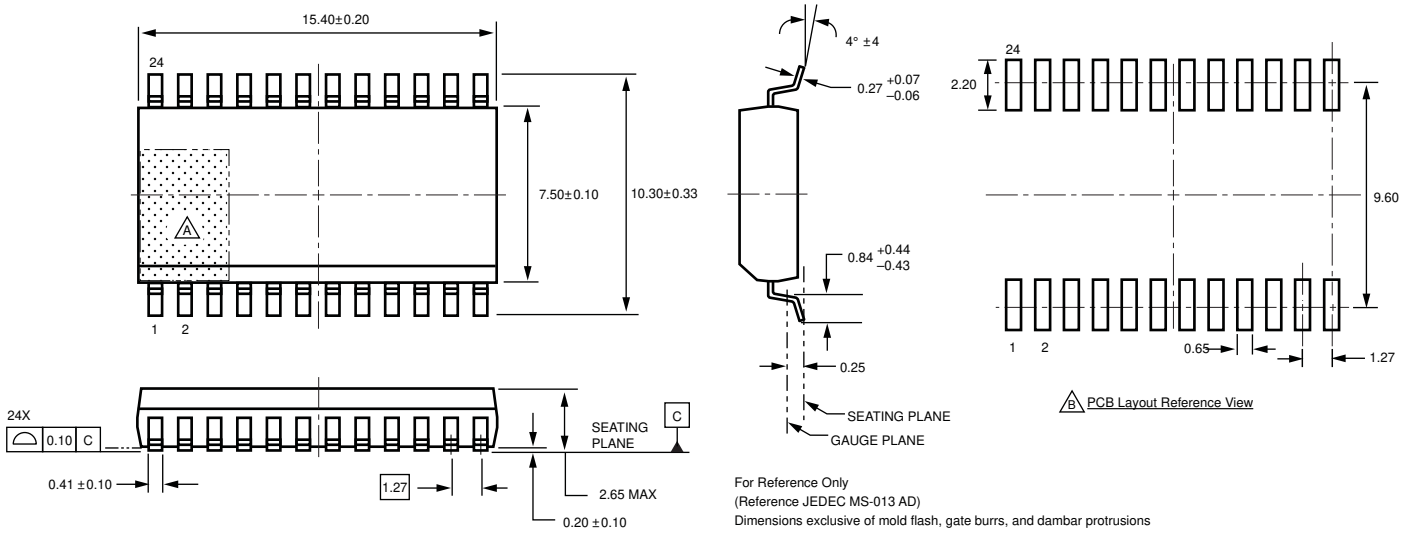


For Reference Only
Dimensions in millimeters
(reference JEDEC MS-013 AA)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-16M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Package LW, 24-pin SOIC (A6279)

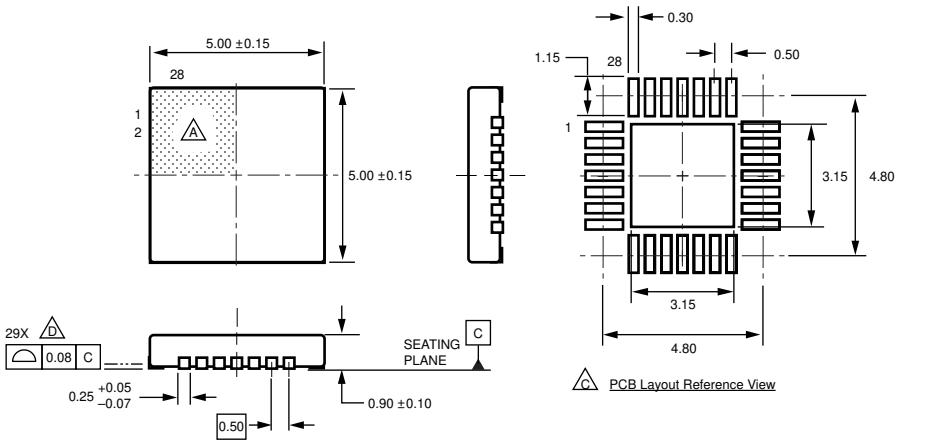


For Reference Only
(Reference JEDEC MS-013 AD)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Package ET, 28-pin MLPQ (A6279)



For Reference Only
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals