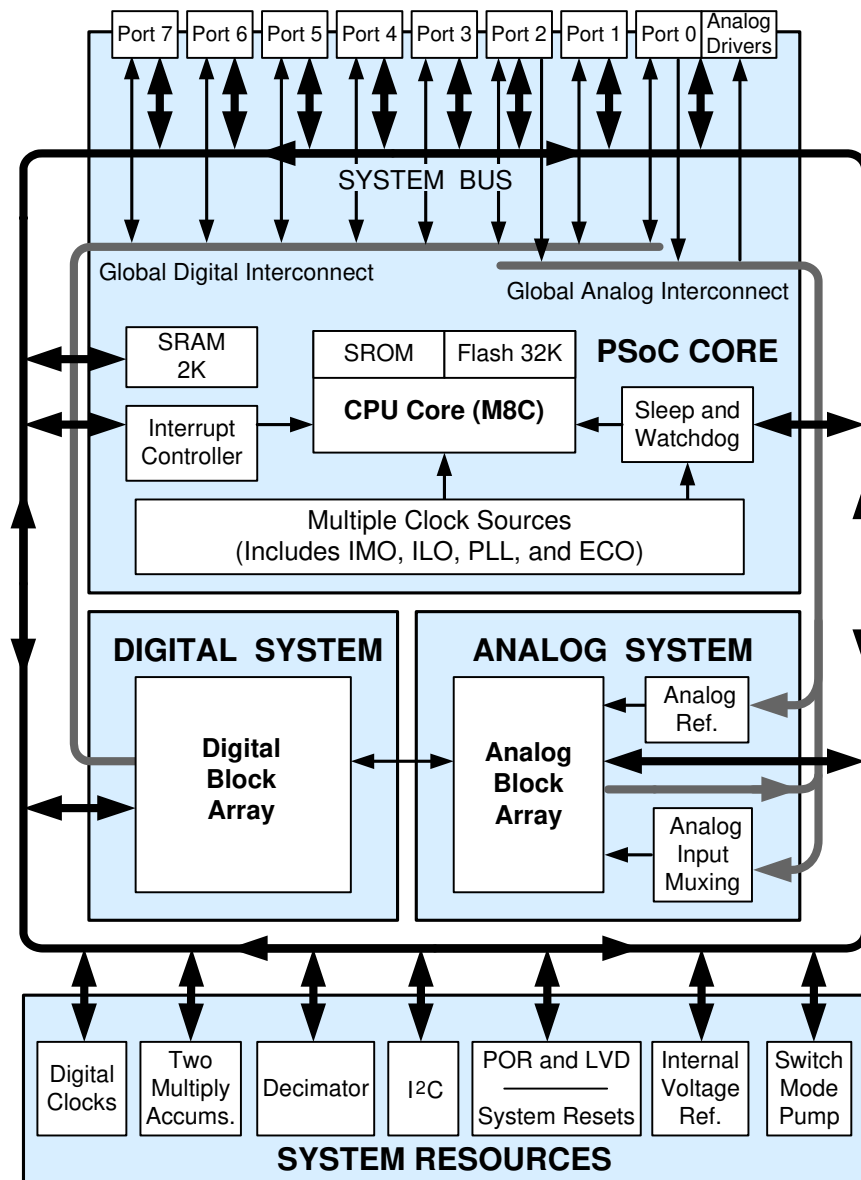


Features

- HB LED Controller
 - Configurable dimmers support up to 16 Independent LED channels
 - 8-to 32-bits of resolution per channel
 - Dynamic reconfiguration Enables LED controller Plus Other Features: CapSense®, battery charging, and motor control
- Visual embedded design
 - LED-based drivers
 - Binning compensation
 - Temperature feedback
 - Optical feedback
 - DMX512
- PrISM modulation technology™
 - Reduces radiated EMI
 - Reduces low frequency blinking
- Powerful Harvard-architecture Processor
 - M8C processor speeds to 24 MHz
 - 3.0 to 5.25 V operating voltage
 - Operating voltages down to 1.0 V using On-Chip switch mode pump (SMP)
 - Industrial temperature range: -40 °C to +85 °C
- Programmable pin configurations
 - 25 mA sink, 10 mA source on all GPIO
 - Pull-up, Pull-down, High Z, Strong, or Open Drain Drive Modes on all GPIO
 - Up to eight analog Inputs on GPIO
 - Configurable interrupt on all GPIO
- Advanced peripherals (PSoC® Blocks)
 - 16 Digital PSoC Blocks Provide:
 - 8-to 32-bit timers, counters, and PWMs
 - Up to 4 Full-Duplex UARTs
 - Multiple SPI masters or slaves
 - Connectable to all GPIO Pins
 - 12 Rail-to-Rail Analog PSoC Blocks Provide:
 - Up to 14-Bit ADCs
 - Up to 9-Bit DACs
 - Programmable gain amplifiers
 - Programmable filters and comparators
 - Complex peripherals by combining blocks
- Flexible on-chip memory
 - 32K flash program storage 50,000 Erase/Write Cycles
 - 2K SRAM Data Storage
 - In-system serial programming (ISSP)
 - Partial flash updates
 - Flexible Protection Modes
 - electrically erasable programmable read-only memory (EEPROM) emulation in flash
- Complete development tools
 - Free development software
 - PSoC Designer™
 - Full-featured, In-circuit emulator and programmer
 - Full speed emulation
 - Complex breakpoint structure
 - 128 KB trace memory

Logic Block Diagram



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EZ-Color™ Functional Overview

Cypress's EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of Programmable System-on-Chip (PSoC); with Cypress's precise illumination signal modulation (PrISM) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports a range of independent LED channels from 4 channels at 32 bits of resolution each, up to 16 channels at 8 bits of resolution each. This enables lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature, optical, and LED binning compensation. EZ-Color's virtually limitless analog and digital customization allow for simple integration of features in addition to intelligent lighting, such as Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress' best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

- LCD Backlight
- Large Signs
- General Lighting
- Architectural Lighting
- Camera/Cell Phone flash
- flashlights

The PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a central processing unit (CPU), memory, clocks, and configurable general purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 48 MHz, providing a four million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU utilizes an interrupt controller with 25 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and watchdog timers (WDT).

Memory encompasses 32 KB of flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The EZ-Color family incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also

be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low speed oscillator (ILO) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the EZ-Color device.

EZ-Color GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

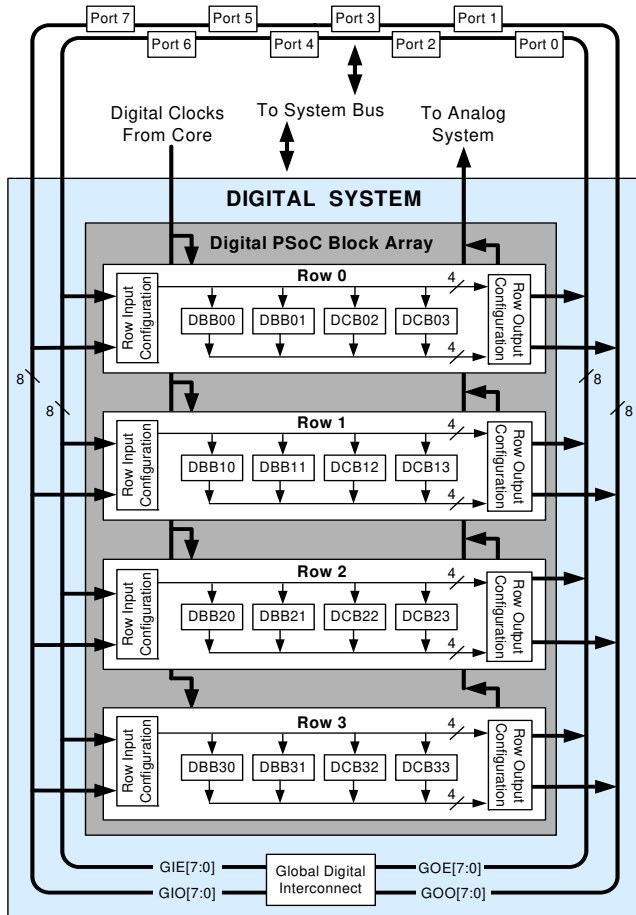
The digital system is composed of 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include those listed below.

- PrISM (8-to 32-bit)
- PWMs (8-to 32-bit)
- PWMs with Dead band (8-to 32-bit)
- Counters (8-to 32-bit)
- Timers (8-to 32-bit)
- UART 8 bit with selectable parity (up to 4)
- SPI master and slave (up to 4 each)
- I²C slave and multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8- to 32-bit)
- IrDA (up to 4)
- Generators (8-to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by EZ-Color device family. This allows you the optimum choice of system resources for your application. Family resources are shown in [Table 1](#) on page 6.

Figure 1. Digital System Block Diagram



The Analog System

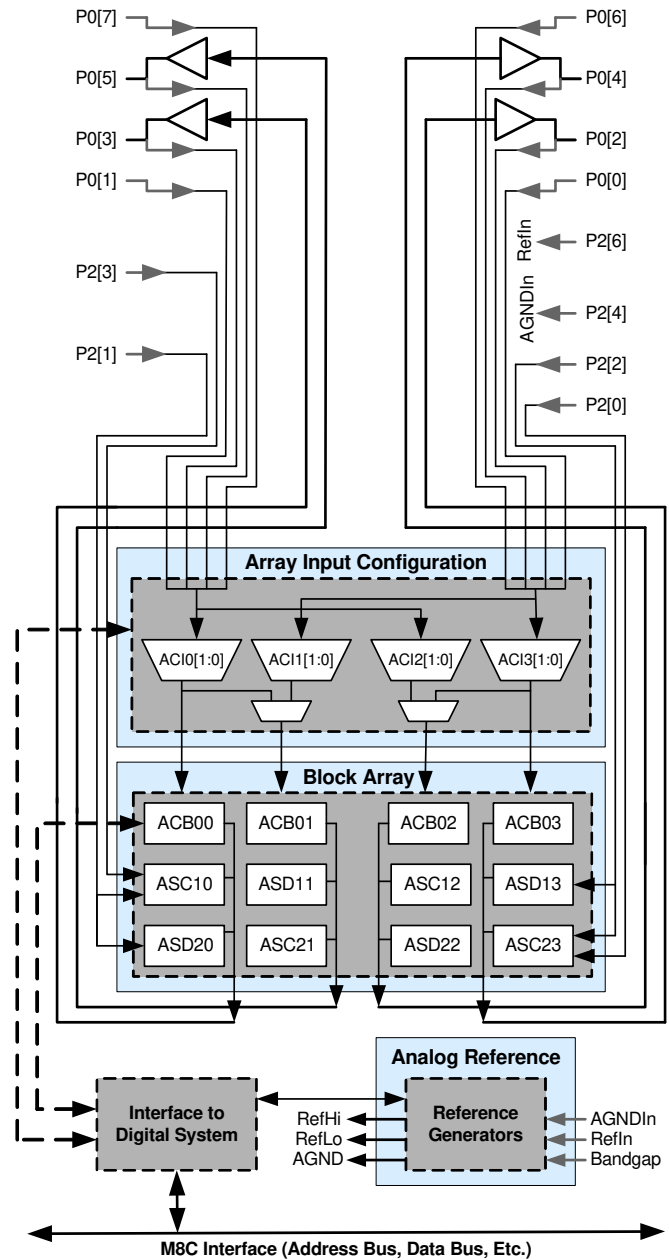
The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 40 mA drive as a core resource)
- 1.3 V reference (as a System resource)

- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in the figure below.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Resources include a multiplier, decimator, switch mode pump, low-voltage detection, and power-onreset (POR). Statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.

- The decimator provides a custom hardware filter for digital signal, processing applications including the creation of Delta Sigma ADCs.
- The I²C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-voltage-detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch-mode pump (SMP) generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1. EZ-Color Device Characteristics

| Part Number | LED Channels | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size | CapSense |
|-------------|--------------|-------------|--------------|----------------|---------------|----------------|----------------|---------------|-----------|------------|----------|
| CY8CLED02 | 2 | 16 | 1 | 4 | 8 | 0 | 2 | 4 | 256 Bytes | 4K | No |
| CY8CLED04 | 4 | 56 | 1 | 4 | 48 | 2 | 2 | 6 | 1K | 16K | Yes |
| CY8CLED08 | 8 | 44 | 2 | 8 | 12 | 4 | 4 | 12 | 256 Bytes | 16K | No |
| CY8CLED16 | 16 | 44 | 4 | 16 | 12 | 4 | 4 | 12 | 2K | 32K | No |

Getting Started

The quickest way to understand the device is to read this data sheet and then use the PSoC Designer Integrated development environment (IDE). This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, see the Technical Reference Manual for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest device data sheets on the web at <http://www.cypress.com>.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse with modulator (PWM) user module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes

the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip-Level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Information

Pinouts

The CY8CLED16 device is available in three packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

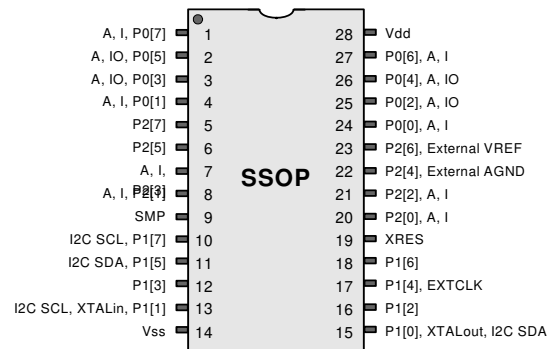
28-Pin Part Pinout

Table 2. 28-Pin Part Pinout (SSOP)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I | P0[7] | Analog column mux input. |
| 2 | I/O | I/O | P0[5] | Analog column mux input and column output. |
| 3 | I/O | I/O | P0[3] | Analog column mux input and column output. |
| 4 | I/O | I | P0[1] | Analog column mux input. |
| 5 | I/O | | P2[7] | |
| 6 | I/O | | P2[5] | |
| 7 | I/O | I | P2[3] | Direct switched capacitor block input. |
| 8 | I/O | I | P2[1] | Direct switched capacitor block input. |
| 9 | Power | | SMP | Switch mode pump (SMP) connection to external components required. |
| 10 | I/O | | P1[7] | I ² C serial clock (SCL). |
| 11 | I/O | | P1[5] | I ² C serial data (SDA). |
| 12 | I/O | | P1[3] | |
| 13 | I/O | | P1[1] | Crystal (XTALin), I ² C serial clock (SCL), ISSP-SCLK ¹ . |
| 14 | Power | | V _{SS} | Ground connection. |
| 15 | I/O | | P1[0] | Crystal (XTALout), I ² C serial data (SDA), ISSP-SDATA ¹ . |
| 16 | I/O | | P1[2] | |
| 17 | I/O | | P1[4] | optional external clock input (EXTCLK). |
| 18 | I/O | | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull-down. |
| 20 | I/O | I | P2[0] | Direct switched capacitor block input. |
| 21 | I/O | I | P2[2] | Direct switched capacitor block input. |
| 22 | I/O | | P2[4] | External analog ground (AGND). |
| 23 | I/O | | P2[6] | External voltage reference (VREF). |
| 24 | I/O | I | P0[0] | Analog column mux input. |
| 25 | I/O | I/O | P0[2] | Analog column mux input and column output. |
| 26 | I/O | I/O | P0[4] | Analog column mux input and column output. |
| 27 | I/O | I | P0[6] | Analog column mux input. |
| 28 | Power | | V _{DD} | Supply voltage. |

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. 28-Pin Device



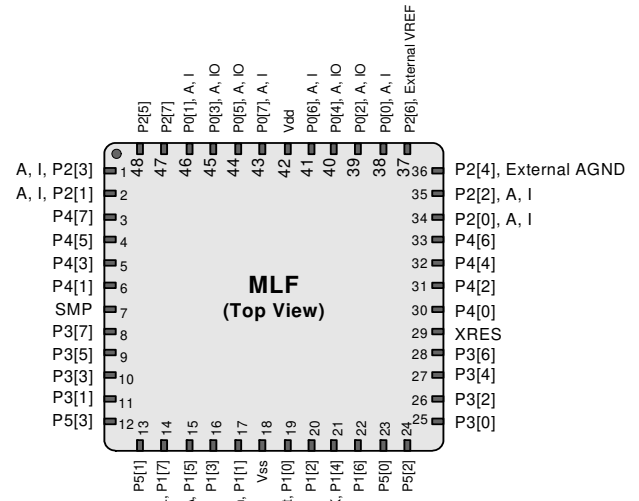
Note

1. These are the ISSP pins, which are not High Z at POR.

Table 3. 48-Pin Part Pinout (QFN)^[2]

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I | P2[3] | Direct switched capacitor block input. |
| 2 | I/O | I | P2[1] | Direct switched capacitor block input. |
| 3 | I/O | | P4[7] | |
| 4 | I/O | | P4[5] | |
| 5 | I/O | | P4[3] | |
| 6 | I/O | | P4[1] | |
| 7 | Power | | SMP | Switch mode pump (SMP) connection to external components required. |
| 8 | I/O | | P3[7] | |
| 9 | I/O | | P3[5] | |
| 10 | I/O | | P3[3] | |
| 11 | I/O | | P3[1] | |
| 12 | I/O | | P5[3] | |
| 13 | I/O | | P5[1] | |
| 14 | I/O | | P1[7] | I ² C serial clock (SCL). |
| 15 | I/O | | P1[5] | I ² C serial data (SDA). |
| 16 | I/O | | P1[3] | |
| 17 | I/O | | P1[1] | Crystal (XTALin), I ² C serial clock (SCL), ISSP-SCLK ^[1] . |
| 18 | Power | | Vss | Ground connection. |
| 19 | I/O | | P1[0] | Crystal (XTALout), I ² C serial data (SDA), ISSP-SDATA ^[1] . |
| 20 | I/O | | P1[2] | |
| 21 | I/O | | P1[4] | optional external clock input (EXTCLK). |
| 22 | I/O | | P1[6] | |
| 23 | I/O | | P5[0] | |
| 24 | I/O | | P5[2] | |
| 25 | I/O | | P3[0] | |
| 26 | I/O | | P3[2] | |
| 27 | I/O | | P3[4] | |
| 28 | I/O | | P3[6] | |
| 29 | Input | | XRES | Active high external reset with internal pull-down. |
| 30 | I/O | | P4[0] | |
| 31 | I/O | | P4[2] | |
| 32 | I/O | | P4[4] | |
| 33 | I/O | | P4[6] | |
| 34 | I/O | I | P2[0] | Direct switched capacitor block input. |
| 35 | I/O | I | P2[2] | Direct switched capacitor block input. |
| 36 | I/O | | P2[4] | external analog ground (AGND). |
| 37 | I/O | | P2[6] | external voltage reference (VREF). |
| 38 | I/O | I | P0[0] | Analog column mux input. |
| 39 | I/O | I/O | P0[2] | Analog column mux input and column output. |
| 40 | I/O | I/O | P0[4] | Analog column mux input and column output. |
| 41 | I/O | I | P0[6] | Analog column mux input. |
| 42 | Power | | V _{DD} | Supply voltage. |
| 43 | I/O | I | P0[7] | Analog column mux input. |
| 44 | I/O | I/O | P0[5] | Analog column mux input and column output. |
| 45 | I/O | I/O | P0[3] | Analog column mux input and column output. |
| 46 | I/O | I | P0[1] | Analog column mux input. |
| 47 | I/O | | P2[7] | |
| 48 | I/O | | P2[5] | |

Figure 4. 48-Pin Device



LEGEND: A = Analog, I = Input, and O = Output.

Note

- The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Register Reference

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|------------|------------------------------|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

This chapter lists the registers of the CY8CLED16 EZ-Color device.

The device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 4. Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|----------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DR | 00 | RW | DBB20DR0 | 40 | # | ASC10CR0 | 80 | RW | RD12RI | C0 | RW |
| PRT0IE | 01 | RW | DBB20DR1 | 41 | W | ASC10CR1 | 81 | RW | RD12SYN | C1 | RW |
| PRT0GS | 02 | RW | DBB20DR2 | 42 | RW | ASC10CR2 | 82 | RW | RD12IS | C2 | RW |
| PRT0DM2 | 03 | RW | DBB20CR0 | 43 | # | ASC10CR3 | 83 | RW | RD12LT0 | C3 | RW |
| PRT1DR | 04 | RW | DBB21DR0 | 44 | # | ASD11CR0 | 84 | RW | RD12LT1 | C4 | RW |
| PRT1IE | 05 | RW | DBB21DR1 | 45 | W | ASD11CR1 | 85 | RW | RD12RO0 | C5 | RW |
| PRT1GS | 06 | RW | DBB21DR2 | 46 | RW | ASD11CR2 | 86 | RW | RD12RO1 | C6 | RW |
| PRT1DM2 | 07 | RW | DBB21CR0 | 47 | # | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | DCB22DR0 | 48 | # | ASC12CR0 | 88 | RW | RD13RI | C8 | RW |
| PRT2IE | 09 | RW | DCB22DR1 | 49 | W | ASC12CR1 | 89 | RW | RD13SYN | C9 | RW |
| PRT2GS | 0A | RW | DCB22DR2 | 4A | RW | ASC12CR2 | 8A | RW | RD13IS | CA | RW |
| PRT2DM2 | 0B | RW | DCB22CR0 | 4B | # | ASC12CR3 | 8B | RW | RD13LT0 | CB | RW |
| PRT3DR | 0C | RW | DCB23DR0 | 4C | # | ASD13CR0 | 8C | RW | RD13LT1 | CC | RW |
| PRT3IE | 0D | RW | DCB23DR1 | 4D | W | ASD13CR1 | 8D | RW | RD13RO0 | CD | RW |
| PRT3GS | 0E | RW | DCB23DR2 | 4E | RW | ASD13CR2 | 8E | RW | RD13RO1 | CE | RW |
| PRT3DM2 | 0F | RW | DCB23CR0 | 4F | # | ASD13CR3 | 8F | RW | | CF | |
| PRT4DR | 10 | RW | DBB30DR0 | 50 | # | ASD20CR0 | 90 | RW | CUR_PP | D0 | RW |
| PRT4IE | 11 | RW | DBB30DR1 | 51 | W | ASD20CR1 | 91 | RW | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | DBB30DR2 | 52 | RW | ASD20CR2 | 92 | RW | | D2 | |
| PRT4DM2 | 13 | RW | DBB30CR0 | 53 | # | ASD20CR3 | 93 | RW | IDX_PP | D3 | RW |
| PRT5DR | 14 | RW | DBB31DR0 | 54 | # | ASC21CR0 | 94 | RW | MVR_PP | D4 | RW |
| PRT5IE | 15 | RW | DBB31DR1 | 55 | W | ASC21CR1 | 95 | RW | MVW_PP | D5 | RW |
| PRT5GS | 16 | RW | DBB31DR2 | 56 | RW | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| PRT5DM2 | 17 | RW | DBB31CR0 | 57 | # | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| PRT6DR | 18 | RW | DCB32DR0 | 58 | # | ASD22CR0 | 98 | RW | I2C_DR | D8 | RW |
| PRT6IE | 19 | RW | DCB32DR1 | 59 | W | ASD22CR1 | 99 | RW | I2C_MSCR | D9 | # |
| PRT6GS | 1A | RW | DCB32DR2 | 5A | RW | ASD22CR2 | 9A | RW | INT_CLR0 | DA | RW |
| PRT6DM2 | 1B | RW | DCB32CR0 | 5B | # | ASD22CR3 | 9B | RW | INT_CLR1 | DB | RW |
| PRT7DR | 1C | RW | DCB33DR0 | 5C | # | ASC23CR0 | 9C | RW | INT_CLR2 | DC | RW |
| PRT7IE | 1D | RW | DCB33DR1 | 5D | W | ASC23CR1 | 9D | RW | INT_CLR3 | DD | RW |
| PRT7GS | 1E | RW | DCB33DR2 | 5E | RW | ASC23CR2 | 9E | RW | INT_MSK3 | DE | RW |
| PRT7DM2 | 1F | RW | DCB33CR0 | 5F | # | ASC23CR3 | 9F | RW | INT_MSK2 | DF | RW |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | MUL1_X | A8 | W | MUL0_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | MUL1_Y | A9 | W | MUL0_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | MUL1_DH | AA | R | MUL0_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | MUL1_DL | AB | R | MUL0_DL | EB | R |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | ACC1_DR1 | AC | RW | ACC0_DR1 | EC | RW |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | ACC1_DR0 | AD | RW | ACC0_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | ACC1_DR3 | AE | RW | ACC0_DR3 | EE | RW |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | ACC1_DR2 | AF | RW | ACC0_DR2 | EF | RW |
| DBB10DR0 | 30 | # | ACB00CR3 | 70 | RW | RD10RI | B0 | RW | | F0 | |
| DBB10DR1 | 31 | W | ACB00CR0 | 71 | RW | RD10SYN | B1 | RW | | F1 | |
| DBB10DR2 | 32 | RW | ACB00CR1 | 72 | RW | RD10IS | B2 | RW | | F2 | |
| DBB10CR0 | 33 | # | ACB00CR2 | 73 | RW | RD10LT0 | B3 | RW | | F3 | |
| DBB11DR0 | 34 | # | ACB01CR3 | 74 | RW | RD10LT1 | B4 | RW | | F4 | |
| DBB11DR1 | 35 | W | ACB01CR0 | 75 | RW | RD10RO0 | B5 | RW | | F5 | |
| DBB11DR2 | 36 | RW | ACB01CR1 | 76 | RW | RD10RO1 | B6 | RW | | F6 | |
| DBB11CR0 | 37 | # | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12DR0 | 38 | # | ACB02CR3 | 78 | RW | RD11RI | B8 | RW | | F8 | |
| DCB12DR1 | 39 | W | ACB02CR0 | 79 | RW | RD11SYN | B9 | RW | | F9 | |
| DCB12DR2 | 3A | RW | ACB02CR1 | 7A | RW | RD11IS | BA | RW | | FA | |
| DCB12CR0 | 3B | # | ACB02CR2 | 7B | RW | RD11LT0 | BB | RW | | FB | |
| DCB13DR0 | 3C | # | ACB03CR3 | 7C | RW | RD11LT1 | BC | RW | | FC | |
| DCB13DR1 | 3D | W | ACB03CR0 | 7D | RW | RD11RO0 | BD | RW | | FD | |
| DCB13DR2 | 3E | RW | ACB03CR1 | 7E | RW | RD11RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCB13CR0 | 3F | # | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

Blank fields are reserved and should not be accessed.

Access is bit specific.

Table 5. Register Map Bank 1 Table: Configuration Space

| Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access |
|---------|-------------|--------|----------|-------------|--------|----------|-------------|--------|-----------|-------------|--------|
| PRT0DM0 | 00 | RW | DBB20FN | 40 | RW | ASC10CR0 | 80 | RW | RD12RI | C0 | RW |
| PRT0DM1 | 01 | RW | DBB20IN | 41 | RW | ASC10CR1 | 81 | RW | RD12SYN | C1 | RW |
| PRT0IC0 | 02 | RW | DBB20OU | 42 | RW | ASC10CR2 | 82 | RW | RD12IS | C2 | RW |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | RD12LT0 | C3 | RW |
| PRT1DM0 | 04 | RW | DBB21FN | 44 | RW | ASD11CR0 | 84 | RW | RD12LT1 | C4 | RW |
| PRT1DM1 | 05 | RW | DBB21IN | 45 | RW | ASD11CR1 | 85 | RW | RD12RO0 | C5 | RW |
| PRT1IC0 | 06 | RW | DBB21OU | 46 | RW | ASD11CR2 | 86 | RW | RD12RO1 | C6 | RW |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DM0 | 08 | RW | DCB22FN | 48 | RW | ASC12CR0 | 88 | RW | RD13RI | C8 | RW |
| PRT2DM1 | 09 | RW | DCB22IN | 49 | RW | ASC12CR1 | 89 | RW | RD13SYN | C9 | RW |
| PRT2IC0 | 0A | RW | DCB22OU | 4A | RW | ASC12CR2 | 8A | RW | RD13IS | CA | RW |
| PRT2IC1 | 0B | RW | | 4B | | ASC12CR3 | 8B | RW | RD13LT0 | CB | RW |
| PRT3DM0 | 0C | RW | DCB23FN | 4C | RW | ASD13CR0 | 8C | RW | RD13LT1 | CC | RW |
| PRT3DM1 | 0D | RW | DCB23IN | 4D | RW | ASD13CR1 | 8D | RW | RD13RO0 | CD | RW |
| PRT3IC0 | 0E | RW | DCB23OU | 4E | RW | ASD13CR2 | 8E | RW | RD13RO1 | CE | RW |
| PRT3IC1 | 0F | RW | | 4F | | ASD13CR3 | 8F | RW | | CF | |
| PRT4DM0 | 10 | RW | DBB30FN | 50 | RW | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | DBB30IN | 51 | RW | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | DBB30OU | 52 | RW | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| PRT5DM0 | 14 | RW | DBB31FN | 54 | RW | ASC21CR0 | 94 | RW | | D4 | |
| PRT5DM1 | 15 | RW | DBB31IN | 55 | RW | ASC21CR1 | 95 | RW | | D5 | |
| PRT5IC0 | 16 | RW | DBB31OU | 56 | RW | ASC21CR2 | 96 | RW | | D6 | |
| PRT5IC1 | 17 | RW | | 57 | | ASC21CR3 | 97 | RW | | D7 | |
| PRT6DM0 | 18 | RW | DCB32FN | 58 | RW | ASD22CR0 | 98 | RW | | D8 | |
| PRT6DM1 | 19 | RW | DCB32IN | 59 | RW | ASD22CR1 | 99 | RW | | D9 | |
| PRT6IC0 | 1A | RW | DCB32OU | 5A | RW | ASD22CR2 | 9A | RW | | DA | |
| PRT6IC1 | 1B | RW | | 5B | | ASD22CR3 | 9B | RW | | DB | |
| PRT7DM0 | 1C | RW | DCB33FN | 5C | RW | ASC23CR0 | 9C | RW | | DC | |
| PRT7DM1 | 1D | RW | DCB33IN | 5D | RW | ASC23CR1 | 9D | RW | OSC_GO_EN | DD | RW |
| PRT7IC0 | 1E | RW | DCB33OU | 5E | RW | ASC23CR2 | 9E | RW | OSC_CR4 | DE | RW |
| PRT7IC1 | 1F | RW | | 5F | | ASC23CR3 | 9F | RW | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | DEC_CR2 | E7 | RW |
| DCB02FN | 28 | RW | ALT_CR1 | 68 | RW | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | CLK_CR2 | 69 | RW | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| DBB10FN | 30 | RW | ACB00CR3 | 70 | RW | RD10RI | B0 | RW | | F0 | |
| DBB10IN | 31 | RW | ACB00CR0 | 71 | RW | RD10SYN | B1 | RW | | F1 | |
| DBB10OU | 32 | RW | ACB00CR1 | 72 | RW | RD10IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RD10LT0 | B3 | RW | | F3 | |
| DBB11FN | 34 | RW | ACB01CR3 | 74 | RW | RD10LT1 | B4 | RW | | F4 | |
| DBB11IN | 35 | RW | ACB01CR0 | 75 | RW | RD10RO0 | B5 | RW | | F5 | |
| DBB11OU | 36 | RW | ACB01CR1 | 76 | RW | RD10RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12FN | 38 | RW | ACB02CR3 | 78 | RW | RD11RI | B8 | RW | | F8 | |
| DCB12IN | 39 | RW | ACB02CR0 | 79 | RW | RD11SYN | B9 | RW | | F9 | |
| DCB12OU | 3A | RW | ACB02CR1 | 7A | RW | RD11IS | BA | RW | FLS_PR1 | FA | RW |
| | 3B | | ACB02CR2 | 7B | RW | RD11LT0 | BB | RW | | FB | |
| DCB13FN | 3C | RW | ACB03CR3 | 7C | RW | RD11LT1 | BC | RW | | FC | |
| DCB13IN | 3D | RW | ACB03CR0 | 7D | RW | RD11RO0 | BD | RW | | FD | |
| DCB13OU | 3E | RW | ACB03CR1 | 7E | RW | RD11RO1 | BE | RW | CPU_SCR1 | FE | # |
| | 3F | | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

Blank fields are reserved and should not be accessed.

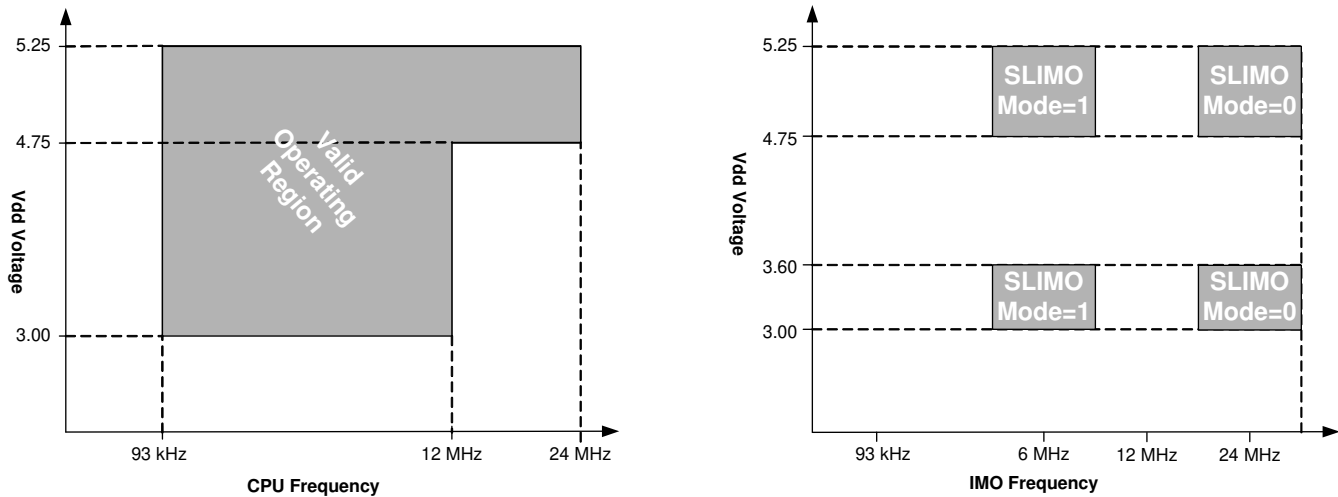
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED16 EZ-Color device. For the most up-to-date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Refer to Table 20 for the electrical specifications for the internal main oscillator (IMO) using SLIMO mode.

Figure 5. Voltage versus CPU Frequency, and IMO Frequency Trim Options



Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|---|-----------------------|-----|-----------------------|-------|---|
| T _{STG} | Storage temperature | -55 | 25 | +100 | °C | Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability. |
| T _{BAKETEMP} | Bake temperature | - | 125 | See package label | °C | |
| T _{BAKETIME} | Bake time | See package label | - | 72 | Hours | |
| T _A | Ambient temperature with power applied | -40 | - | +85 | °C | |
| V _{DD} | Supply voltage on V _{DD} relative to V _{SS} | -0.5 | - | +6.0 | V | |
| V _{IO} | DC input voltage | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V | |
| V _{IOZ} | DC Voltage applied to Tri-state | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V | |
| I _{MIO} | Maximum current into any port pin | -25 | - | +50 | mA | |
| I _{MAIO} | Maximum current into any port pin configured as analog driver | -50 | - | +50 | mA | |
| ESD | Electro static discharge voltage | 2000 | - | - | V | Human body model ESD. |
| LU | Latch up current | - | - | 200 | mA | |

Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|----------------------|-----|-----|------|-------|---|
| T _A | Ambient temperature | -0 | - | +85 | °C | |
| T _J | Junction temperature | -0 | - | +100 | °C | The temperature rise from ambient to junction is package specific. See Thermal Impedances per Package on page 42 . The user must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics
DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 6. DC Chip Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|------|-----|------|-------|--|
| V _{DD} | Supply voltage | 3.00 | – | 5.25 | V | See DC POR and LVD specifications, Table 3-15 on page 27. |
| I _{DD} | Supply current | – | 8 | 14 | mA | Conditions are 5.0 V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. |
| I _{DD3} | Supply current | – | 5 | 9 | mA | Conditions are V _{DD} = 3.3 V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. |
| I _{DDP} | Supply current when IMO = 6 MHz using SLIMO mode. | – | 2 | 3 | mA | Conditions are V _{DD} = 3.3 V, T _A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz. |
| I _{SB} | Sleep (Mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 3 | 10 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3 V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$. |
| I _{SBH} | Sleep (Mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 4 | 25 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3 V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$. |
| I _{SBXTL} | Sleep (Mode) current with POR, LVD, Sleep Timer, WDT, internal slow oscillator, and 32 kHz crystal oscillator active. | – | 4 | 12 | μA | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3 V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$. |
| I _{SBXTLH} | Sleep (Mode) current with POR, LVD, sleep timer, WDT, and 32 kHz crystal oscillator active. | – | 5 | 27 | μA | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3 V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$. |
| V _{REF} | Reference voltage (Bandgap) | 1.28 | 1.3 | 1.32 | V | Trimmed for appropriate V _{DD} . |

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|---|
| R _{PU} | Pull-up Resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull-down Resistor | 4 | 5.6 | 8 | kΩ | |
| V _{OH} | High output level | V _{DD} - 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget. |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I _{OL} budget. |
| I _{OH} | High level source current | 10 | – | – | mA | V _{OH} = V _{DD} - 1.0 V. See the limitations of the total current in the Note for V _{OH} . |
| I _{OL} | Low level sink current | 25 | – | – | mA | V _{OL} = 0.75 V. See the limitations of the total current in the Note for V _{OL} . |
| V _{IL} | Input low level | – | – | 0.8 | V | V _{DD} = 3.0 to 5.25. |
| V _{IH} | Input high level | 2.1 | – | – | V | V _{DD} = 3.0 to 5.25. |
| V _H | Input hysteresis | – | 60 | – | mV | |
| I _{IL} | Input leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 μA. |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the Analog Continuous Time PSoC blocks and the analog switched capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 8. 5-V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|----------------------|---|------------------------|------|-----------------------|-------|--|
| V _{OSOA} | Input offset voltage (absolute value) | | | | | – |
| | Power = Low, Opamp bias = Low | – | 1.6 | 10 | mV | |
| | Power = Low, Opamp bias = High | – | 1.6 | 10 | mV | |
| | Power = Medium, Opamp bias = Low | – | 1.6 | 10 | mV | |
| | Power = Medium, Opamp bias = High | – | 1.6 | 10 | mV | |
| | Power = High, Opamp bias = Low | – | 1.6 | 10 | mV | |
| | Power = High, Opamp bias = High | – | 1.6 | 10 | mV | |
| TCV _{OSOA} | Average input offset voltage drift | – | 4 | 23 | μV/°C | |
| I _{EBOA} | Input leakage current (port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 μA |
| C _{INOA} | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| V _{CMOA} | Common mode voltage range (All cases, except Power = High, Opamp bias = High) | 0 | – | V _{DD} | V | The common-mode input voltage range is measured through an analog output buffer. |
| | Common mode voltage range (Power = High, Opamp bias = High) | 0.5 | – | V _{DD} – 0.5 | V | The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| CMRROA | Common mode rejection ratio | 60 | – | – | dB | – |
| GOLOA | Open loop gain | 80 | – | – | dB | – |
| V _{OHIGHOA} | High output voltage swing (internal signals) | V _{DD} – 0.01 | – | – | V | – |
| V _{OLOWOA} | Low output voltage swing (internal signals) | – | – | 0.1 | V | – |
| I _{SOA} | Supply current (including associated AGND buffer) | | | | | – |
| | Power = Low, Opamp bias = Low | – | 150 | 200 | μA | |
| | Power = Low, Opamp bias = High | – | 300 | 400 | μA | |
| | Power = Medium, Opamp bias = Low | – | 600 | 800 | μA | |
| | Power = Medium, Opamp bias = High | – | 1200 | 1600 | μA | |
| | Power = High, Opamp bias = Low | – | 2400 | 3200 | μA | |
| | Power = High, Opamp bias = High | – | 4600 | 6400 | μA | |
| PSRR _{OA} | Supply voltage rejection ratio | 67 | 80 | – | dB | V _{SS} ≤ V _{IN} ≤ (V _{DD} – 2.25) or (V _{DD} – 1.25 V) ≤ V _{IN} ≤ V _{DD} . |

Table 9. 3.3-V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---------------------------------|---|------------------------|------|-----------------|-------|--|
| V _{OSOA} | Input offset voltage (absolute value) | – | 1.4 | 10 | mV | Power = High, Opamp bias = High setting is not allowed for 3.3 V V _{DD} operation. |
| | Power = Low, Opamp bias = Low | – | 1.4 | 10 | mV | |
| | Power = Low, Opamp bias = High | – | 1.4 | 10 | mV | |
| | Power = Medium, Opamp bias = Low | – | 1.4 | 10 | mV | |
| | Power = Medium, Opamp bias = High | – | 1.4 | 10 | mV | |
| | Power = High, Opamp bias = Low | – | 1.4 | 10 | mV | |
| Power = High, Opamp bias = High | – | – | – | – | mV | |
| TCV _{OSOA} | Average input offset voltage drift | – | 7 | 40 | μV/°C | – |
| I _{EBOA} | Input leakage current (port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 μA. |
| C _{INOA} | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| V _{CMOA} | Common mode voltage range | 0 | – | V _{DD} | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| CMRR _{OA} | Common mode rejection ratio | 60 | – | – | dB | – |
| G _{OLOA} | Open loop gain | 80 | – | – | dB | – |
| V _{OHIGHOA} | High output voltage swing (internal signals) | V _{DD} – 0.01 | – | – | V | – |
| V _{OLOWOA} | Low output voltage swing (internal signals) | – | – | 0.01 | V | – |
| I _{SOA} | Supply current (including associated AGND buffer) | – | – | – | – | Power = High, Opamp bias = High setting is not allowed for 3.3 V V _{DD} operation. |
| | Power = Low, Opamp bias = Low | – | 150 | 200 | μA | |
| | Power = Low, Opamp bias = High | – | 300 | 400 | μA | |
| | Power = Medium, Opamp bias = Low | – | 600 | 800 | μA | |
| | Power = Medium, Opamp bias = High | – | 1200 | 1600 | μA | |
| | Power = High, Opamp bias = Low | – | 2400 | 3200 | μA | |
| Power = High, Opamp bias = High | – | – | – | – | μA | |
| PSRR _{OA} | Supply voltage rejection ratio | 54 | 80 | – | dB | V _{SS} ≤ V _{IN} ≤ (V _{DD} – 2.25) or (V _{DD} – 1.25 V) ≤ V _{IN} ≤ V _{DD} |

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 10. DC Low Power Comparator Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-----|-----|---------------------|-------|-------|
| V _{REFLPC} | Low power comparator (LPC) reference voltage range | 0.2 | – | V _{DD} – 1 | V | – |
| I _{SLPC} | LPC supply current | – | 10 | 40 | μA | – |
| V _{OSSLPC} | LPC voltage offset | – | 2.5 | 30 | mV | – |

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 11. 5-V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|----------------------|---|-----------------------------|-----|-----------------------------|-------|--|
| V _{OSOB} | Input offset voltage (absolute value) | | | | | |
| | Power = Low, Opamp bias = Low | – | 3.2 | 18 | mV | – |
| | Power = Low, Opamp bias = High | – | 3.2 | 18 | mV | – |
| | Power = High, Opamp bias = Low | – | 3.2 | 18 | mV | – |
| | Power = High, Opamp bias = High | – | 3.2 | 18 | mV | – |
| TCV _{OSOB} | Average input offset voltage drift | – | 5.5 | 26 | μV/°C | – |
| V _{CMOB} | Common-mode input voltage range | 0.5 | – | V _{DD} – 1.0 | V | – |
| R _{OUTOB} | Output resistance | | | | | |
| | Power = Low | – | – | 1 | Ω | – |
| | Power = High | – | – | 1 | Ω | – |
| V _{OHIGHOB} | High output voltage swing (Load = 32 ohms to V _{DD} /2) | | | | | |
| | Power = Low | 0.5 × V _{DD} + 1.3 | – | – | V | – |
| | Power = High | 0.5 × V _{DD} + 1.3 | – | – | V | – |
| V _{LOWOB} | Low output voltage swing (Load = 32 ohms to V _{DD} /2) | | | | | |
| | Power = Low | – | – | 0.5 × V _{DD} – 1.3 | V | – |
| | Power = High | – | – | 0.5 × V _{DD} – 1.3 | V | – |
| I _{SOB} | Supply current including bias cell (no load) | | | | | |
| | Power = Low | – | 1.1 | 2 | mA | – |
| | Power = High | – | 2.6 | 5 | mA | – |
| PSRR _{OB} | Supply voltage rejection ratio | 40 | 64 | | dB | – |
| C _L | Load capacitance | – | – | 200 | pF | This specification applies to the external circuit driven by the analog output buffer. |

Table 12. 3.3-V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---------------------------------|---|-----------------------------|-----|-----------------------------|-------|--|
| V _{OSOB} | Input offset voltage (absolute value) | | | | | |
| | Power = Low, Opamp bias = Low | – | 3.2 | 20 | mV | High power setting is not recommended. |
| | Power = Low, Opamp bias = High | – | 3.2 | 20 | mV | |
| | Power = High, Opamp bias = Low | – | 6 | 25 | mV | |
| Power = High, Opamp bias = High | – | 6 | 25 | mV | | |
| TCV _{OSOB} | Average input offset voltage drift | | | | | |
| | Power = Low, Opamp bias = Low | – | 8 | 32 | μV/°C | High power setting is not recommended. |
| | Power = Low, Opamp bias = High | – | 8 | 32 | μV/°C | |
| | Power = High, Opamp bias = Low | – | 12 | 41 | μV/°C | |
| Power = High, Opamp bias = High | – | 12 | 41 | μV/°C | | |
| V _{CMOB} | Common-mode input voltage range | 0.5 | – | V _{DD} – 1.0 | V | – |
| R _{OUTOB} | Output resistance | | | | | |
| | Power = Low | – | – | 10 | W | – |
| | Power = High | – | – | 10 | W | – |
| V _{OHIGHOB} | High output voltage swing (Load = 32 ohms to V _{DD} /2) | | | | | |
| | Power = Low | 0.5 × V _{DD} + 1.0 | – | – | V | – |
| | Power = High | 0.5 × V _{DD} + 1.0 | – | – | V | – |
| V _{LOWOB} | Low output voltage swing (Load = 32 ohms to V _{DD} /2) | | | | | |
| | Power = Low | – | – | 0.5 × V _{DD} – 1.0 | V | – |
| | Power = High | – | – | 0.5 × V _{DD} – 1.0 | V | – |

Table 12. 3.3-V DC Analog Output Buffer Specifications (continued)

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|--------------------|---|-----|-----|-----|------|--|
| I _{SOB} | Supply current including bias cell (no load) Power = Low Power = High | – | 0.8 | 1 | mA | – |
| | | – | 2.0 | 5 | | |
| PSRR _{OB} | Supply voltage rejection ratio | 60 | 64 | – | dB | |
| C _L | Load capacitance | – | – | 200 | pF | This specification applies to the external circuit driven by the analog output buffer. |

DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

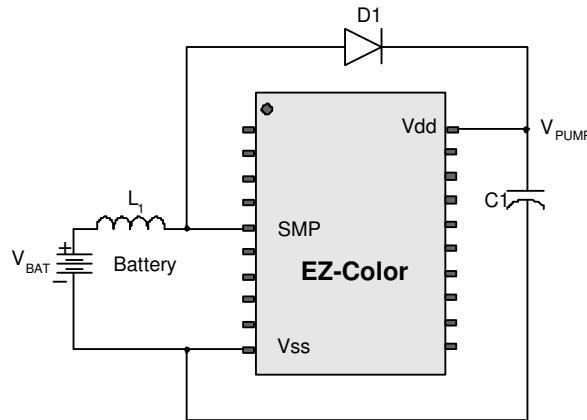
Table 13. DC Switch Mode Pump (SMP) Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------|---|------|------|------|-----------------|--|
| V _{PUMP 5V} | 5 V output voltage at V _{DD} from Pump | 4.75 | 5.0 | 5.25 | V | Configured as in Note 3 . Average, neglecting ripple. SMP trip voltage is set to 5.0 V. |
| V _{PUMP 3V} | 3 V output voltage at V _{DD} from Pump | 3.00 | 3.25 | 3.60 | V | Configured as in Note 3 . Average, neglecting ripple. SMP trip voltage is set to 3.25 V. |
| I _{PUMP} | Available output current V _{BAT} = 1.5 V, V _{PUMP} = 3.25 V V _{BAT} = 1.8 V, V _{PUMP} = 5.0 V | 8 | – | – | mA | Configured as in Note 3 . SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V. |
| | | 5 | – | – | | |
| V _{BAT5V} | Input voltage range from battery | 1.8 | – | 5.0 | V | Configured as in Note 3 . SMP trip voltage is set to 5.0 V. |
| V _{BAT3V} | Input voltage range from battery | 1.0 | 3– | 3.3 | V | Configured as in Note 3 . SMP trip voltage is set to 3.25 V. |
| V _{BATSTART} | Minimum input voltage from battery to start Pump | 1.2 | – | – | V | Configured as in Note 3 . 0 °C ≤ T _A ≤ 100. 1.25 V at T _A = -40 °C. |
| ΔV _{PUMP_Line} | Line regulation (over V _{BAT} range) | – | 5 | – | %V _O | Configured as in Note 3 . V _O is the “V _{DD} Value for PUMP Trip” specified by the VM[2:0] setting in Table 17, “DC POR, SMP, and LVD Specifications,” on page 28. |
| ΔV _{PUMP_Load} | Load regulation | – | 5 | – | %V _O | Configured as in Note 3 . V _O is the “V _{DD} Value for PUMP Trip” specified by the VM[2:0] setting in Table 17, “DC POR, SMP, and LVD Specifications,” on page 28. |
| ΔV _{PUMP_Ripple} | Output Voltage Ripple (depends on capacitor/load) | – | 100 | – | mVpp | Configured as in Note 3 . Load is 5 mA. |
| E ₃ | Efficiency | 35 | 50 | – | % | Configured as in Note 3 . Load is 5 mA. SMP trip voltage is set to 3.25 V. |
| F _{PUMP} | Switching Frequency | – | 1.4 | – | MHz | – |
| DC _{PUMP} | Switching Duty Cycle | – | 50 | – | % | – |

Note

3. L₁ = 2 mH inductor, C₁ = 10 mF capacitor, D₁ = Schottky diode. See Figure 6.

Figure 6. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the analog reference control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 14. 5-V DC Analog Reference Specifications

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|--------------------|-----------|------------------------------|----------------------------|----------------------------|----------------------------|------|
| 0b000 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.228 | V _{DD} /2 + 1.290 | V _{DD} /2 + 1.352 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.078 | V _{DD} /2 - 0.007 | V _{DD} /2 + 0.063 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.336 | V _{DD} /2 - 1.295 | V _{DD} /2 - 1.250 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.224 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.356 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.056 | V _{DD} /2 - 0.005 | V _{DD} /2 + 0.043 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.338 | V _{DD} /2 - 1.298 | V _{DD} /2 - 1.255 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.226 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.356 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.057 | V _{DD} /2 - 0.006 | V _{DD} /2 + 0.044 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.337 | V _{DD} /2 - 1.298 | V _{DD} /2 - 1.256 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.226 | V _{DD} /2 + 1.294 | V _{DD} /2 + 1.359 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.047 | V _{DD} /2 - 0.004 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.338 | V _{DD} /2 - 1.299 | V _{DD} /2 - 1.258 | V |

Table 14. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|--------------------|-----------|---|----------------------------|----------------------------|----------------------------|------|
| 0b001 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] – 0.085 | P2[4] + P2[6] – 0.016 | P2[4] + P2[6] + 0.044 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] – P2[6] – 0.022 | P2[4] – P2[6] + 0.010 | P2[4] – P2[6] + 0.055 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] – 0.077 | P2[4] + P2[6] – 0.010 | P2[4] + P2[6] + 0.051 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] – P2[6] – 0.022 | P2[4] – P2[6] + 0.005 | P2[4] – P2[6] + 0.039 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] – 0.070 | P2[4] + P2[6] – 0.010 | P2[4] + P2[6] + 0.050 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] – P2[6] – 0.022 | P2[4] – P2[6] + 0.005 | P2[4] – P2[6] + 0.039 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] – 0.070 | P2[4] + P2[6] – 0.007 | P2[4] + P2[6] + 0.054 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] – P2[6] – 0.022 | P2[4] – P2[6] + 0.002 | P2[4] – P2[6] + 0.032 | V |
| 0b010 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.037 | V _{DD} – 0.009 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.061 | V _{DD} /2 – 0.006 | V _{DD} /2 + 0.047 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.007 | V _{SS} + 0.028 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.039 | V _{DD} – 0.006 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.049 | V _{DD} /2 – 0.005 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.019 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.037 | V _{DD} – 0.007 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.054 | V _{DD} /2 – 0.005 | V _{DD} /2 + 0.041 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.006 | V _{SS} + 0.024 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.042 | V _{DD} – 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.046 | V _{DD} /2 – 0.004 | V _{DD} /2 + 0.034 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.017 | V |

Table 14. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|--------------------|-----------|-------------------------------------|---------------|---------------|---------------|------|
| 0b011 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | 3 × Bandgap | 3.788 | 3.891 | 3.986 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.500 | 2.604 | 3.699 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.257 | 1.306 | 1.359 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | 3 × Bandgap | 3.792 | 3.893 | 3.982 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.518 | 2.602 | 2.692 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.256 | 1.302 | 1.354 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | 3 × Bandgap | 3.795 | 3.894 | 3.993 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.516 | 2.603 | 2.698 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.256 | 1.303 | 1.353 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | 3 × Bandgap | 3.792 | 3.895 | 3.986 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.522 | 2.602 | 2.685 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.255 | 1.301 | 1.350 | V |
| 0b100 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.495 – P2[6] | 2.586 – P2[6] | 2.657 – P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.502 | 2.604 | 2.719 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.531 – P2[6] | 2.611 – P2[6] | 2.681 – P2[6] | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.500 – P2[6] | 2.591 – P2[6] | 2.662 – P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.519 | 2.602 | 2.693 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.530 – P2[6] | 2.605 – P2[6] | 2.666 – P2[6] | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.503 – P2[6] | 2.592 – P2[6] | 2.662 – P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.517 | 2.603 | 2.698 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.529 – P2[6] | 2.606 – P2[6] | 2.665 – P2[6] | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.505 – P2[6] | 2.594 – P2[6] | 2.665 – P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.525 | 2.602 | 2.685 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.528 – P2[6] | 2.603 – P2[6] | 2.661 – P2[6] | V |

Table 14. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|--------------------|-----------|---|-----------------|-------------------------|-------------------------|------|
| 0b101 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.222 | P2[4] + 1.290 | P2[4] + 1.343 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.331 | P2[4] – 1.295 | P2[4] – 1.254 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.226 | P2[4] + 1.293 | P2[4] + 1.347 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.331 | P2[4] – 1.298 | P2[4] – 1.259 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.227 | P2[4] + 1.294 | P2[4] + 1.347 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.331 | P2[4] – 1.298 | P2[4] – 1.259 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.228 | P2[4] + 1.295 | P2[4] + 1.349 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.332 | P2[4] – 1.299 | P2[4] – 1.260 | V |
| 0b110 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | 2 × Bandgap | 2.535 | 2.598 | 2.644 | V |
| | | V _{AGND} | AGND | Bandgap | 1.227 | 1.305 | 1.398 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.009 | V _{SS} + 0.038 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | 2 × Bandgap | 2.530 | 2.598 | 2.643 | V |
| | | V _{AGND} | AGND | Bandgap | 1.244 | 1.303 | 1.370 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.024 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | 2 × Bandgap | 2.532 | 2.598 | 2.644 | V |
| | | V _{AGND} | AGND | Bandgap | 1.239 | 1.304 | 1.380 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.006 | V _{SS} + 0.026 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | 2 × Bandgap | 2.528 | 2.598 | 2.645 | V |
| | | V _{AGND} | AGND | Bandgap | 1.249 | 1.302 | 1.362 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.018 | V |
| 0b111 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.041 | 4.155 | 4.234 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 1.998 | 2.083 | 2.183 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.010 | V _{SS} + 0.038 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.047 | 4.153 | 4.236 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.012 | 2.082 | 2.157 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.006 | V _{SS} + 0.024 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.049 | 4.154 | 4.238 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.008 | 2.083 | 2.165 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.006 | V _{SS} + 0.026 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.047 | 4.154 | 4.238 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.016 | 2.081 | 2.150 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.018 | V |

Table 15. 3.3-V DC Analog Reference Specifications

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------|--------------------|-----------|---|----------------------------|----------------------------|----------------------------|------|
| 0b000 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | V _{DD} /2 + BandGap | V _{DD} /2 + 1.225 | V _{DD} /2 + 1.292 | V _{DD} /2 + 1.361 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.067 | V _{DD} /2 - 0.002 | V _{DD} /2 + 0.063 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - BandGap | V _{DD} /2 - 1.35 | V _{DD} /2 - 1.293 | V _{DD} /2 - 1.210 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} /2 + BandGap | V _{DD} /2 + 1.218 | V _{DD} /2 + 1.294 | V _{DD} /2 + 1.370 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.038 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - BandGap | V _{DD} /2 - 1.329 | V _{DD} /2 - 1.296 | V _{DD} /2 - 1.259 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | V _{DD} /2 + BandGap | V _{DD} /2 + 1.221 | V _{DD} /2 + 1.294 | V _{DD} /2 + 1.366 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.050 | V _{DD} /2 - 0.002 | V _{DD} /2 + 0.046 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - BandGap | V _{DD} /2 - 1.331 | V _{DD} /2 - 1.296 | V _{DD} /2 - 1.260 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} /2 + BandGap | V _{DD} /2 + 1.226 | V _{DD} /2 + 1.295 | V _{DD} /2 + 1.365 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.028 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.025 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - BandGap | V _{DD} /2 - 1.329 | V _{DD} /2 - 1.297 | V _{DD} /2 - 1.262 | V |
| 0b001 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] - 0.098 | P2[4] + P2[6] - 0.018 | P2[4] + P2[6] + 0.055 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4] - P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] - P2[6] - 0.055 | P2[4] - P2[6] + 0.013 | P2[4] - P2[6] + 0.086 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] - 0.082 | P2[4] + P2[6] - 0.011 | P2[4] + P2[6] + 0.050 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4] - P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] - P2[6] - 0.037 | P2[4] - P2[6] + 0.006 | P2[4] - P2[6] + 0.054 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] - 0.079 | P2[4] + P2[6] - 0.012 | P2[4] + P2[6] + 0.047 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] - P2[6] - 0.038 | P2[4] - P2[6] + 0.006 | P2[4] - P2[6] + 0.057 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] - 0.080 | P2[4] + P2[6] - 0.008 | P2[4] + P2[6] + 0.055 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] - P2[6] - 0.032 | P2[4] - P2[6] + 0.003 | P2[4] - P2[6] + 0.042 | V |

Table 15. 3.3-V DC Analog Reference Specifications (continued)

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|------------------------------------|--|--------------------|--------------------|---|----------------------------|----------------------------|----------------------------|------|
| 0b010 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.06 | V _{DD} - 0.010 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.05 | V _{DD} /2 - 0.002 | V _{DD} /2 + 0.040 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.009 | V _{SS} + 0.056 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.060 | V _{DD} - 0.006 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.028 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.025 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.034 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.058 | V _{DD} - 0.008 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.037 | V _{DD} /2 - 0.002 | V _{DD} /2 + 0.033 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.007 | V _{SS} + 0.046 | V |
| RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.057 | V _{DD} - 0.006 | V _{DD} | V | |
| | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.025 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.022 | V | |
| | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.030 | V | |
| 0b011 | All power settings. Not allowed for 3.3 V | - | - | - | - | - | - | |
| 0b100 | All power settings. Not allowed for 3.3 V | - | - | - | - | - | - | |
| 0b101 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | P2[4] + BandGap (P2[4] = V _{DD} /2) | P2[4] + 1.213 | P2[4] + 1.291 | P2[4] + 1.367 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | V |
| | | V _{REFLO} | Ref Low | P2[4] - BandGap (P2[4] = V _{DD} /2) | P2[4] - 1.333 | P2[4] - 1.294 | P2[4] - 1.208 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + BandGap (P2[4] = V _{DD} /2) | P2[4] + 1.217 | P2[4] + 1.294 | P2[4] + 1.368 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | V |
| | | V _{REFLO} | Ref Low | P2[4] - BandGap (P2[4] = V _{DD} /2) | P2[4] - 1.320 | P2[4] - 1.296 | P2[4] - 1.261 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | P2[4] + BandGap (P2[4] = V _{DD} /2) | P2[4] + 1.217 | P2[4] + 1.294 | P2[4] + 1.369 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | V |
| | | V _{REFLO} | Ref Low | P2[4] - BandGap (P2[4] = V _{DD} /2) | P2[4] - 1.322 | P2[4] - 1.297 | P2[4] - 1.262 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | P2[4] + BandGap (P2[4] = V _{DD} /2) | P2[4] + 1.219 | P2[4] + 1.295 | P2[4] + 1.37 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | V |
| | | V _{REFLO} | Ref Low | P2[4] - BandGap (P2[4] = V _{DD} /2) | P2[4] - 1.324 | P2[4] - 1.297 | P2[4] - 1.262 | V |

Table 15. 3.3-V DC Analog Reference Specifications (continued)

| Reference ARF_CR[5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Unit |
|-----------------------|---|--------------------|-----------|-----------------|-----------------|-------------------------|-------------------------|------|
| 0b110 | RefPower = High Opamp bias = High | V _{REFHI} | Ref High | 2 × BandGap | 2.507 | 2.598 | 2.698 | V |
| | | V _{AGND} | AGND | BandGap | 1.203 | 1.307 | 1.424 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.012 | V _{SS} + 0.067 | V |
| | RefPower = High Opamp bias = Low | V _{REFHI} | Ref High | 2 × BandGap | 2.516 | 2.598 | 2.683 | V |
| | | V _{AGND} | AGND | BandGap | 1.241 | 1.303 | 1.376 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.007 | V _{SS} + 0.040 | V |
| | RefPower = Med Opamp bias = High | V _{REFHI} | Ref High | 2 × BandGap | 2.510 | 2.599 | 2.693 | V |
| | | V _{AGND} | AGND | BandGap | 1.240 | 1.305 | 1.374 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.008 | V _{SS} + 0.048 | V |
| | RefPower = Med Opamp bias = Low | V _{REFHI} | Ref High | 2 × BandGap | 2.515 | 2.598 | 2.683 | V |
| | | V _{AGND} | AGND | BandGap | 1.258 | 1.302 | 1.355 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.03 | V |
| 0b111 | All power settings. Not allowed for 3.3 V. | – | – | – | – | – | – | |

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Analog PSoC Block Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------|---|-----|------|-----|-------|-------|
| R _{CT} | Resistor Unit Value (Continuous Time) | – | 12.2 | – | kΩ | |
| C _{SC} | Capacitor Unit Value (Switched Capacitor) | – | 80 | – | fF | |

DC POR, SMP, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. DC POR, SMP, and LVD Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|-----|------|-----|-------|-------|
| V _{PPOR0R} | V _{DD} Value for PPOR Trip (positive ramp) | | | | | |
| V _{PPOR1R} | PORLEV[1:0] = 00b | – | 2.91 | – | V | |
| V _{PPOR2R} | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| | PORLEV[1:0] = 10b | – | 4.55 | – | V | |
| V _{PPOR0} | V _{DD} Value for PPOR Trip (negative ramp) | | | | | |
| V _{PPOR1} | PORLEV[1:0] = 00b | – | 2.82 | – | V | |
| V _{PPOR2} | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| | PORLEV[1:0] = 10b | – | 4.55 | – | V | |
| V _{PH0} | PPOR Hysteresis | – | 92 | – | mV | |
| V _{PH1} | PORLEV[1:0] = 00b | – | 0 | – | mV | |
| V _{PH2} | PORLEV[1:0] = 01b | – | 0 | – | mV | |
| | PORLEV[1:0] = 10b | – | 0 | – | mV | |

Notes

4. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
5. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

Table 17. DC POR, SMP, and LVD Specifications (continued)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|------------------------------------|------|------|---------------------|-------|-------|
| | V _{DD} Value for LVD Trip | | | | | |
| V _{LVD0} | VM[2:0] = 000b | 2.86 | 2.92 | 2.98 ^[4] | V | |
| V _{LVD1} | VM[2:0] = 001b | 2.96 | 3.02 | 3.08 | V | |
| V _{LVD2} | VM[2:0] = 010b | 3.07 | 3.13 | 3.20 | V | |
| V _{LVD3} | VM[2:0] = 011b | 3.92 | 4.00 | 4.08 | V | |
| V _{LVD4} | VM[2:0] = 100b | 4.39 | 4.48 | 4.57 | V | |
| V _{LVD5} | VM[2:0] = 101b | 4.55 | 4.64 | 4.74 ^[5] | V | |
| V _{LVD6} | VM[2:0] = 110b | 4.63 | 4.73 | 4.82 | V | |
| V _{LVD7} | VM[2:0] = 111b | 4.72 | 4.81 | 4.91 | V | |
| | V _{DD} Value for SMP Trip | | | | | |
| V _{PUMP0} | VM[2:0] = 000b | 2.96 | 3.02 | 3.08 | V | |
| V _{PUMP1} | VM[2:0] = 001b | 3.03 | 3.10 | 3.16 | V | |
| V _{PUMP2} | VM[2:0] = 010b | 3.18 | 3.25 | 3.32 | V | |
| V _{PUMP3} | VM[2:0] = 011b | 4.11 | 4.19 | 4.28 | V | |
| V _{PUMP4} | VM[2:0] = 100b | 4.55 | 4.64 | 4.74 | V | |
| V _{PUMP5} | VM[2:0] = 101b | 4.63 | 4.73 | 4.82 | V | |
| V _{PUMP6} | VM[2:0] = 110b | 4.72 | 4.82 | 4.91 | V | |
| V _{PUMP7} | VM[2:0] = 111b | 4.90 | 5.00 | 5.10 | V | |

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|---|-----------------------|-----|------------------------|-------|---|
| V _{DDP} | V _{DD} for programming and erase | 4.5 | 5 | 5.5 | V | This specification applies to the functional requirements of external programmer tools. |
| V _{DDL} | Low V _{DD} for verify | 3.0 | 3.1 | 3.2 | V | This specification applies to the functional requirements of external programmer tools. |
| V _{DDH} | High V _{DD} for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools. |
| V _{DDIWRITE} | Supply voltage for flash write operation | 3.15 | – | 5.25 | V | This specification applies to this device when it is executing internal flash writes. |
| I _{DDP} | Supply current during programming or verify | – | 10 | 30 | mA | |
| V _{ILP} | Input Low-voltage during programming or verify | – | – | 0.8 | V | |
| V _{IHP} | Input High-voltage during programming or verify | 2.2 | – | – | V | |
| I _{ILP} | Input Current when Applying V _{ILP} to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| I _{IHP} | Input Current when Applying V _{IHP} to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| V _{OLV} | Output Low-voltage during programming or verify | – | – | V _{SS} + 0.75 | V | |
| V _{OHV} | Output High-voltage during programming or verify | V _{DD} - 1.0 | – | V _{DD} | V | |
| Flash _{ENPB} | flash endurance (per block) | 50,000 ^[6] | – | – | – | Erase/write cycles per block. |
| Flash _{ENT} | flash endurance (total) ^[7] | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | flash data retention | 10 | – | – | Years | |

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. DC I²C Specifications

| Parameter | Description | Min | Typ | Max | Units | Notes |
|-----------------------------------|------------------|-----------------------|-----|------------------------|-------|-----------------------------------|
| V _{IL12C} ^[8] | Input low level | – | – | 0.3 × V _{DD} | V | 3.0 V ≤ V _{DD} ≤ 3.6 V |
| | | – | – | 0.25 × V _{DD} | V | 4.75 V ≤ V _{DD} ≤ 5.25 V |
| V _{IH12C} ^[8] | Input high level | 0.7 × V _{DD} | – | – | V | 3.0 V ≤ V _{DD} ≤ 5.25 V |

Notes

- The 50,000 cycle flash endurance per block is only guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
- A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (flashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.
- All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections. The I²C GPIO pins also meet the mentioned specs.

AC Electrical Characteristics
AC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 20. AC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------------|---|--------|--------|---------------------------|-------|--|
| F _{IMO24} | Internal main oscillator frequency for 24 MHz | 23.4 | 24 | 24.6 ^[9,10,11] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See the figure on page 19. SLIMO Mode = 0. |
| F _{IMO6} | Internal main oscillator frequency for 6 MHz | 5.5 | 6 | 6.5 ^[9,10,11] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See the figure on page 19. SLIMO Mode = 1. |
| F _{CPU1} | CPU frequency (5 V Nominal) | 0.0914 | 24 | 24.6 ^[9,10] | MHz | – |
| F _{CPU2} | CPU frequency (3.3 V Nominal) | 0.0914 | 12 | 12.3 ^[10,11] | MHz | – |
| F _{48M} | Digital PSoC block frequency | 0 | 48 | 49.2 ^[9,10,12] | MHz | Refer to the AC Digital Block Specifications below. |
| F _{24M} | Digital PSoC block frequency | 0 | 24 | 24.6 ^[10,12] | MHz | – |
| F _{32K1} | Internal low speed oscillator frequency | 15 | 32 | 64 | kHz | – |
| F _{32K_U} | Internal low speed oscillator untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the <i>PSoC Technical Reference Manual</i> for details on timing this. |
| DC _{ILO} | Internal low speed oscillator duty cycle | 20 | 50 | 80 | % | – |
| F _{32K2} | External crystal oscillator | – | 32.768 | – | kHz | Accuracy is capacitor and crystal dependent. 50% duty cycle. |
| F _{PLL} | PLL frequency | – | 23.986 | – | MHz | A multiple (x732) of crystal frequency. |
| T _{PLLSLEW} | PLL lock time | 0.5 | – | 10 | ms | – |
| T _{PLLSLEWLOW} | PLL lock time for low gain setting | 0.5 | – | 50 | ms | – |
| T _{OS} | External crystal oscillator startup to 1% | – | 250 | 500 | ms | – |
| T _{OSACC} | External crystal oscillator startup to 100 ppm | – | 300 | 600 | ms | The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{OSACC} period. Correct operation assumes a properly loaded 1 μW maximum drive level 32.768 kHz crystal. 3.0V ≤ V _{DD} ≤ 5.5 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$. |
| T _{XRST} | External reset pulse width | 10 | – | – | μs | – |
| DC _{24M} | 24 MHz duty cycle | 40 | 50 | 60 | % | – |
| Step _{24M} | 24 MHz trim step size | – | 50 | – | kHz | – |

Notes

9. 4.75 V < V_{DD} < 5.25 V.

10. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.

11. 3.0 V < V_{DD} < 3.6 V.

12. See the individual user module data sheets for information on maximum frequencies for user modules.

13. Refer to Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

Table 20. AC Chip-Level Specifications (continued)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------------|---|------|------|-------------------------|-------|---|
| Fout48M | 48 MHz Output Frequency | 46.8 | 48.0 | 49.2 ^[9, 11] | MHz | Trimmed. Utilizing factory trim values. |
| F _{MAX} | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | – |
| SR _{POWER_UP} | Power Supply Slew Rate | – | – | 250 | V/ms | V _{DD} slew rate during power up. |
| T _{POWERUP} | Time from End of POR to CPU Executing Code | – | 16 | 100 | ms | Power up from 0V. See the System Resets section of the <i>PSoC Technical Reference Manual</i> . |
| tjit_IMO ^[13] | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 200 | 700 | ps | N = 32 |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS) | – | 300 | 900 | | |
| | 24 MHz IMO period jitter (RMS) | – | 100 | 400 | | |
| tjit_PLL ^[13] | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 200 | 800 | ps | N = 32 |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS) | – | 300 | 1200 | | |
| | 24 MHz IMO period jitter (RMS) | – | 100 | 700 | | |

Figure 7. PLL Lock Timing Diagram

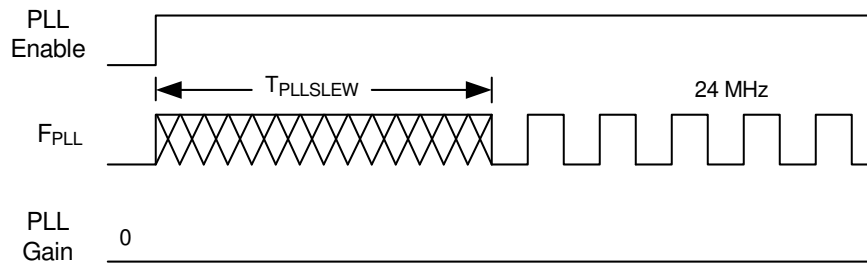


Figure 8. PLL Lock for Low Gain Setting Timing Diagram

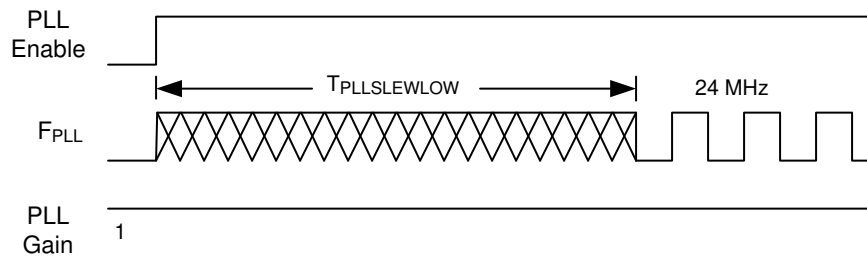
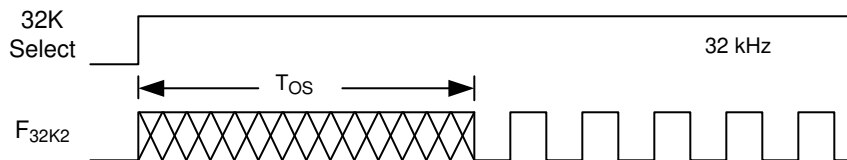


Figure 9. External Crystal Oscillator Startup Timing Diagram



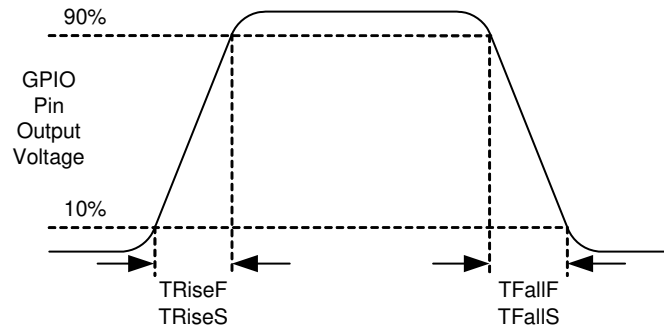
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 $^{\circ}\text{C}$ and are for design guidance only.

Table 21. AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------|--|-----|-----|------|-------|---|
| F_{GPIO} | GPIO operating frequency | 0 | – | 12.3 | MHz | Normal Strong Mode |
| T_{RiseF} | Rise time, normal strong mode, $C_{load} = 50\text{ pF}$ | 3 | – | 18 | ns | $V_{DD} = 4.75\text{ to }5.25\text{ V}$, 10% - 90% |
| T_{FallF} | Fall time, normal strong mode, $C_{load} = 50\text{ pF}$ | 2 | – | 18 | ns | $V_{DD} = 4.75\text{ to }5.25\text{ V}$, 10% - 90% |
| T_{RiseS} | Rise time, slow strong mode, $C_{load} = 50\text{ pF}$ | 10 | 27 | – | ns | $V_{DD} = 3\text{ to }5.25\text{ V}$, 10% - 90% |
| T_{FallS} | Fall time, slow strong mode, $C_{load} = 50\text{ pF}$ | 10 | 22 | – | ns | $V_{DD} = 3\text{ to }5.25\text{ V}$, 10% - 90% |

Figure 10. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 22. 5-V AC Operational Amplifier Specifications

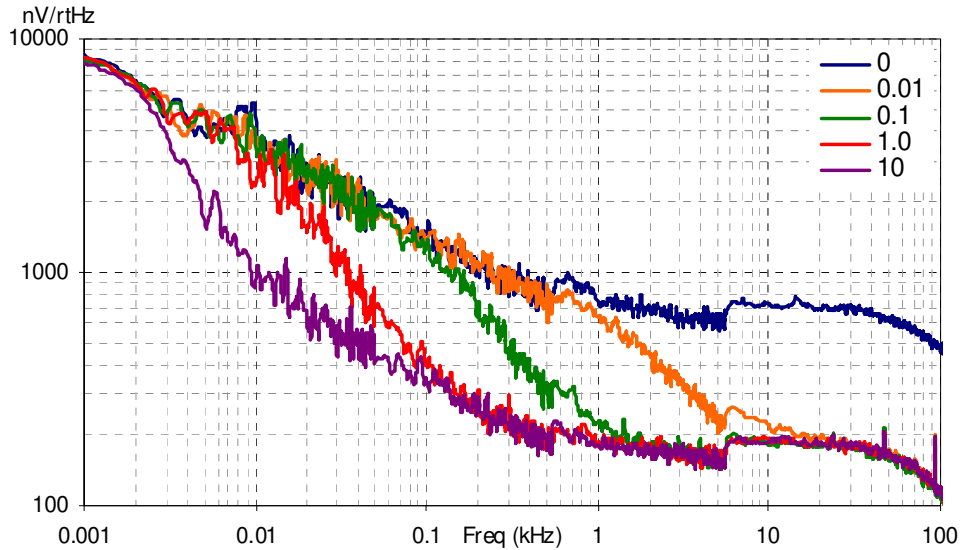
| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|------|-----|------|----------|-------|
| T _{ROA} | Rising Settling Time to 0.1% for a 1 V Step (10 pF load, Unity Gain) | – | – | 3.9 | μs | – |
| | Power = Low, Opamp Bias = Low | – | – | 0.72 | μs | – |
| | Power = High, Opamp Bias = High | – | – | 0.62 | μs | – |
| T _{SOA} | Falling Settling Time to 0.1% for a 1 V Step (10 pF load, Unity Gain) | – | – | 5.9 | μs | – |
| | Power = Low, Opamp Bias = Low | – | – | 0.92 | μs | – |
| | Power = High, Opamp Bias = High | – | – | 0.72 | μs | – |
| SR _{ROA} | Rising Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) | 0.15 | – | – | V/μs | – |
| | Power = Low, Opamp Bias = Low | 1.7 | – | – | V/μs | – |
| | Power = High, Opamp Bias = High | 6.5 | – | – | V/μs | – |
| SR _{FOA} | Falling Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) | 0.01 | – | – | V/μs | – |
| | Power = Low, Opamp Bias = Low | 0.5 | – | – | V/μs | – |
| | Power = High, Opamp Bias = High | 4.0 | – | – | V/μs | – |
| BW _{OA} | Gain Bandwidth Product | 0.75 | – | – | MHz | – |
| | Power = Low, Opamp Bias = Low | 3.1 | – | – | MHz | – |
| | Power = High, Opamp Bias = High | 5.4 | – | – | MHz | – |
| E _{NOA} | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz | – |

Table 23. 3.3-V AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|------|-----|------|----------|-------|
| T _{ROA} | Rising settling time to 0.1% of a 1 V Step (10 pF load, Unity Gain) | – | – | 3.92 | μs | – |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | – |
| T _{SOA} | Falling settling time to 0.1% of a 1 V Step (10 pF load, Unity Gain) | – | – | 5.41 | μs | – |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | – |
| SR _{ROA} | Rising Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) | 0.31 | – | – | V/μs | – |
| | Power = Medium, Opamp Bias = High | 2.7 | – | – | V/μs | – |
| SR _{FOA} | Falling slew rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain) | 0.24 | – | – | V/μs | – |
| | Power = Medium, Opamp Bias = High | 1.8 | – | – | V/μs | – |
| BW _{OA} | Gain bandwidth product | 0.67 | – | – | MHz | – |
| | Power = Medium, Opamp Bias = High | 2.8 | – | – | MHz | – |
| E _{NOA} | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz | – |

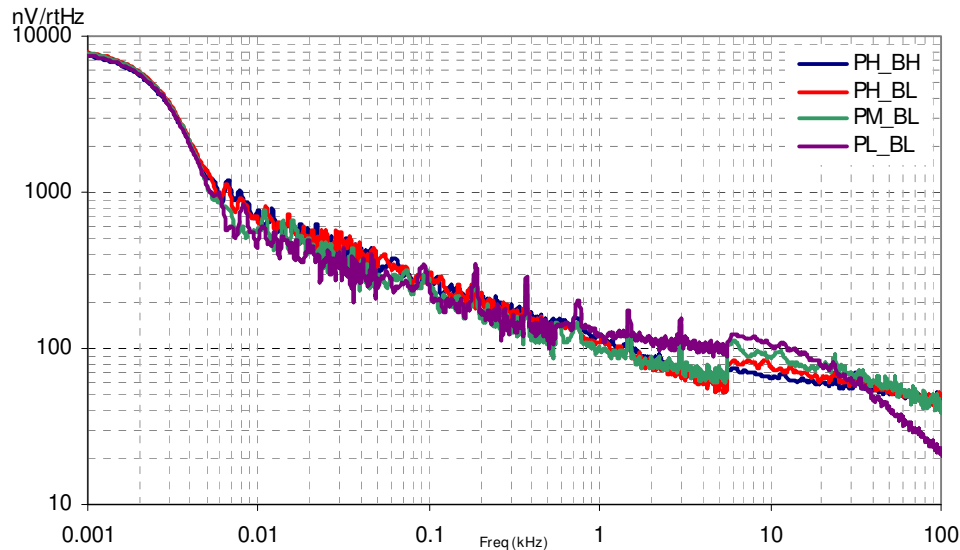
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 11. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 12. Typical Opamp Noise



AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 24. AC Low Power Comparator Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------|-------------------|-----|-----|-----|---------------|--|
| T_{RLPC} | LPC response time | – | – | 50 | μs | $\geq 50\text{ mV}$ overdrive comparator reference set within V_{REFLPC} . |

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Unit | Notes |
|-------------------|--|--------------------|-----|------|------|--|
| All functions | Block input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| Timer | Input clock frequency | | | | | |
| | No capture, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | No capture, $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| | With capture | – | – | 24.6 | MHz | |
| | Capture pulse width | 50 ^[14] | – | – | ns | |
| Counter | Input clock frequency | | | | | |
| | No enable input, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | No enable input, $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| | With enable input | – | – | 24.6 | MHz | |
| | Enable input pulse width | 50 ^[14] | – | – | ns | |
| Dead Band | Kill pulse width | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50 ^[14] | – | – | ns | |
| | Disable mode | 50 ^[14] | – | – | ns | |
| | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| CRCPRS (PRS Mode) | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.2 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| CRCPRS (CRC Mode) | Input clock frequency | – | – | 24.6 | MHz | |
| SPIM | Input clock frequency | – | – | 8.2 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2 |
| SPIS | Input clock (SCLK) frequency | – | – | 4.1 | MHz | The input clock is the SPI SCLK in SPIS mode |
| | Width of SS_negated between transmissions | 50 ^[14] | – | – | ns | |

Note

14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 25. AC Digital Block Specifications (continued)

| Function | Description | Min | Typ | Max | Unit | Notes |
|-------------|-----------------------------------|-----|-----|------|------|--|
| Transmitter | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8 |
| | $V_{DD} \geq 4.75$ V, 2 stop bits | – | – | 49.2 | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 24.6 | MHz | |
| Receiver | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8 |
| | $V_{DD} \geq 4.75$ V, 2 stop bits | – | – | 49.2 | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 24.6 | MHz | |

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. 5V AC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------|--|------|-----|-----|------------------------|-------|
| T_{ROB} | Rising Settling Time to 0.1%, 1 V Step, 100pF Load Power = Low Power = High | – | – | 4 | μs | |
| | | – | – | 4 | μs | |
| T_{SOB} | Falling Settling Time to 0.1%, 1 V Step, 100pF Load Power = Low Power = High | – | – | 3.4 | μs | |
| | | – | – | 3.4 | μs | |
| SR_{ROB} | Rising Slew Rate (20% to 80%), 1 V Step, 100pF Load Power = Low Power = High | 0.5 | – | – | $\text{V}/\mu\text{s}$ | |
| | | 0.5 | – | – | $\text{V}/\mu\text{s}$ | |
| SR_{FOB} | Falling Slew Rate (80% to 20%), 1 V Step, 100pF Load Power = Low Power = High | 0.55 | – | – | $\text{V}/\mu\text{s}$ | |
| | | 0.55 | – | – | $\text{V}/\mu\text{s}$ | |
| BW_{OB} | Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load Power = Low Power = High | 0.8 | – | – | MHz | |
| | | 0.8 | – | – | MHz | |
| BW_{OB} | Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load Power = Low Power = High | 300 | – | – | kHz | |
| | | 300 | – | – | kHz | |

Table 27. 3.3V AC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|--|-----|-----|-----|-------|-------|
| T _{ROB} | Rising Settling Time to 0.1%, 1 V Step, 100pF Load Power = Low Power = High | – | – | 4.7 | μs | |
| | | – | – | 4.7 | μs | |
| T _{SOB} | Falling Settling Time to 0.1%, 1 V Step, 100pF Load Power = Low Power = High | – | – | 4 | μs | |
| | | – | – | 4 | μs | |
| SR _{ROB} | Rising Slew Rate (20% to 80%), 1 V Step, 100pF Load Power = Low Power = High | .36 | – | – | V/μs | |
| | | .36 | – | – | V/μs | |
| SR _{FOB} | Falling Slew Rate (80% to 20%), 1 V Step, 100pF Load Power = Low Power = High | .4 | – | – | V/μs | |
| | | .4 | – | – | V/μs | |
| BW _{OB} | Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load Power = Low Power = High | 0.7 | – | – | MHz | |
| | | 0.7 | – | – | MHz | |
| BW _{OB} | Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load Power = Low Power = High | 200 | – | – | kHz | |
| | | 200 | – | – | kHz | |

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and -40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 28. 5V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|------------------------|-------|-----|------|-------|-------|
| F _{OSCEXT} | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High Period | 20.6 | – | 5300 | ns | |
| – | Low Period | 20.6 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | μs | |

Table 29. 3.3V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|-------|-----|------|-------|---|
| F _{OSCEXT} | Frequency with CPU Clock Divide by 1 | 0.093 | – | 12.3 | MHz | Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| F _{OSCEXT} | Frequency with CPU Clock Divide by 2 or Greater | 0.186 | – | 24.6 | MHz | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met. |
| – | High Period with CPU Clock Divide by 1 | 41.7 | – | 5300 | ns | – |
| – | Low Period with CPU Clock Divide by 1 | 41.7 | – | – | ns | – |
| – | Power Up IMO to Switch | 150 | – | – | μs | – |

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 30. AC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-----|-----|---------------------|-------|---|
| T_{RSCLK} | Rise Time of SCLK | 1 | – | 20 | ns | – |
| T_{FSCLK} | Fall Time of SCLK | 1 | – | 20 | ns | – |
| T_{SSCLK} | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | – |
| T_{HSCLK} | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | – |
| F_{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | – |
| T_{ERASEB} | flash Erase Time (Block) | – | 10 | – | ms | – |
| T_{WRITE} | flash Block Write Time | – | 40 | – | ms | – |
| T_{DSCLK} | Data Out Delay from Falling Edge of SCLK | – | – | 45 | ns | $V_{DD} > 3.6$ |
| T_{DSCLK3} | Data Out Delay from Falling Edge of SCLK | – | – | 50 | ns | $3.0 \leq V_{DD} \leq 3.6$ |
| $T_{ERASEALL}$ | flash Erase Time (Bulk) | – | 80 | – | ms | Erase all blocks and protection fields at once. |
| $T_{PROGRAM_HOT}$ | flash Block Erase + flash Block Write Time | – | – | 100 ^[15] | ms | $0^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$ |
| $T_{PROGRAM_COLD}$ | flash Block Erase + flash Block Write Time | – | – | 200 ^[15] | ms | $-40^{\circ}\text{C} \leq T_J \leq 0\text{ }^{\circ}\text{C}$ |

Note

15. For the full industrial range, the user must employ a Temperature Sensor User Module (flashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

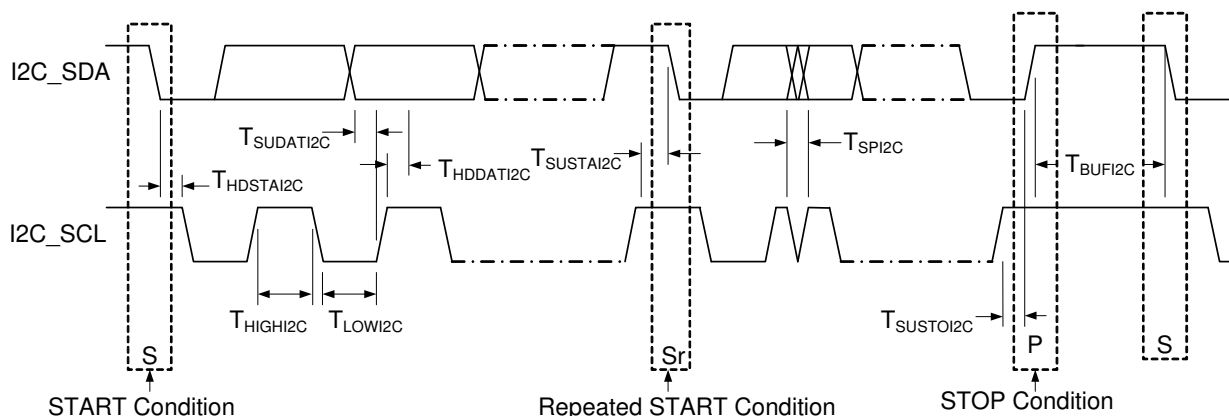
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and -40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard-Mode | | Fast-Mode | | Units | Notes |
|------------------------|--|---------------|-----|---------------------|-----|-------|-------|
| | | Min | Max | Min | Max | | |
| F _{SCL I2C} | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz | – |
| T _{HDSTA I2C} | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | μs | – |
| T _{LOW I2C} | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | μs | – |
| T _{HIGH I2C} | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | μs | – |
| T _{SUSTA I2C} | Set-up Time for a Repeated START Condition | 4.7 | – | 0.6 | – | μs | – |
| T _{HDDAT I2C} | Data Hold Time | 0 | – | 0 | – | μs | – |
| T _{SUDAT I2C} | Data Set-up Time | 250 | – | 100 ^[16] | – | ns | – |
| T _{SUSTO I2C} | Set-up Time for STOP Condition | 4.0 | – | 0.6 | – | μs | – |
| T _{BUFI2C} | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | μs | – |
| T _{SPI2C} | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | – |

Figure 13. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

16. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement t_{SU, DAT} ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU, DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8CLED16 EZ-Color device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

Packaging Dimensions

Figure 14. 28-Pin (210-Mil) SSOP

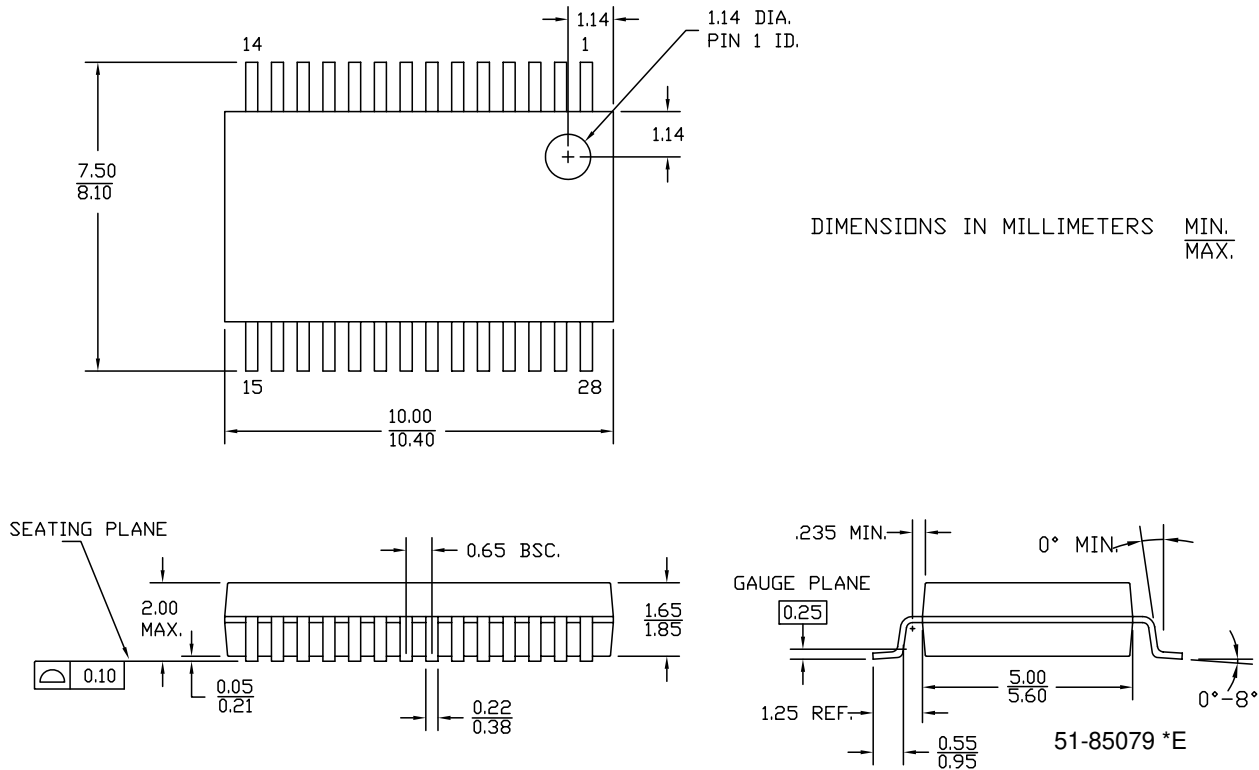
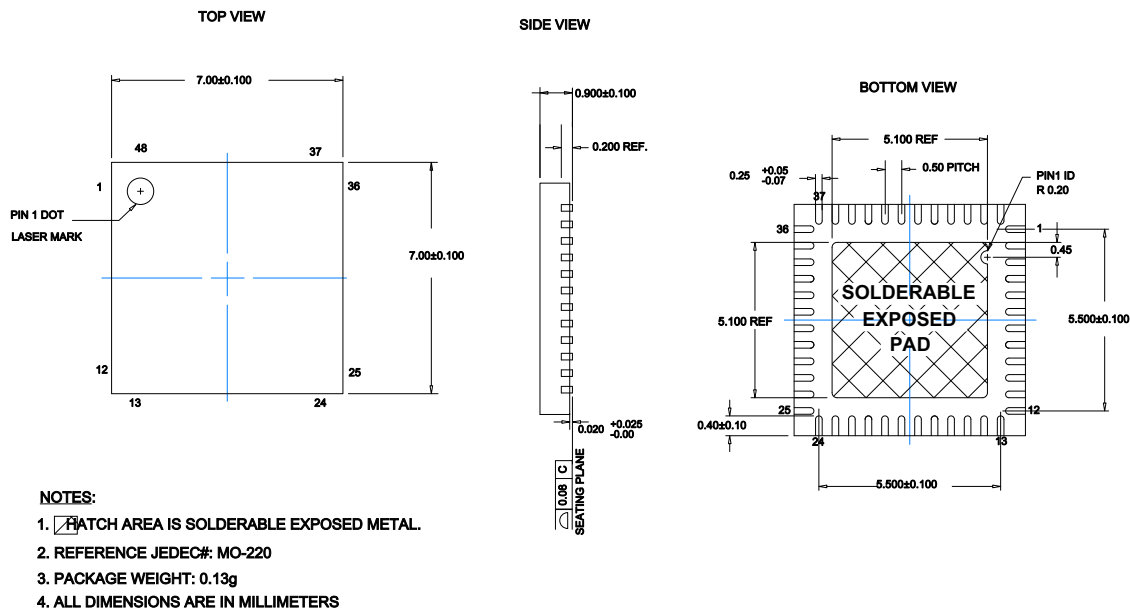


Figure 15. 48-Pin (7 x 7 x 1.0 mm) QFN (Sawn)



001-13191 *E

Important Note

For information on the preferred dimensions for mounting QFN packages, see the following Application Note "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at <http://www.amkor.com>.

Pinned vias for thermal conduction are not required for the low-power device.

Thermal Impedances

Table 32. Thermal Impedances per Package

| Package | Typical θ_{JA} [17] |
|------------------------|----------------------------|
| 28 SSOP | 94 °C/W |
| 48 QFN ^[18] | 28 °C/W |

Capacitance on Crystal Pins

Table 33. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|---------|---------------------|
| 28 SSOP | 2.8 pF |
| 48 QFN | 1.8 pF |

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 34. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Time at Maximum Peak Temperature |
|---------|--------------------------|----------------------------------|
| 28 SSOP | 260 °C | 30 s |
| 48 QFN | 260 °C | 30 s |

Notes

17. $T_J = T_A + \text{POWER} \times \theta_{JA}$

18. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at <http://www.amkor.com>.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at <http://www.cypress.com> and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible and used on the bench in development. It is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. It is available free of charge at <http://www.cypress.com>.

Evaluation Tools

All evaluation tools are sold at the [Cypress Online Store](#).

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval Socket Programming and Evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers are sold at the [Cypress Online Store](#).

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240V power supply, euro-plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 35. Emulation and Programming Accessories

| Part No. | Pin Package | Flex-Pod Kit ^[19] | Foot Kit ^[20] | Adapter ^[21] |
|------------------|-------------|------------------------------|--------------------------|--|
| CY8CLED16-48LFXI | 48-pin QFN | CY3250-LED16QFN | CY3250-48QFN-FK | Adapters can be found at http://www.emulation.com . |

Ordering Information

Key Device Features

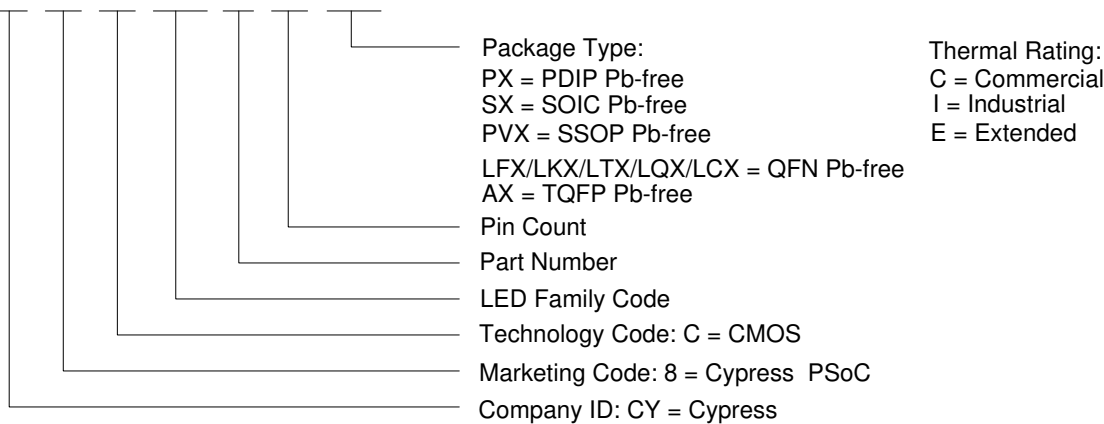
The following table lists the CY8CLED16 EZ-Color devices' key package features and ordering codes.

Table 36. Device Key Features and Ordering Information

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital PSoC Blocks | Analog PSoC Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|-----------------------------------|-------------------|---------------|-------------|------------------|-------------------|---------------------|--------------------|------------------|---------------|----------------|----------|
| 48-Pin QFN (Sawn) | CY8CLED16-48LTXI | 32 K | 2 K | Yes | -40 °C to +85 °C | 16 | 12 | 44 | 12 | 4 | Yes |
| 48-Pin QFN (Tape and Reel) (Sawn) | CY8CLED16-48LTXIT | 32 K | 2 K | Yes | -40 °C to +85 °C | 16 | 12 | 44 | 12 | 4 | Yes |

Ordering Code Definitions

CY 8 C LED xx - xx xxxx



Notes

- 19. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
- 20. Foot kit includes surface mount feet that can be soldered to the target PCB.
- 21. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

Acronyms

Acronyms Used

Table 37 lists the acronyms that are used in this document.

Table 37. Acronyms Used in this Datasheet

| Acronym | Description | Acronym | Description |
|---------|---|-------------------|---|
| AC | alternating current | MAC | multiply-accumulate |
| ADC | analog-to-digital converter | MIPS | million instructions per second |
| API | application programming interface | PCB | printed circuit board |
| CMOS | complementary metal oxide semiconductor | PDIP | plastic dual-in-line package |
| CPU | central processing unit | PLL | phase-locked loop |
| CRC | cyclic redundancy check | POR | power-on reset |
| CT | continuous time | PPOR | precision power on reset |
| DAC | digital-to-analog converter | PRS | pseudo-random sequence |
| DC | direct current | PSoC [®] | Programmable System-on-Chip |
| DTMF | dual-tone multi-frequency | PWM | pulse-width modulator |
| ECO | external crystal oscillator | QFN | quad flat no leads |
| EEPROM | electrically erasable programmable read-only memory | RTC | real time clock |
| GPIO | general purpose I/O | SAR | successive approximation |
| ICE | in-circuit emulator | SC | switched capacitor |
| IDE | integrated development environment | SMP | switch mode pump |
| ILO | internal low speed oscillator | SPI | serial peripheral interface |
| IMO | internal main oscillator | SRAM | static random access memory |
| I/O | input/output | SROM | supervisory read only memory |
| IrDA | infrared data association | SSOP | shrink small-outline package |
| ISSP | in-system serial programming | UART | universal asynchronous receiver / transmitter |
| LCD | liquid crystal display | USB | universal serial bus |
| LED | light-emitting diode | WDT | watchdog timer |
| LPC | low power comparator | XRES | external reset |
| LVD | low-voltage detect | | |

Reference Documents

Design Aids – Reading and Writing PSoC[®] Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at <http://www.amkor.com>.

Document Conventions

Units of Measure

Table 38 lists the units of measures.

Table 38. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------|--------|-------------------|
| dB | decibels | ms | milliseconds |
| °C | degree Celsius | mH | millihenry |
| fF | femtofarad | ns | nanoseconds |
| kHz | kilohertz | μV | microvolts |
| kΩ | kilohm | V | volts |
| MHz | megahertz | mV | millivolts |
| μA | microamperes | μW | microwatts |
| μs | microseconds | % | percent |
| mA | milliamperes | W | watt |
| nA | nanoamperes | mm | millimeters |
| pF | picofarad | ps | picosecond |
| pA | pikoamperes | ppm | parts per million |
| rt-Hz | root hertz | nV | nanovolts |

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are decimals.

Glossary

- active high
 1. A logic signal having its asserted state as the logic 1 state.
 2. A logic signal having the logic 1 state as the higher voltage of the two states.

- analog blocks

The basic programmable opamp circuits. These are switched capacitor (SC) and continuous time (CT) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.

- analog-to-digital (ADC)

A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.

- Application programming interface (API)

A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.

- asynchronous

A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.

- bandgap reference

A stable voltage reference design that matches the positive temperature coefficient of V_T with the negative temperature coefficient of V_{BE} , to produce a zero temperature coefficient (ideally) reference.

- bandwidth
 1. The frequency range of a message or information processing system measured in hertz.
 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

| | |
|-------------------------------|--|
| bias | <ol style="list-style-type: none">1. A systematic deviation of a value from a reference value.2. The amount by which the average of a set of values departs from a reference value.3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | <ol style="list-style-type: none">1. A functional unit that performs a single function, such as an oscillator.2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | <ol style="list-style-type: none">1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.3. An amplifier used to lower the output impedance of a system. |
| bus | <ol style="list-style-type: none">1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |

Glossary (continued)

| | |
|---------------------------------|---|
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |
| External Reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF. |
| flash block | The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected. A flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| I ² C | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I ² C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I ² C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | <ol style="list-style-type: none"> 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses V _{DD} and provides an interrupt to the system when V _{DD} falls lower than a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space. |

Glossary (continued)

| | |
|-----------------------------|---|
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the <i>slave device</i> . |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |
| noise | <ol style="list-style-type: none">1. A disturbance that affects a signal and that may distort the information carried by the signal.2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| Phase-locked loop (PLL) | An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| Power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |

Glossary (continued)

| | |
|-----------------|---|
| serial | <ol style="list-style-type: none">1. Pertaining to a process in which all events occur one after the other.2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | <ol style="list-style-type: none">1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| V _{DD} | A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V. |
| V _{SS} | A name for a power net meaning "voltage source." The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

Document History Page

| Document Title: CY8CLED16 EZ-Color™ HB LED Controller Document Number: 001-13105 | | | | |
|---|---------|------------------|-----------------|---|
| Revision | ECN No | Origin of Change | Submission Date | Description of Change |
| ** | 1148504 | SFVTMP3 | See ECN | New document (revision **). |
| *A | 2763950 | DPT | 09/29/2009 | Added 48QFN package diagram (Sawn). Added Saw Marketing part number in ordering information. |
| *B | 2794355 | XBM | 10/28/2009 | Added "Contents" on page 3 Updated "Development Tools" on page 7. Corrected FCPU1 and FCPU2 parameters in "AC Chip-Level Specifications" on page 31. |
| *C | 2850593 | FRE | 01/14/2010 | Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification. Added note to flash Endurance specification. Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. Corrected the Pod Kit part numbers. Updated Development Tool Selection . Updated copyright and Sales, Solutions, and Legal Information URLs. Updated 28-Pin SSOP 48-Pin QFN (Punched), 48-Pin QFN (Sawn) package diagrams. Removed Preliminary for Final status. |
| *D | 2896238 | CGX | 03/19/10 | Updated ordering information table. Removed part numbers CY8CLED16-48LFXI and CY8CLED16-48LFXIT Updated copyright section. Updated package diagram for spec 51-85061 |
| *E | 2903043 | NJF | 04/01/2010 | Updated Cypress website links Added T _{BAKETEMP} and T _{BAKETIME} parameters Removed reference to 2.4V Removed sections "Third Party Tools" and "Build a PSoC Emulator" |
| *F | 3054665 | CGX | 10/11/2010 | Removed pruned parts CY8CLED16-48PVXI and CY8CLED16-48PVXIT |
| *G | 3114959 | NJF | 12/19/10 | Added DC I ² C Specifications table. Added F _{32K_U} max limit. Added T _{jitter_IMO} specification, removed existing jitter specifications. Updated DC Analog reference, DC operational amplifier specifications and DC analog output buffer specifications tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I ² C Timing Diagram. They were updated for clearer understanding. Updated Figure 12 since the labelling for y-axis was incorrect. Removed footnote reference for "Solder Reflow Peak Temperature" table. |
| *H | 3284932 | SHOB | 06/24/11 | Updated Getting Started , Development Tools , and Designing with PSoC Designer . Removed drawings and references to 48-Pin QFN (Punched) and 48-Pin SSOP. Removed obsolete kits. Removed reference to obsolete spec AN2012. |
| *I | 3403622 | 10/12/11 | MKKU | Removed the following pruned parts from the Ordering Information and Accessories (Emulation and Programming) sections. CY8CLED16-28PVXI CY8CLED16-28PVXIT |

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