

### 1.1 Scope.

This specification covers the device requirements for a hybrid quad 12-bit voltage output D/A converter with double buffered latches.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD390SD/883B
-2	AD390TD/883B

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28.

### 1.3 Absolute Maximum Ratings. ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

+ $V_S$ to DGND	0 to +18V
- $V_S$ to DGND	0 to -18V
Digital Inputs (Pins 1-12, 23-28) to DGND	-1.0V to +7V
Ref In to DGND	$\pm V_S$
AGND to DGND	$\pm 0.6\text{V}$
Analog Outputs (Pins 16, 18-21)	Infinite
Short to AGND or DGND, Momentary Shorts to $\pm V_S$	
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC} = 8^\circ\text{C/W}$   
 $\theta_{JA} = 25^\circ\text{C/W}$

# AD390—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit @ +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Data Input Voltage High End Point Electrical	V <sub>IH</sub>	-1, 2 -1, 2	2.0(2.0) 5.5(5.5)	2.0		2.0	Test Limits Apply to Pins 1-12. Design Limits Apply to Pins 23-28.	V min V max V min
Data Input Voltage Low End Point Electrical	V <sub>IL</sub>	-1, 2 -1, 2	0.0(0.0) 0.8(0.8)	0.8		0.8	Test Limits Apply to Pins 1-12. Design Limits Apply to Pins 23-28.	V min V max V max
Input Current High End Point Electrical	I <sub>IH</sub>	-1, 2 -1, 2	1200(1200)	1200			Test Limits Apply to Pins 1-12. Design Limits Apply to Pins 23-28, Except for Pin 24 Which is 3X.	μA max
Input Current Low End Point Electrical	I <sub>IL</sub>	-1, 2 -1, 2	400(400)	400				μA max
Output Voltage Range	V <sub>OUT</sub>	-1, 2	10(10) 10(10)			10 10		+ V max - V min
Output Current Range	I <sub>OR</sub>	-1, 2	5(5)				( $\pm$ 10V Output)	mA min
Gain Error End Point Electrical	A <sub>E</sub>	-1 -2 -1, 2	0.1 0.05	0.1 0.2		0.05	With External + 10,000 Ref	± % FSR max <sup>2</sup>
Gain Error Temperature Coefficient	TC <sub>AE</sub>	-1 -2 -1 -2	(40) (20) (10) (5)		10 5		With Internal Reference  With External Reference	± ppm/°C max  ± ppm/°C max
Offset Error End Point Electrical	V <sub>OS</sub>	-1 -2 -1, 2	0.05 0.025	0.05 0.1		0.025		± % FSR max
Bipolar Zero Temperature Coefficient	TCB <sub>PZ</sub>	-1 -2	(10) (5)		10 5		V <sub>BPPS</sub> = ± 10V	± ppm/°C max
Differential Linearity <sup>3</sup> Error End Point Electrical	DLE	-1 -2 -1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Linearity Error <sup>4</sup> End Point Electrical	LE	-1 -2 -1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Linearity Error Temperature Coefficient	TC <sub>LE</sub>	-1 -2	(3/4) (1/2)		3/4 1/2			± LSB max
Positive Summation Error End Point Electrical	E <sub>PE</sub>	-1 -2 -1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Negative Summation Error End Point Electrical	E <sub>NE</sub>	-1 -2 -1, 2	3/4 1/2	3/4 1		1/2		± LSB max
Reference Output	REF <sub>OUT</sub>	-1, 2	9.997 10.003	9.997 10.003			R <sub>L</sub> = 6.8kΩ	V min V max
Power Supply Voltages <sup>3</sup>	V <sub>S</sub>	-1, 2 -1, 2	13.5 16.5					± V min ± V max

Test	Symbol	Device	Design Limit @ +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Power Supply Currents	$I_{EE}$ $I_{CC}$	-1, 2	100 35	100 35	120 35		No Load	- mA max + mA max
Power Supply Gain Sensitivity Delta Gain/ Delta $V_S$ (+ $V_S$ and - $V_S$ )	PSRR	-1, 2	0.0067			0.0067	Input Bits = 1111 1111 1111	± % FS/%
Timing Specifications Chip Select Pulse Width	$t_{AW}$	-1 -2	100				See Figure 2	ns min
Address Select Low Time	$t_{WP}$	-1 -2	100				See Figure 2	ns min
Data Valid Before $\overline{A0}$ Rising Edge	$t_{OW}$	-1 -2	50				See Figure 2	ns min
Data Valid After $\overline{A0}$ Rising Edge	$t_{DH}$	-1 -2	10				See Figure 2	ns min
Chip Select Valid Before $\overline{A1}$ Low	$t_{AS}$	-1 -2	0				See Figure 2	ns min
Output Voltage Settling Time	$t_{SETT}$	-1 -2	8				See Figure 2	μs max

**NOTES**

<sup>1</sup>  $T_A = +25^\circ\text{C}$  and  $\pm V_S = \pm 15\text{V}$  unless otherwise specified.

AD390 can be used with supplies as low as  $\pm 11.4\text{V}$  (see AD390 commercial data sheet).

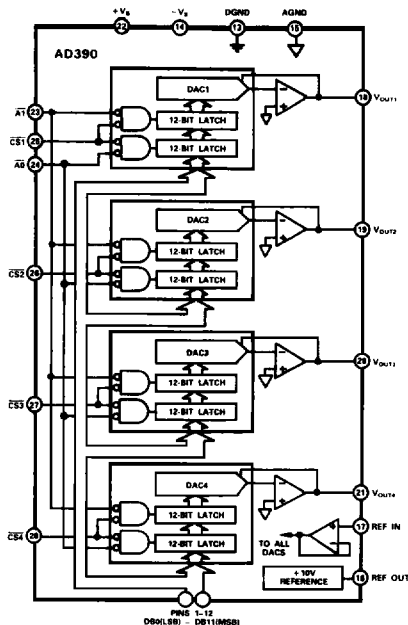
<sup>2</sup> FSR means Full-Scale Range and is equal to 20V for a  $\pm 10\text{V}$  bipolar range.

<sup>3</sup> Monotonicity is tested for over the full military temperature.

<sup>4</sup> Integral Nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.

### 3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



# AD390

## 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (1).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

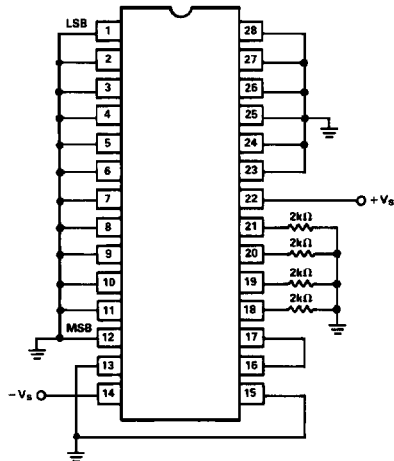


Table 2. AD390 Truth Table

CS1	CS2	CS3	CS4	A1	A0	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC 1
1	0	1	1	1	0	Enable 1st rank of DAC 2
1	1	0	1	1	0	Enable 1st rank of DAC 3
1	1	1	0	1	0	Enable 1st rank of DAC 4
0	1	1	1	0	1	Load DAC 1 second rank from first rank
1	0	1	1	0	1	Load DAC 2 second rank from first rank
1	1	0	1	0	1	Load DAC 3 second rank from first rank
1	1	1	0	0	1	Load DAC 4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table 3. AD390 Analog Output vs. Digital Input ( $\pm V$  Scale)

Digital Input Code	Analog Output Voltage
0000 0000 0000	-10.000V - Full Scale
0100 0000 0000	-5.000V - 1/2 Scale
1000 0000 0000	0.000V Zero
1000 0000 0001	+4.88mV +1LSB
1100 0000 0000	+5.000V +1/2 Scale
1111 1111 1111	+9.9951V + Full Scale - 1LSB

Write Cycle #1 (Load First Rank from Data Bus;  $\overline{A1} = 1$ )

Write Cycle #2 (Load Second Rank from First Rank;  $\overline{A0} = 1$ )

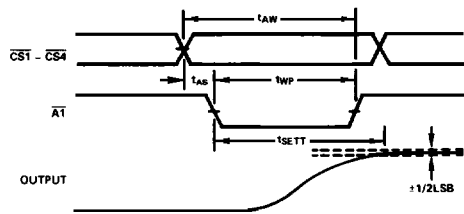
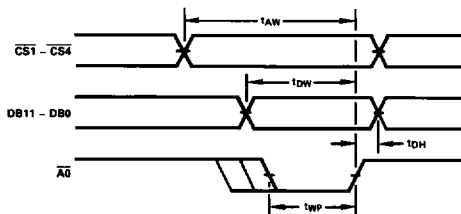


Figure 1. Timing Diagram