

7V to 18V Input, 4.5-A Synchronous Step-Down SWIFT™ Converter with Eco-Mode™

Check for Samples: [TPS54429E](#)

FEATURES

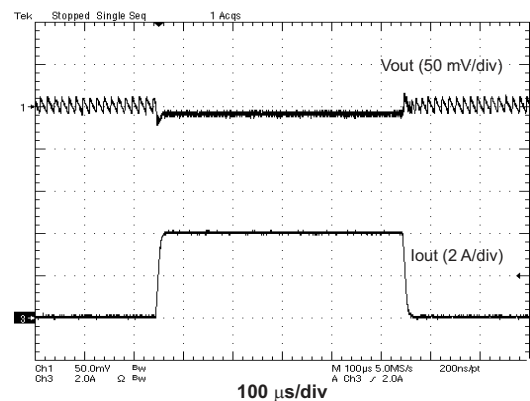
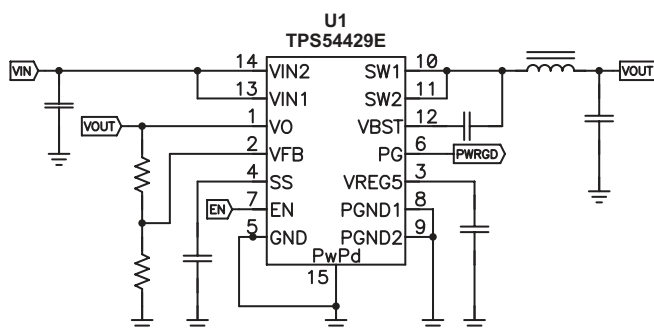
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide V_{IN} Input Voltage Range: 7 V to 18 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications**
 - 63 m Ω (High Side) and 55 m Ω (Low Side)
- **High Efficiency, less than 10 μ A at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **700-kHz Switching Frequency (f_{sw})**
- **Cycle By Cycle Over Current Limit**
- **Power Good Output**
- **Auto-Skip Eco-mode™ for High Efficiency at Light Load**

APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
 - Digital TV Power Supply
 - High Definition Blu-ray Disc™ Players
 - Networking Home Terminal
 - Digital Set Top Box (STB)

DESCRIPTION

The TPS54429E is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54429E enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54429E uses the D-CAP2™ mode control which provides a very fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light load loads. Eco-mode™ allows the TPS54429E to maintain high efficiency during lighter load conditions. The TPS54429E also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP, SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 7-V to 18-V V_{IN} input. The output voltage can be programmed between 0.76V and 5.5V. The device also features an adjustable soft start time and a power good function. The TPS54429E is available in the 14-pin HTSSOP package and the 16 pin QFN package, designed to operate from -20°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP2, Eco-mode, PowerPAD are trademarks of Texas Instruments.

Blu-ray Disc is a trademark of Blu-ray Disc Association.

TPS54429E

SLVSAS0 – FEBRUARY 2011

www.ti.com



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾ ⁽³⁾	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA
-20°C to 85°C	PowerPAD™ (HTSSOP) – PWP	TPS54429EPWP	14	Tube
		TPS54429EPWPR		Tape and Reel
	Plastic Quad Flat Pack (QFN)	TPS54429ERSAT	16	Tape and Reel
		TPS54429ERSAR		Tape and Reel

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) All package options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE		UNIT	
		MIN	MAX		
V _I	Input voltage range	V _{IN1} , V _{IN2} , EN	-0.3	20	V
		V _{BST}	-0.3	26	
		V _{BST} (10 ns transient)	-0.3	28	
		V _{FB} , V _O , SS, PG	-0.3	6.5	
		SW1, SW2	-2	20	
		SW1, SW2 (10 ns transient)	-3	22	
V _O	Output voltage range	V _{REG5}	-0.3	6.5	
		P _{GND1} , P _{GND2}	-0.3	0.3	
V _{diff}	Voltage from GND to POWERPAD	-0.2	0.2		
ESD rating	Electrostatic discharge	Human Body Model (HBM)		2	kV
		Charged Device Model (CDM)		500	V
T _J	Operating junction temperature	-20	150	°C	
T _{stg}	Storage temperature	-55	150		

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS54426		UNITS
		PWP (14) PINS	RSA (16) PINS	
θ _{JA}	Junction-to-ambient thermal resistance	55.6	37.3	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	51.3	42.5	
θ _{JB}	Junction-to-board thermal resistance	36.4	14.9	
ψ _{JT}	Junction-to-top characterization parameter	1.8	0.8	
ψ _{JB}	Junction-to-board characterization parameter	20.6	14.8	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	4.3	4.9	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{IN}	Supply input voltage range	7	18	V	
V _I	Input voltage range	VBST	-0.3	24	V
		VBST (10 ns transient)	-0.3	27	
		SS, PG	-0.1	5.7	
		EN	-0.1	18	
		VO, VFB	-0.1	5.5	
		SW1, SW2	-1.8	18	
		SW1, SW2 (10 ns transient)	-3	21	
	PGND1, PGND2	-0.1	0.1		
V _O	Output voltage range	VREG5	-0.1	5.7	V
I _O	Output Current range	I _{VREG5}	0	10	mA
T _A	Operating free-air temperature	-20	85	°C	
T _J	Operating junction temperature	-20	150	°C	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN}	Operating - non-switching supply current	V _{IN} current, T _A = 25°C, EN = 5 V, V _{F_B} = 0.8 V		850	1300	μA
I _{VINSDN}	Shutdown supply current	V _{IN} current, T _A = 25°C, EN = 0 V		1.8	10	μA
LOGIC THRESHOLD						
V _{ENH}	EN high-level input voltage	EN	2			V
V _{ENL}	EN low-level input voltage	EN			0.48	V
V_{F_B} VOLTAGE AND DISCHARGE RESISTANCE						
V _{F_B} TH	V _{F_B} threshold voltage	V _{F_B} voltage light load mode, T _A = 25°C, V _O = 1.05 V, I _O = 10mA		771		mV
		T _A = 25°C, V _O = 1.05 V, continuous mode	757	765	773	
		T _A = 0°C to 85°C, V _O = 1.05 V, continuous mode ⁽¹⁾	753		777	
		T _A = -20°C to 85°C, V _O = 1.05 V, continuous mode ⁽¹⁾	751		779	
I _{V_{F_B}}	V _{F_B} input current	V _{F_B} = 0.8 V, T _A = 25°C		0	±0.1	μA
R _{Dischg}	V _O discharge resistance	EN = 0 V, V _O = 0.5 V, T _A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V _{V_{REG5}}	V _{REG5} output voltage	T _A = 25°C, 7 V < V _{IN} < 18 V, 0 < I _{V_{REG5}} < 5 mA	5.3	5.5	5.7	V
V _{LN5}	Line regulation	7 V < V _{IN} < 18 V, I _{V_{REG5}} = 5 mA			20	mV
V _{LD5}	Load regulation	0 mA < I _{V_{REG5}} < 5 mA			100	mV
I _{V_{REG5}}	Output current	V _{IN} = 7 V, V _{REG5} = 4 V, T _A = 25°C		70		mA
MOSFET						
R _{dsonh}	High side switch resistance	25°C, V _{BST} - SW1,2 = 5.5 V		63		mΩ
R _{dsonl}	Low side switch resistance	25°C		55		mΩ

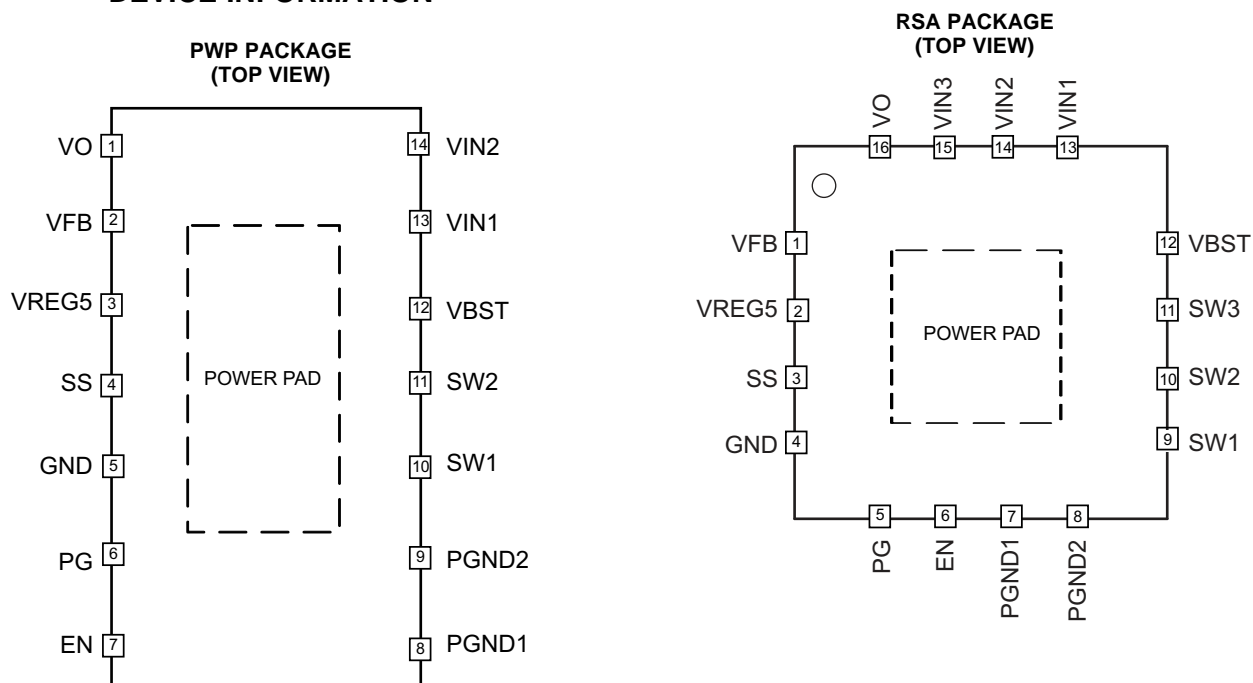
(1) Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

 over operating free-air temperature range, $V_{IN} = 12V$ (unless otherwise noted)

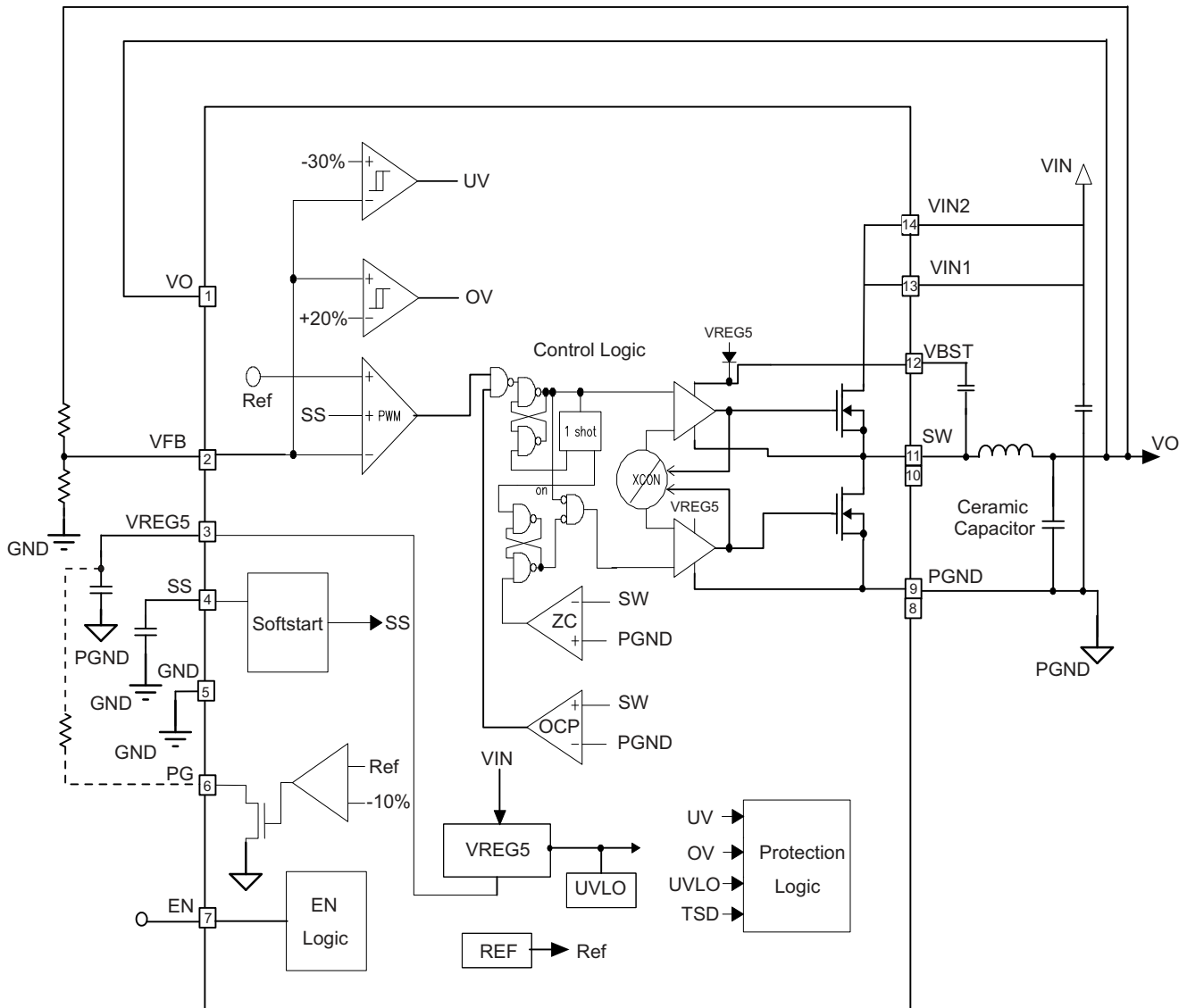
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{ocL}	Current limit	$L_{OUT} = 1.5 \mu H^{(2)}$, $T_A = -20^\circ C$ to $85^\circ C$	5.2	5.9	8.0	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽²⁾	165			°C
		Hysteresis ⁽²⁾	30			
ON-TIME TIMER CONTROL						
T_{ON}	On time	$V_{IN} = 12 V$, $V_O = 1.05 V$	145			ns
$T_{OFF(MIN)}$	Minimum off time	$T_A = 25^\circ C$, $V_{FB} = 0.7 V$	260	310	ns	
SOFT START						
I_{SSC}	SS charge current	$V_{SS} = 0 V$	1.4	2.0	2.6	μA
I_{SSD}	SS discharge current	$V_{SS} = 0.5 V$	0.1	0.2	mA	
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (good)	85	90	95	%
		V_{FB} falling (fault)	85			%
I_{PG}	PG sink current	$PG = 0.5 V$	2.5	5	mA	
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115	120	125	%
T_{OVPDEL}	Output OVP prop delay		10			μs
V_{UVP}	Output UVP trip threshold	UVP detect	60	65	70	%
		Hysteresis	10			%
T_{UVPDEL}	Output UVP delay		0.25			ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time	x 1.7			
UVLO						
V_{UVLO}	UVLO threshold	Wake up V_{REG5} voltage	3.5	3.8	4.1	V
		Hysteresis V_{REG5} voltage	0.23	0.35	0.47	

(2) Not production tested.

DEVICE INFORMATION

PIN FUNCTIONS

NAME	PIN NUMBER		DESCRIPTION
	PWP 14	RSA 16	
VO	1	16	Connect to output of converter. This terminal is used for On-Time Adjustment.
VFB	2	1	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	2	5.5 V power supply output. A capacitor (typical 1 μ F) should be connected to GND. VREG5 is not active when EN is low.
SS	4	3	Soft-start control. A external capacitor should be connected to GND.
GND	5	4	Signal ground pin.
PG	6	5	Open drain power good output.
EN	7	6	Enable control input. EN is active high and must be pulled up to enable the device.
PGND1, PGND2	8, 9	7, 8	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	9, 10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN1, VIN2	13, 14	13, 14, 15	Power input and connected to high side NFET drain. Supply input for 5-V internal linear regulator for the control circuitry.
PowerPAD™ or Thermal Pad	Back side	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



A. The block diagram shown is for the PWP 14 pin package. The QFN 16 pin package block diagram is identical except for the pin out.

OVERVIEW

The TPS54429E is a 4.5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs and auto-skip Eco-mode™ to improve light load efficiency. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54429E is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. The MOSFET is turned off after the internal one-shot timer expires. The one-shot timer is set by the converter input voltage, V_{IN} , and the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54429E uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54429E runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. The actual frequency may vary from 700 kHz depending on the off time, which is ended when the fed back portion of the output voltage falls to the VFB threshold voltage.

Auto-Skip Eco-Mode™ Control

The TPS54429E is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in [Equation 1](#).

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot f_{sw}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 2 μ A current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in [Equation 2](#). VFB voltage is 0.765 V and SS pin source current is 2 μ A.

$$T_{SS}(ms) = \frac{C6(nF) \cdot V_{ref}}{I_{SS}(\mu A)} = \frac{C6(nF) \cdot 0.765}{2} \quad (2)$$

The TPS54429E contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by $(1-D)$, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (V_O) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Power Good

The TPS54429E has power-good open drain output. The power good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage is within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. If the PG output is pulled up to VREG5, the resistor value, which is connected between PG and VREG5, must be in the range of 20k ohm to 150k ohm. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after a 5 μ s internal delay.

VREG5

VREG5 is an internally generated voltage source used by the TPS54429E. It is derived directly from the input voltage and is nominally regulated to 5.5 V when the input voltage is above 5.6 V. The output of the VREG5 regulator is the input to the internal UVLO function. VREG5 must be above the UVLO wake up threshold voltage (3.8 V typical) for the TPS54429E to function. Connect a 1.0 μ F capacitor between pin 3 of the TPS54429E and power ground for proper regulation of the VREG5 output. The VREG5 output voltage is available for external use and can typically source up to 70 mA. The VREG5 output is disabled when the TPS54429E EN pin is open or pulled low.

Output Discharge Control

TPS54429E discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The output is discharged by an internal 50- Ω MOSFET which is connected from V_O to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT} . If the measured voltage is above the voltage proportional to the current limit, the device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current one half of the peak-to-peak inductor current higher than the overcurrent threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output under-voltage protection circuit to be activated. When the overcurrent condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

Over/Under Voltage Protection

The TPS54429E detects over and undervoltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on. When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 μ s, the device latches off both internal top and bottom MOSFET.

UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54429E is shut off. This protection is non-latching.

Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 165°C), the TPS54429E shuts off. This protection is non-latching.

TYPICAL CHARACTERISTICS

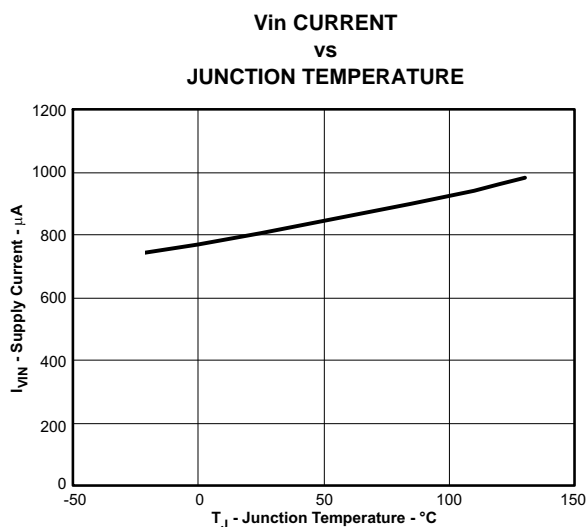


Figure 1.

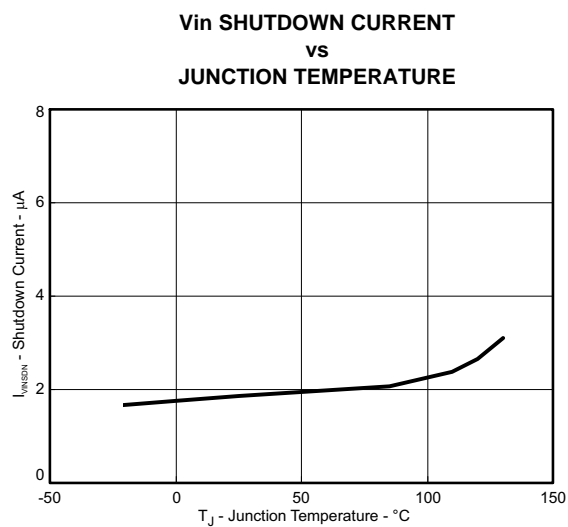


Figure 2.

TYPICAL CHARACTERISTICS (continued)

EN CURRENT
vs
EN VOLTAGE

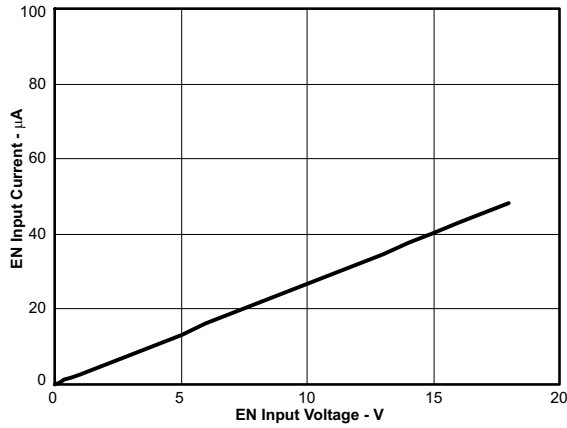


Figure 3.

1.05V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

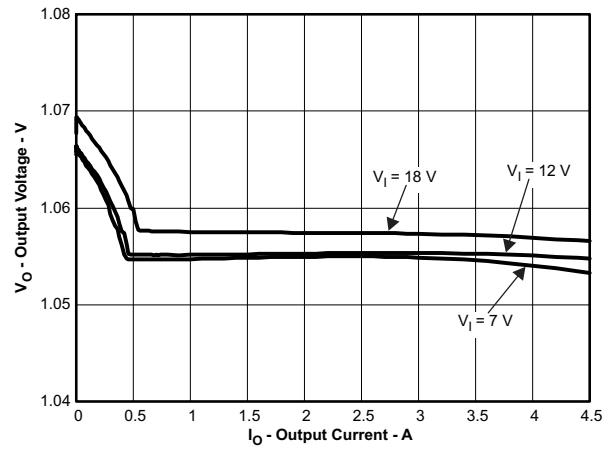


Figure 4.

1.05V OUTPUT VOLTAGE
vs
INPUT VOLTAGE

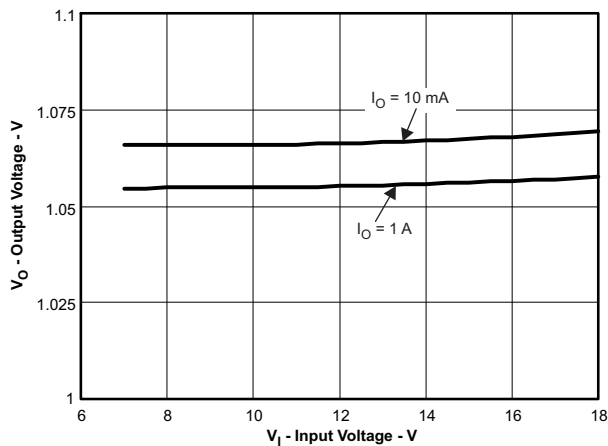


Figure 5.

1.05V 50mA to 4A LOAD TRANSIENT RESPONSE

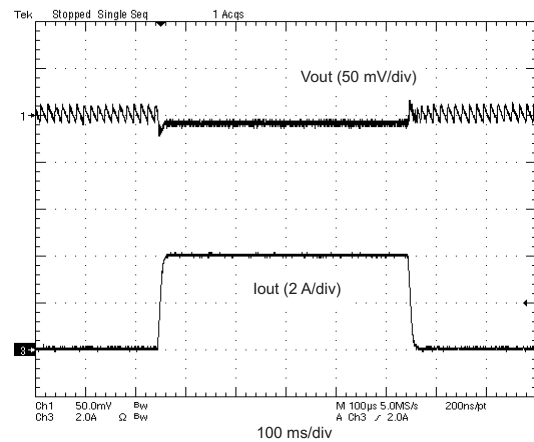
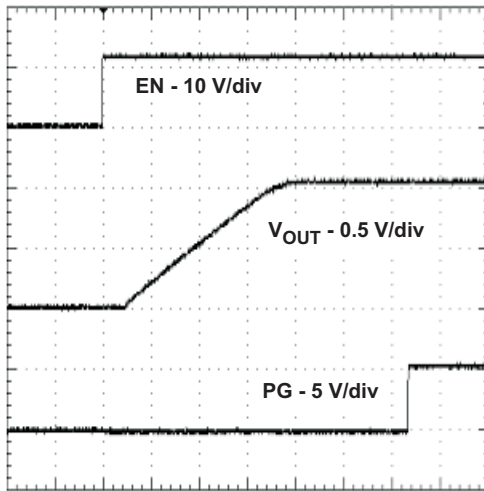


Figure 6.

TYPICAL CHARACTERISTICS (continued)

STARTUP WAVEFORM



400 μs/div

Figure 7.

EFFICIENCY
vs
OUTPUT CURRENT

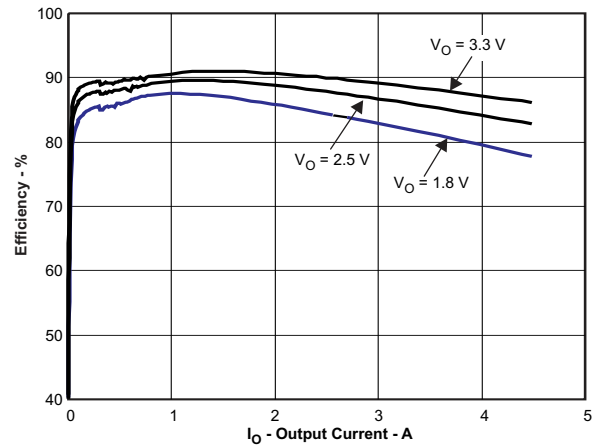


Figure 8.

LIGHT LOAD EFFICIENCY
vs
OUTPUT CURRENT

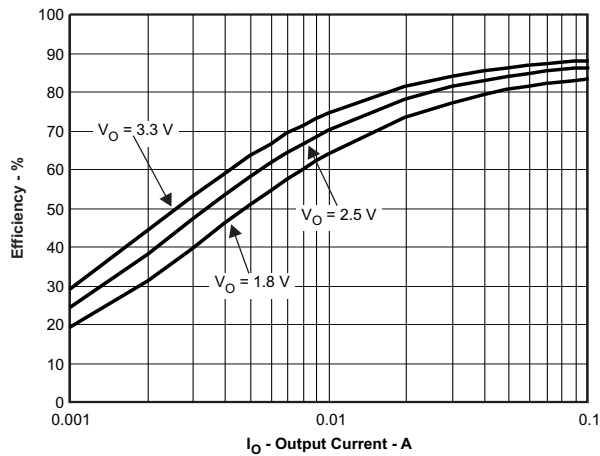


Figure 9.

SWITCHING FREQUENCY
vs
INPUT VOLTAGE (I_O=1A)

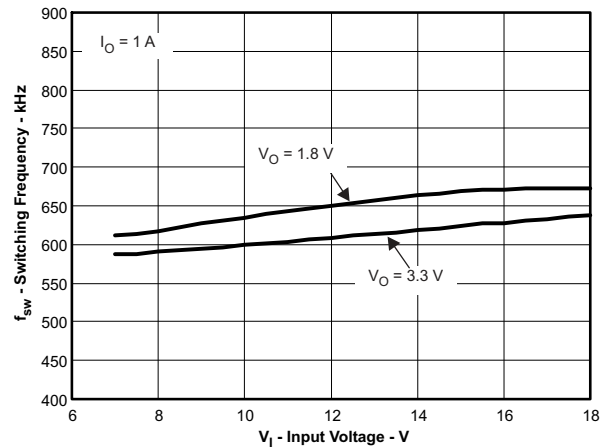


Figure 10.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY
vs
OUTPUT CURRENT

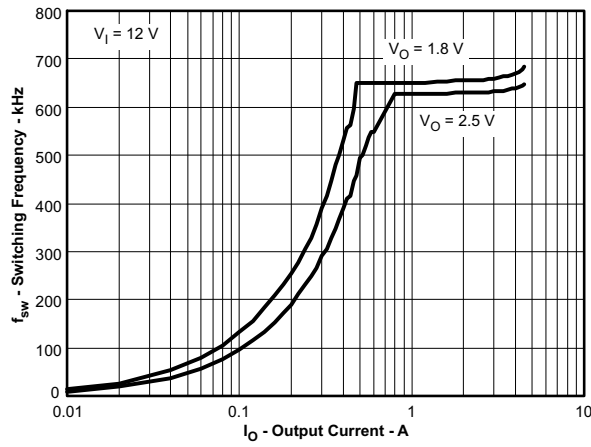
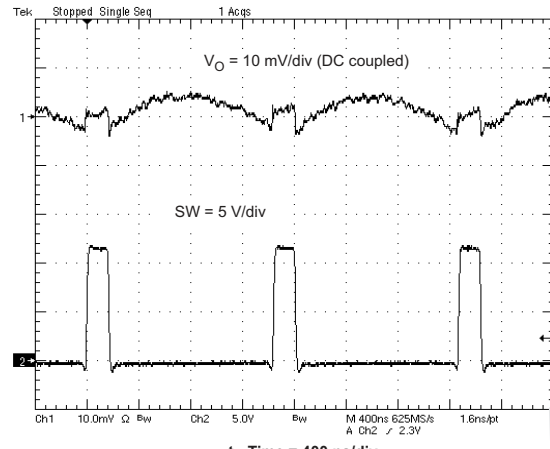


Figure 11.

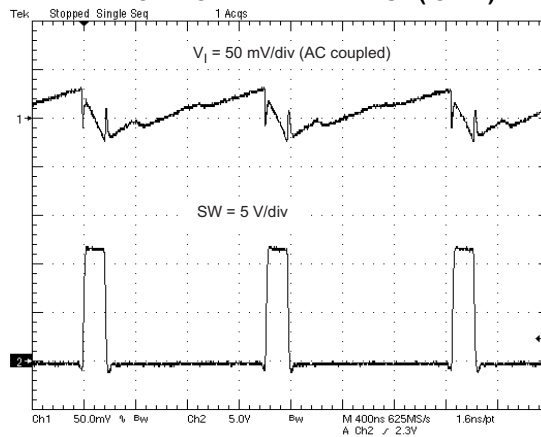
VOLTAGE RIPPLE AT OUTPUT ($I_o=4A$)



t - Time = 400 ns/div

Figure 12.

VOLTAGE RIPPLE AT INPUT ($I_o=4A$)



t - Time = 400 ns/div

Figure 13.

DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

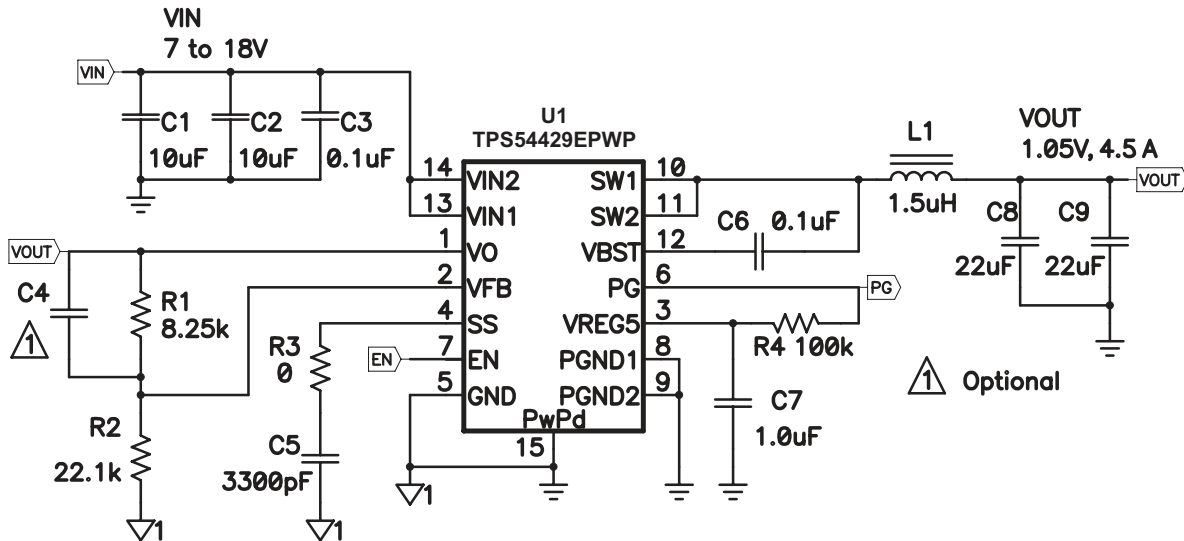


Figure 14. Schematic Diagram for This Design Example

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 and Equation 4 to calculate V_{OUT}

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \cdot \left(1 + \frac{R1}{R2}\right) \quad (3)$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \cdot V_{OUT_SET}) \cdot \left(1 + \frac{R1}{R2}\right) \quad (4)$$

Where:

V_{OUT_SET} = Target V_{OUT} voltage

Output Filter Selection

The output filter used with the TPS54429E is an LC circuit. This LC filter has double pole at:

$$F_p = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \quad (5)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54429E. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 5 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

Table 1. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF) ⁽¹⁾	L1 (μH)	C8 + C9 (μF)
1	6.81	22.1		1.5	22 - 68
1.05	8.25	22.1		1.5	22 - 68
1.2	12.7	22.1		1.5	22 - 68
1.5	23.2	22.1		1.5	22 - 68
1.8	30.1	22.1	10 - 22	2.2	22 - 68
2.5	49.9	22.1	10 - 22	2.2	22 - 68
3.3	73.2	22.1	10 - 22	2.2	22 - 68
5	121	22.1	10 - 22	3.3	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 6, Equation 7 and Equation 8. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for f_{SW} .

$$I_{lp} - p = \frac{V_{OUT}}{V_{IN(max)}} \cdot \frac{V_{IN(max)} - V_{OUT}}{L_O \cdot f_{SW}} \quad (6)$$

$$I_{lpeak} = I_O + \frac{I_{lp} - p}{2} \quad (7)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} (I_{lp} - p)^2} \quad (8)$$

For this design example, the calculated peak current is 4.97A and the calculated RMS current is 4.508 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54429E is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22μF to 68μF. Use Equation 9 to determine the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_O \cdot f_{SW}} \quad (9)$$

For this design two TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is .271A and each output capacitor is rated for 4A.

Input Capacitor Selection

The TPS54429E requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1.0 μF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

THERMAL INFORMATION

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. [SLMA002](#) and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. [SLMA004](#).

The exposed thermal pad dimensions for this package are shown in the following illustration.

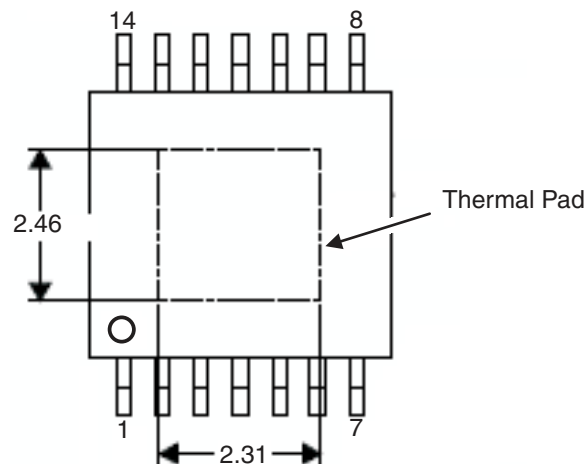


Figure 15. Thermal Pad Dimensions

LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. VIN Capacitor should be placed as near as possible to the device.

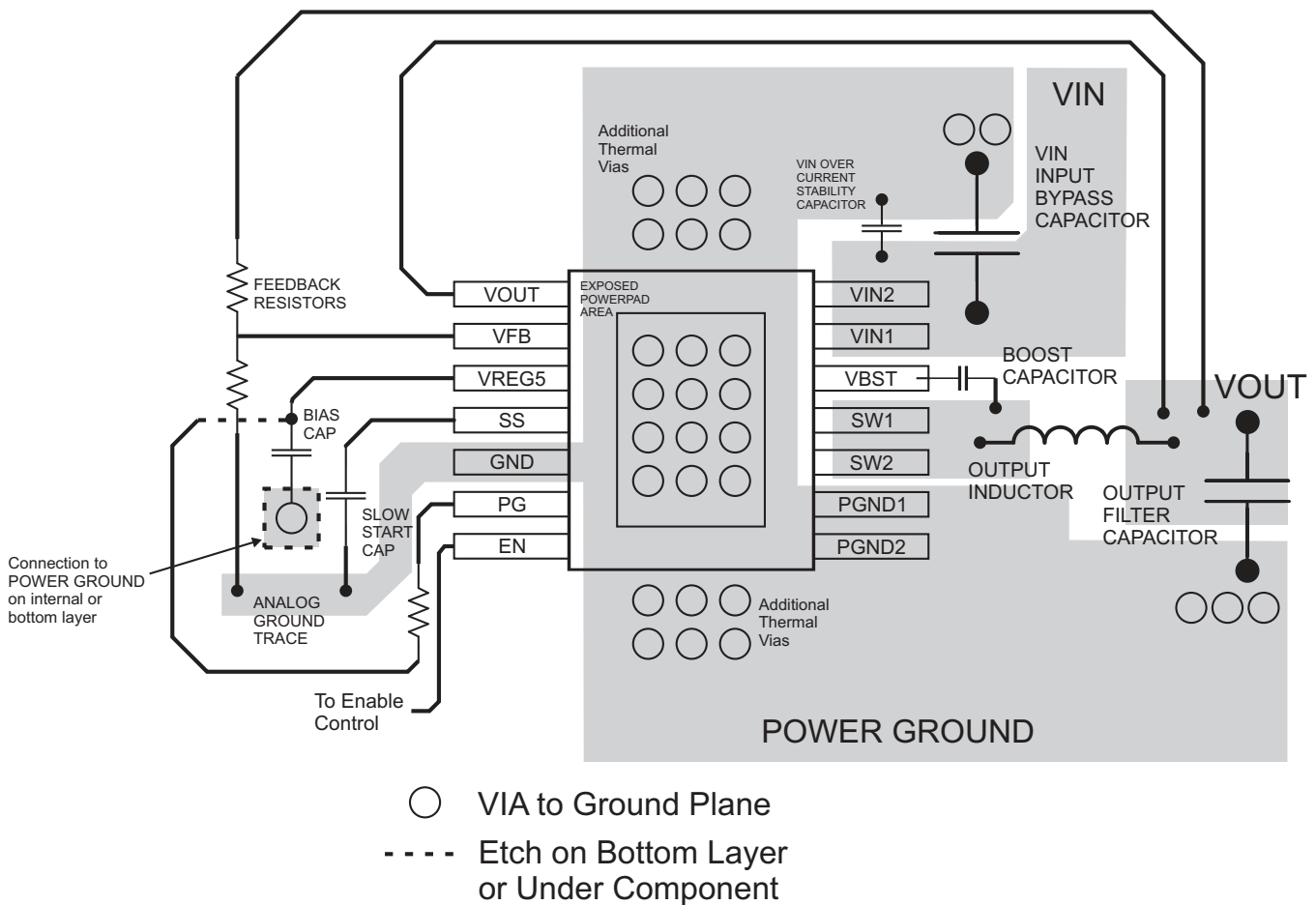


Figure 16. PCB Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54429EPWP	ACTIVE	HTSSOP	PWP	14		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 85	54429E	Samples
TPS54429EPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 85	54429E	Samples
TPS54429ERSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 85	TPS 54429E	Samples
TPS54429ERSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 85	TPS 54429E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54429EPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54429ERSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54429ERSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

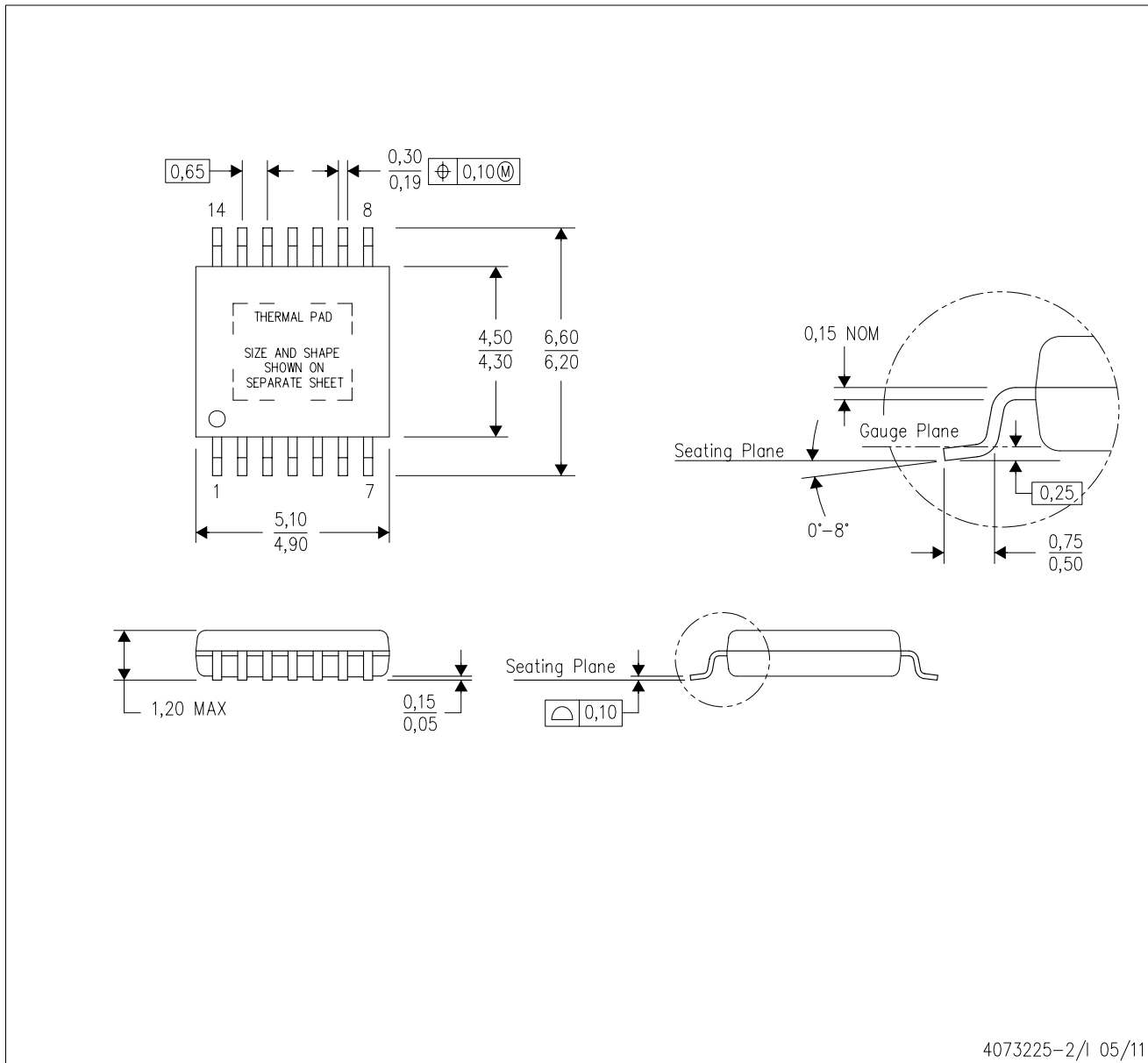

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54429EPWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS54429ERSAR	QFN	RSA	16	3000	367.0	367.0	35.0
TPS54429ERSAT	QFN	RSA	16	250	210.0	185.0	35.0

MECHANICAL DATA

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

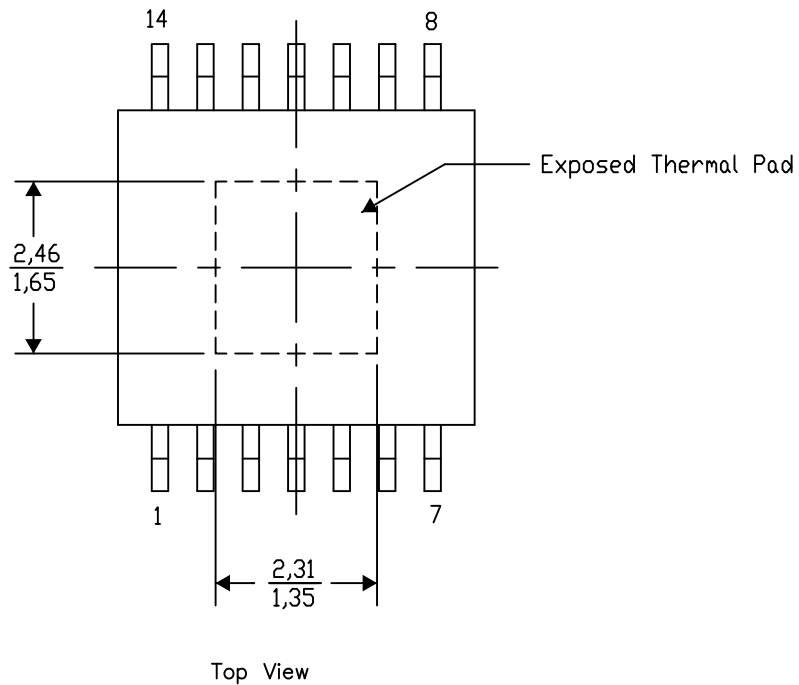
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

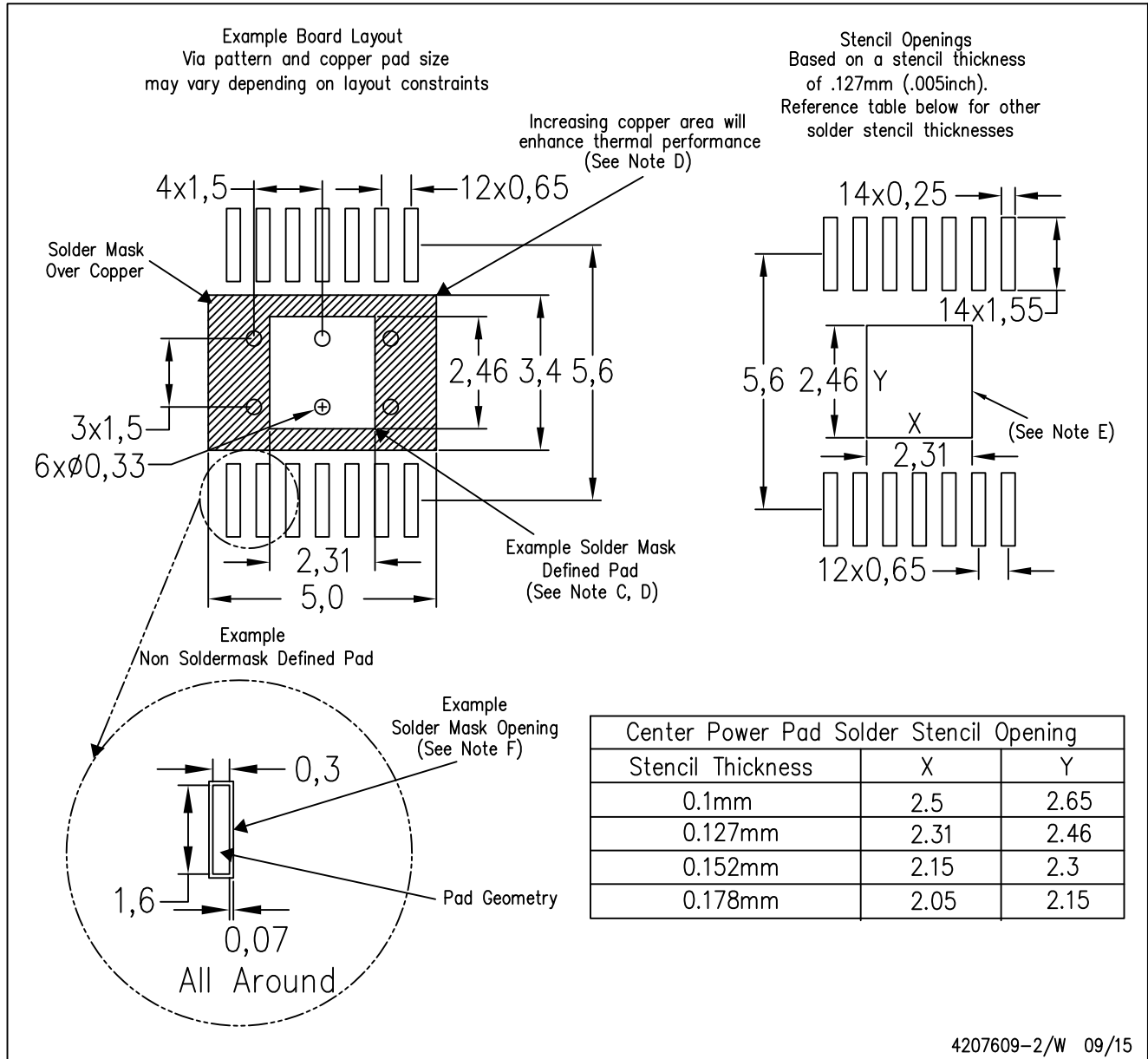
4206332-2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-2/W 09/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

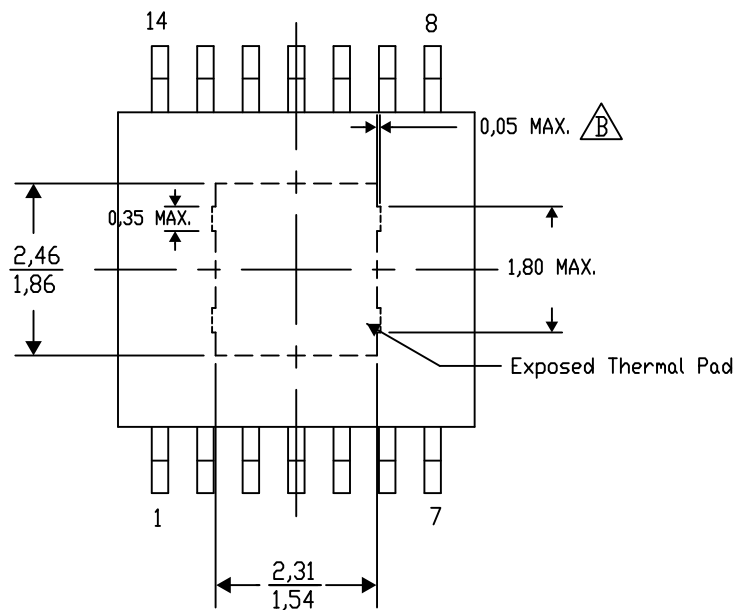
PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332-44/AO 01/16

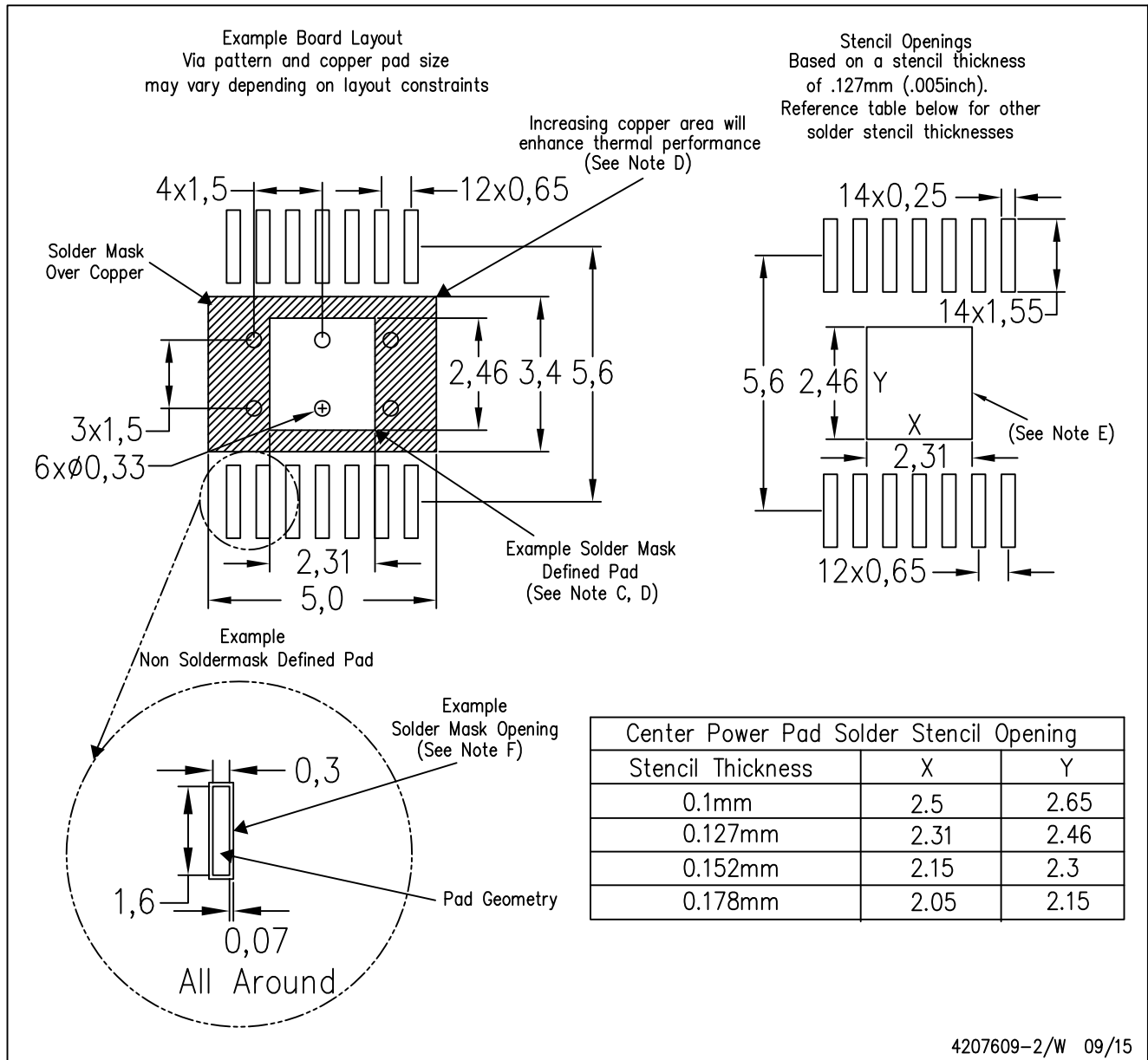
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE

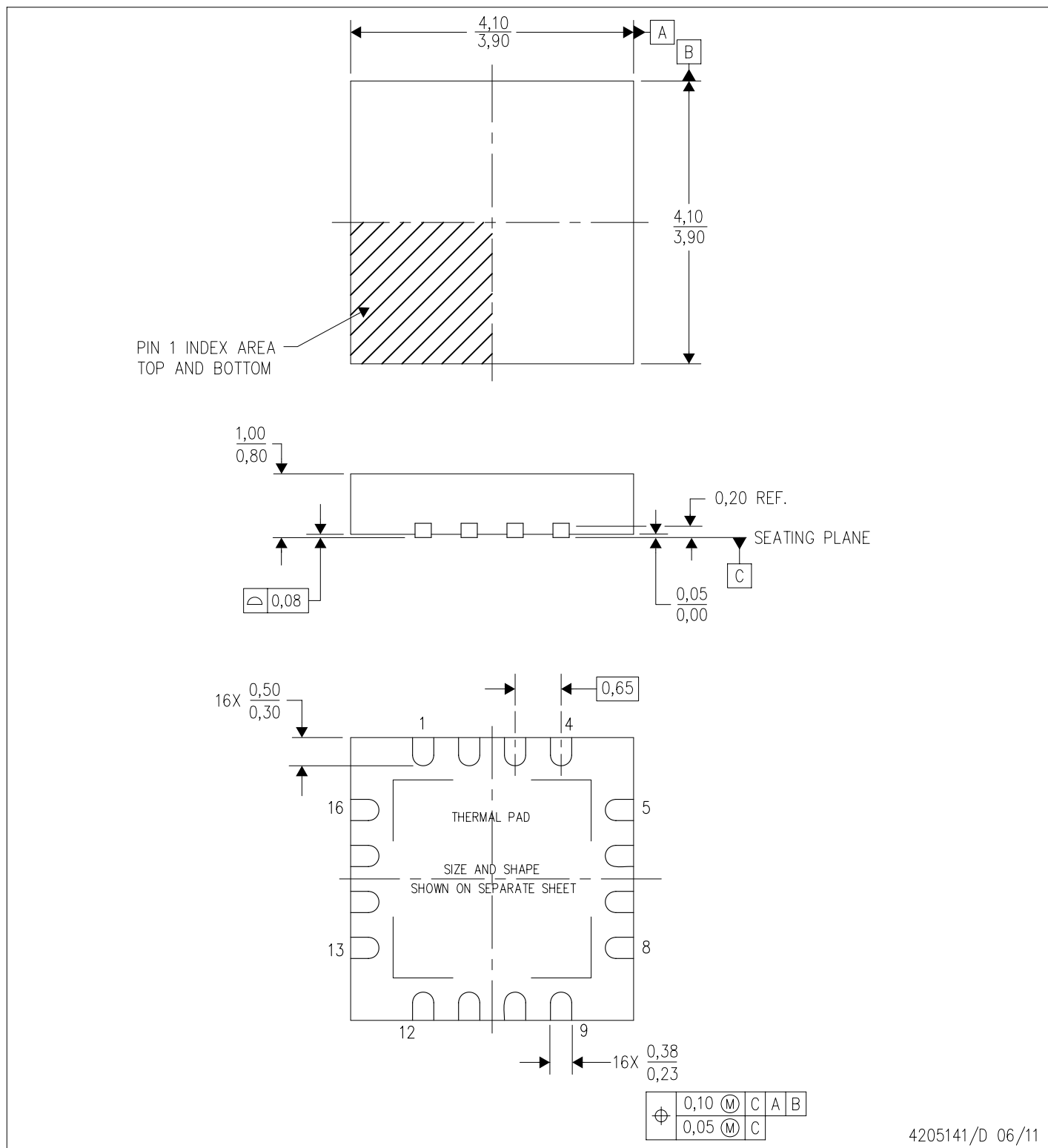


4207609-2/W 09/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205141/D 06/11

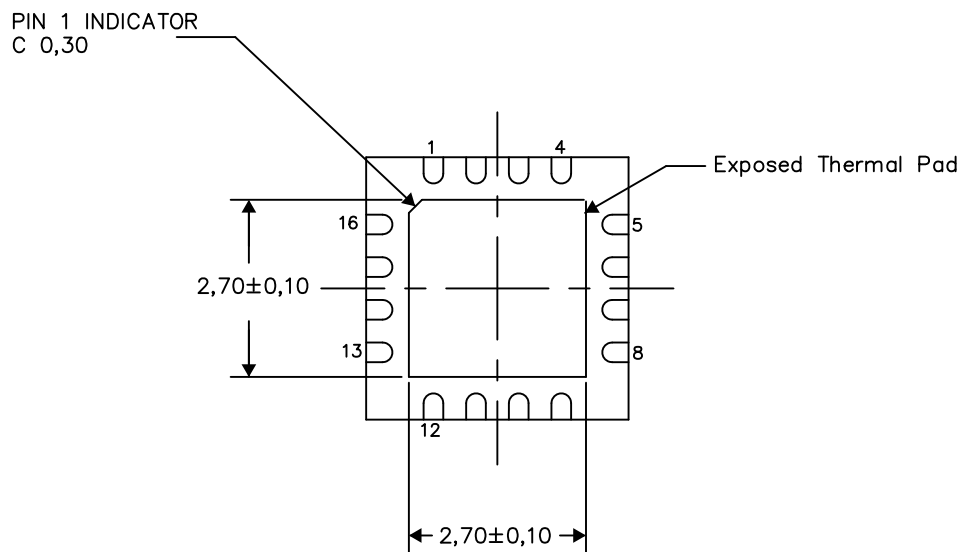
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

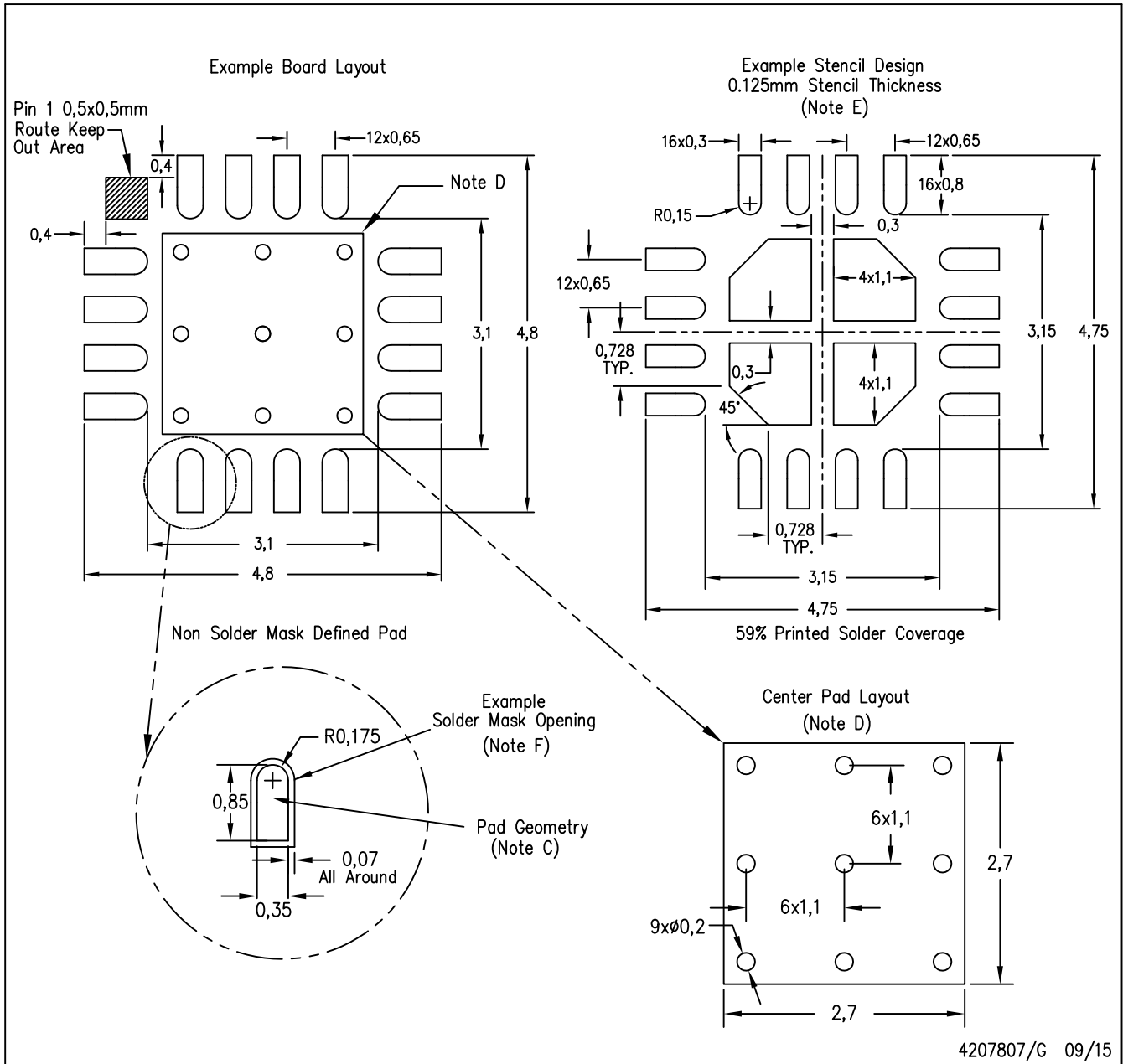
4206364-2/0 09/15

NOTES:

A. All linear dimensions are in millimeters

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.