= Preliminary =

AK09940

Ultrahigh precision 3-axis Electronic Magnetometer

1. General Description

AK09940 is ultrahigh precision 3-axis electronic magnetometer IC with ultrahigh sensitive TMR sensor technology.
Small package of AK09940 incorporates magnetic sensors for detecting magnetic field in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self-test function is also incorporated.

2. Features

- Functions:
  - 3-axis magnetometer device
  - Built-in A to D Converter for magnetometer data out
  - 18-bit data out for each 3-axis magnetic component
    - Sensitivity: 10 nT/LSB (typ.)
    - Range: ±1200 μT (max.)
  - Serial interface
    - I^2C bus interface
      Standard and Fast modes compliant with Philips I^2C specification Ver.2.1
    - 4-wire SPI
  - Operation mode
    - Power-down, Single measurement, Continuous measurement and Self-test
  - DRDY function for measurement data ready
  - Magnetic sensor overflow monitor function
  - Built-in oscillator for internal clock source
  - Power on Reset circuit
  - Self-test function with internal magnetic source
  - Built-in temperature sensor
  - Built-in magnetic sensitivity adjustment circuit
  - 8 FIFO data buffer
  - Selectable sensor drive
    - Low power drive / Low noise drive

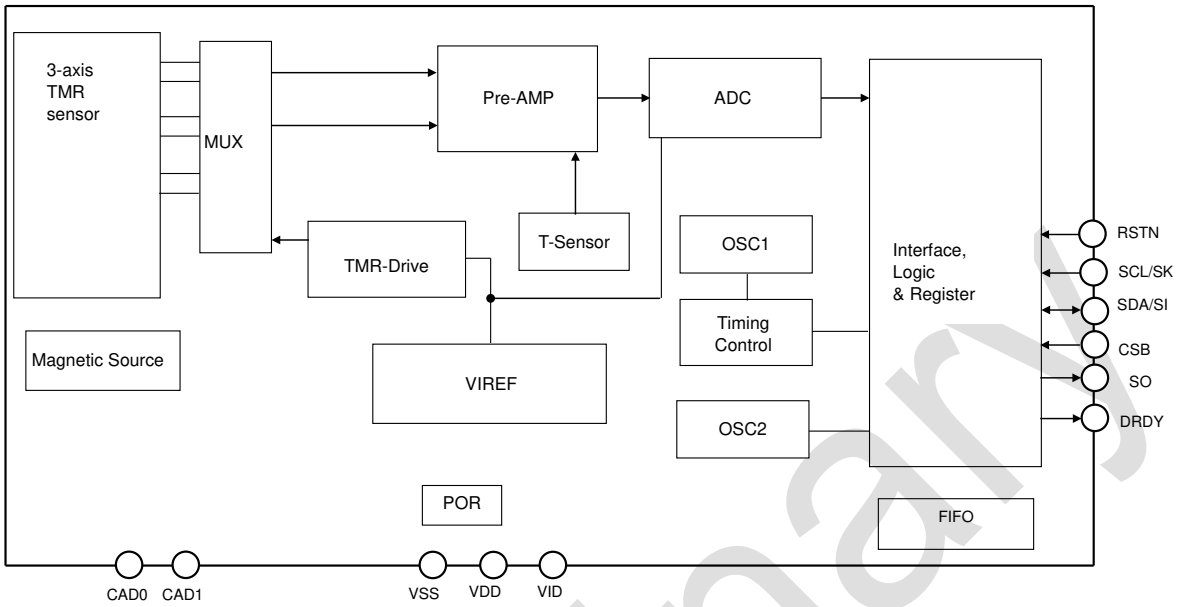
- Operating temperatures:
  - -30˚C to +85˚C
- Operating supply voltage:
  - Analog power supply +1.7 V to +1.98 V
  - Digital Interface supply +1.65 V to analog power supply voltage
- Current consumption:
  - Power-down: 0.5 μA (typ.)
  - Measurement:
    - Average current consumption at 100 Hz repetition rate
      - Low power drive 1: 0.03 mA (typ.)
      - Low power drive 2: 0.06 mA (typ.)
      - Low noise drive 1 : 0.10 mA (typ.)
      - Low noise drive 2 : 0.20 mA (typ.)

- Package:
  AK09940 11-pin LGA: 1.6 mm × 1.6 mm × 0.58 mm (typ.)

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram



4.2. Functions

Block	Function
3-axis TMR sensor	TMR elements.
MUX	Multiplexer for selecting TMR elements.
TMR-Drive	Magnetic sensor drive circuit.
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
T-Sensor	Temperature sensor. Generates a voltage in proportion to temperature.
ADC	Amplifies Pre-AMP output or T-Sensor output and performs analog-to-digital conversion.
OSC1	Generates an operating clock for sensor measurement.
OSC2	Generates an operating periodic clock for sequencer.
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
VIREF	Generates reference voltage and current.
Interface Logic & Register	Exchanges data with an external CPU. DRDY pin indicates sensor measurement has ended and data is ready to be read. I^2C bus interface using two pins, namely, SCL and SDA. Standard and Fast modes are supported. The low-voltage specification can be supported by applying 1.65 V to the VID pin. 4-wire SPI is also supported by SK, SI, SO and CSB pins. 4-wire SPI works in VID pin voltage down to 1.65 V, too.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC1.
Magnetic Source	Generates magnetic field for self-test of magnetic sensor.
FIFO	The buffer is capable up to 8 sets of data.

5. Pin Configurations and Functions

Pin No.	Pin name	I/O	Power supply	Type	Function
A1	DRDY	O	VID	CMOS	Data Ready output pin. "H" active. Informs measurement ended and data is ready to be read.
A2	CSB	I	VID	CMOS	Chip select pin for 4-wire SPI. "L" active. Connect to VID when selecting I²C bus interface.
A3	SCL	I	VID	CMOS	When the I²C bus interface is selected (CSB pin is connected to VID). SCL: Control clock input pin. Input: Schmitt trigger.
	SK				When the 4-wire SPI is selected. SK: Serial clock input pin.
A4	SDA	I/O	VID	CMOS	When the I²C bus interface is selected (CSB pin is connected to VID). SDA: Control data input/output pin. Input: Schmitt trigger, Output: Open drain.
	SI	I			When the 4-wire SPI is selected. SI: Serial data input pin.
B1	VDD	-	-	Power	Positive power supply pin.
B4	SO	O	VID	CMOS	When the I²C bus interface is selected (CSB pin is connected to VID). Hi-Z output. Keep this pin electrically non-connected.
					When the 4-wire SPI is selected. Serial data output pin.
C1	VSS	-	-	Power	Ground pin.
C4	VID	-	-	Power	Digital interface positive power supply pin.
D1	CAD0	I	VID	CMOS	When the I²C bus interface is selected (CSB pin is connected to VID). CAD0: Slave address 0 input pin. Connect to VSS or VID.
					When the 4-wire serial interface is selected. Connect to VSS.
D2	CAD1	I	VID	CMOS	When the I²C bus interface is selected (CSB pin is connected to VID). CAD1: Slave address 1 input pin. Connect to VSS or VID.
					When the 4-wire serial interface is selected. Connect to VSS.
D4	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to "L". Connect to VID when not in use.

6. Absolute Maximum Ratings

Vss = 0 V

Parameter	Symbol	Condition	Min.	Max.	Unit
Power supply voltage (Vdd, Vid)	V+		-0.3	+2.5	V
Input voltage (except for power supply pin)	VIN		-0.3	(V+)+0.3	V
Input current (except for power supply pin)	IIN		-10	+10	mA
Storage temperature	Tst		-40	+125	˚C
External magnetic field	Hext	Ta = 25˚C Less than 3 seconds		TBD	mT

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

Vss = 0 V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-30		+85	˚C
Power supply voltage	VDD pin voltage	Vdd	1.7	1.8	1.98	V
	VID pin voltage	Vid	1.65	1.8	Vdd	V

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd = 1.7 V to 1.98 V, Vid = 1.65 V to Vdd, Temperature range = -30˚C to 85˚C
Typical condition: Vdd = Vid = 1.8 V, Temperature = 25˚C

8.1. DC Characteristics

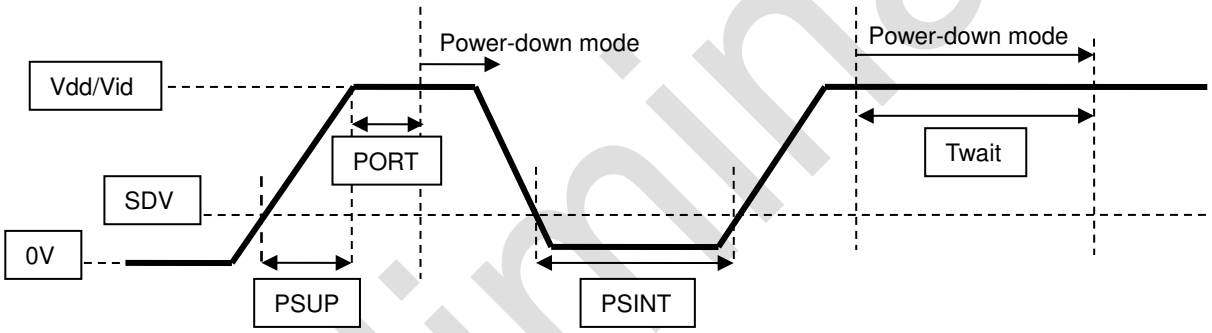
Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	CSB RSTN SK/SCL SI/SDA CAD0 CAD1		70%Vid		Vid+0.3	V
Low level input voltage	VIL			-0.3		30%Vid	V
Input current	IIN		Vin = Vss or Vid	-10		+10	µA
Hysteresis input voltage (* 1)	VHS	SCL SDA		10%Vid			V
High level output voltage	VOH	SO DRDY	IOH ≥ -100 µA	80%Vid			V
Low level output voltage 1	VOL1		IOL1 ≤ +100 µA			20%Vid	V
Low level output voltage 2 (* 2)	VOL2	SDA	IOL2 ≤ +3 mA			20%Vid	V
Current consumption (* 3)	IDD1	VDD VID	Power-down mode Vdd = Vid = 1.8 V		0.5	6.0	µA
	IDD2		When magnetic sensor is driven		0.8	1.1	mA
	IDD3		Self-test mode		1.9	2.5	mA
	IDD4		When temperature sensor is driven		0.7	0.9	mA
	IDD5		(* 4)		0.2	5.0	µA

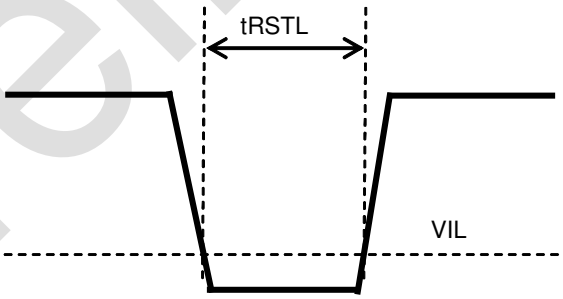
Notes:
* 1. Schmitt trigger input (reference value for design).
* 2. Output is open-drain. Connect a pull-up resistor externally.
* 3. Without any resistance load.
* 4. (case 1) Vdd = ON, Vid = ON, RSTN pin = “L”.
(case 2) Vdd = ON, Vid = OFF (0 V), RSTN pin = “L”.
(case 3) Vdd = OFF (0 V), Vid = ON.

8.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2 V to Vdd (Vid).			50	ms
POR completion time (* 5)	PORT		Period of time after PSUP to Power-down mode (* 6)			100	µs
Power supply turn off voltage (* 5)	SDV	VDD VID	Turn off voltage to enable POR to restart (* 6)			0.2	V
Power supply turn on interval (* 5)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (* 6)	100			µs
Wait time before mode setting	Twait			100			µs
Reset input effective pulse width (“L”)	tRSTL	RSTN		5			µs

Notes:
* 5. Reference value for design.
* 6. When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK09940 transits to Power-down mode.





8.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT		-	18	-	Bit
Time for measurement	TSM	MT[1:0] = “00”		0.6	0.7	ms
		MT[1:0] = “01”		0.9	1.0	
		MT[1:0] = “10”		1.5	1.7	
		MT[1:0] = “11”		2.8	3.1	
Magnetic sensor sensitivity	BSE	Ta = 25˚C		10		nT/LSB
Magnetic sensor measurement range (* 7)	BRG	Ta = 25˚C Each Axis		±1200		µT
Magnetic sensor initial offset (* 8)	BOF	Ta = 25˚C	TBD		TBD	LSB
RMS noise (* 7)	NIS	MT[1:0] = “00”		70		nT rms
		MT[1:0] = “01”		60		
		MT[1:0] = “10”		50		
		MT[1:0] = “11”		40		

Notes:
* 7. Reference value for design.
* 8. Value of measurement data register on shipment test without applying magnetic field on purpose.

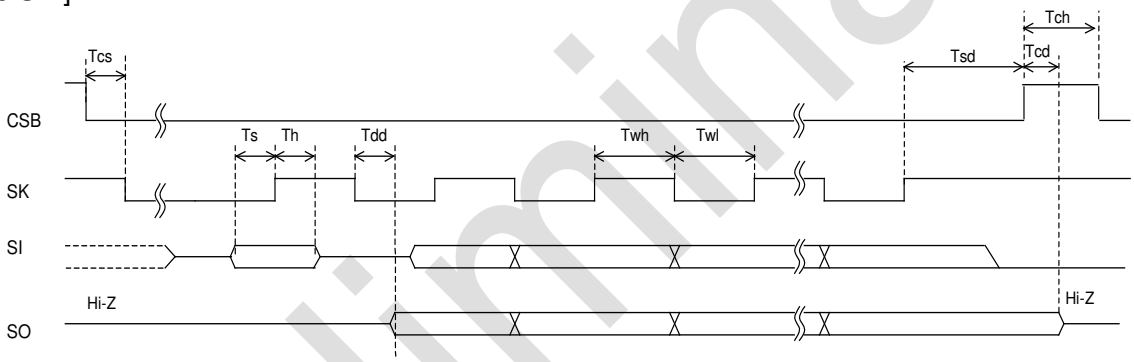
8.4. 4-wire SPI

4-wire SPI is compliant with mode 3 (SPI-mode3).

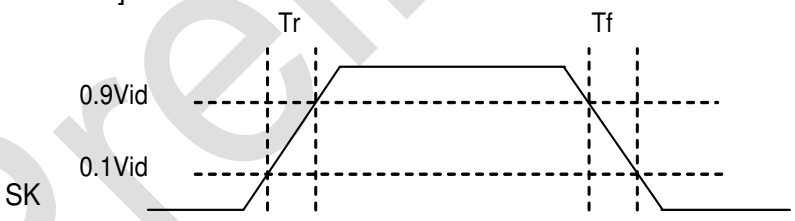
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSB setup time	Tcs		50			ns
Data setup time	Ts		50			ns
Data hold time	Th		50			ns
SK high time	Twh		150			ns
SK low time	Twl		150			ns
SK setup time	Tsd		50			ns
SK to SO delay time (* 9)	Tdd				50	ns
CSB to SO delay time (* 9)	Tcd				50	ns
SK rise time(* 10)	Tr				100	ns
SK fall time (* 10)	Tf				100	ns
CSB high time	Tch		150			ns

* 9. SO load capacitance: 20 pF
* 10. Reference value for design.

[4-wire SPI]



[Rise time and fall time]



8.5. I²C Bus Interface

CSB pin = "H".
I²C bus interface is compliant with Standard mode and Fast mode. Standard/Fast mode is selected automatically by fSCL.

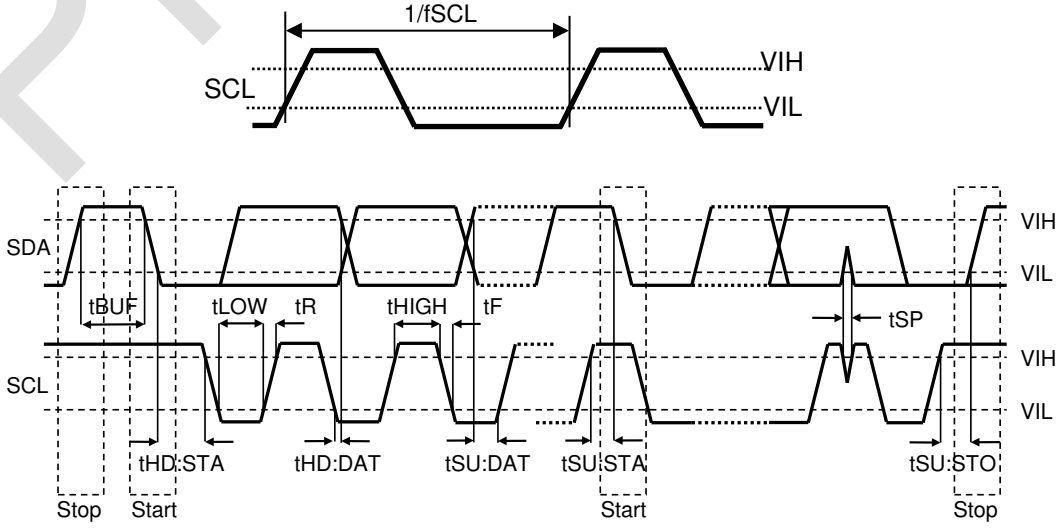
☐ Standard mode
fSCL ≤ 100 kHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL			100	kHz
SCL clock "High" time	tHIGH	4.0			µs
SCL clock "Low" time	tLOW	4.7			µs
SDA and SCL rise time	tR			1.0	µs
SDA and SCL fall time	tF			0.3	µs
Start Condition hold time	tHD:STA	4.0			µs
Start Condition setup time	tSU:STA	4.7			µs
SDA hold time (vs. SCL falling edge)	tHD:DAT	0			µs
SDA setup time (vs. SCL rising edge)	tSU:DAT	250			ns
Stop Condition setup time	tSU:STO	4.0			µs
Bus free time	tBUF	4.7			µs

☐ Fast mode
100 kHz ≤ fSCL ≤ 400 kHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL			400	kHz
SCL clock "High" time	tHIGH	0.6			µs
SCL clock "Low" time	tLOW	1.3			µs
SDA and SCL rise time	tR			0.3	µs
SDA and SCL fall time	tF			0.3	µs
Start Condition hold time	tHD:STA	0.6			µs
Start Condition setup time	tSU:STA	0.6			µs
SDA hold time (vs. SCL falling edge)	tHD:DAT	0			µs
SDA setup time (vs. SCL rising edge)	tSU:DAT	100			ns
Stop Condition setup time	tSU:STO	0.6			µs
Bus free time	tBUF	1.3			µs
Noise suppression pulse width	tSP			50	ns

[I²C bus interface timing]



9. Functional Descriptions

9.1. Power States

When VDD and VID are turned on from Vdd = OFF (0 V) and Vid = OFF (0 V), all registers in AK09940 are initialized by POR circuit and AK09940 transits to Power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

Table 9.1. Power States

State	VDD	VID	Power state
1	OFF (0 V)	OFF (0 V)	OFF (0 V). It does not affect external interface. Digital input pins other than SCL and SDA pin should be fixed to “L” (0 V).
2	OFF (0 V)	1.65 V to 1.98 V	OFF (0 V). It does not affect external interface.
3	1.7 V to 1.98 V	OFF (0 V)	OFF (0 V). It does not affect external interface. Digital input pins other than SCL and SDA pin should be fixed to “L” (0 V).
4	1.7 V to 1.98 V	1.65 V to Vdd	ON.

9.2. Reset Functions

When the power state is ON, always keep Vid ≤ Vdd.
Power-on reset (POR) works until Vdd reaches to the operation effective voltage (about 1.2 V: reference value for design) on power-on sequence. After POR is deactivated, all registers are initialized and transits to power down mode.

When Vdd = 1.7 to 1.98 V, POR circuit and VID monitor circuit are active. When Vid = 0 V, AK09940 is in reset status and it consumes the current of reset state (IDD5).

AK09940 has four types of reset;
(1) Power on reset (POR)
When Vdd rise is detected, POR circuit operates, and AK09940 is reset.
(2) VID monitor
When Vid is turned OFF (0V), AK09940 is reset.
(3) Reset pin (RSTN)
AK09940 is reset by Reset pin. When Reset pin is not used, connect to VID.
(4) Soft reset
AK09940 is reset by setting SRST bit.

After reset is completed, all registers and FIFO buffer are initialized and AK09940 transit to Power-down mode automatically.

9.3. Operation Modes

AK09940 has following nine operation modes:
(1) Power-down mode
(2) Single measurement mode
(3) Continuous measurement mode 1
(4) Continuous measurement mode 2
(5) Continuous measurement mode 3
(6) Continuous measurement mode 4
(7) Continuous measurement mode 5
(8) Continuous measurement mode 6: Only valid for low power drive 1 or 2
(9) Self-test mode

By setting CNTL3 register MODE[4:0] bits, the operation set for each mode is started. A transition from one mode to another is shown below.

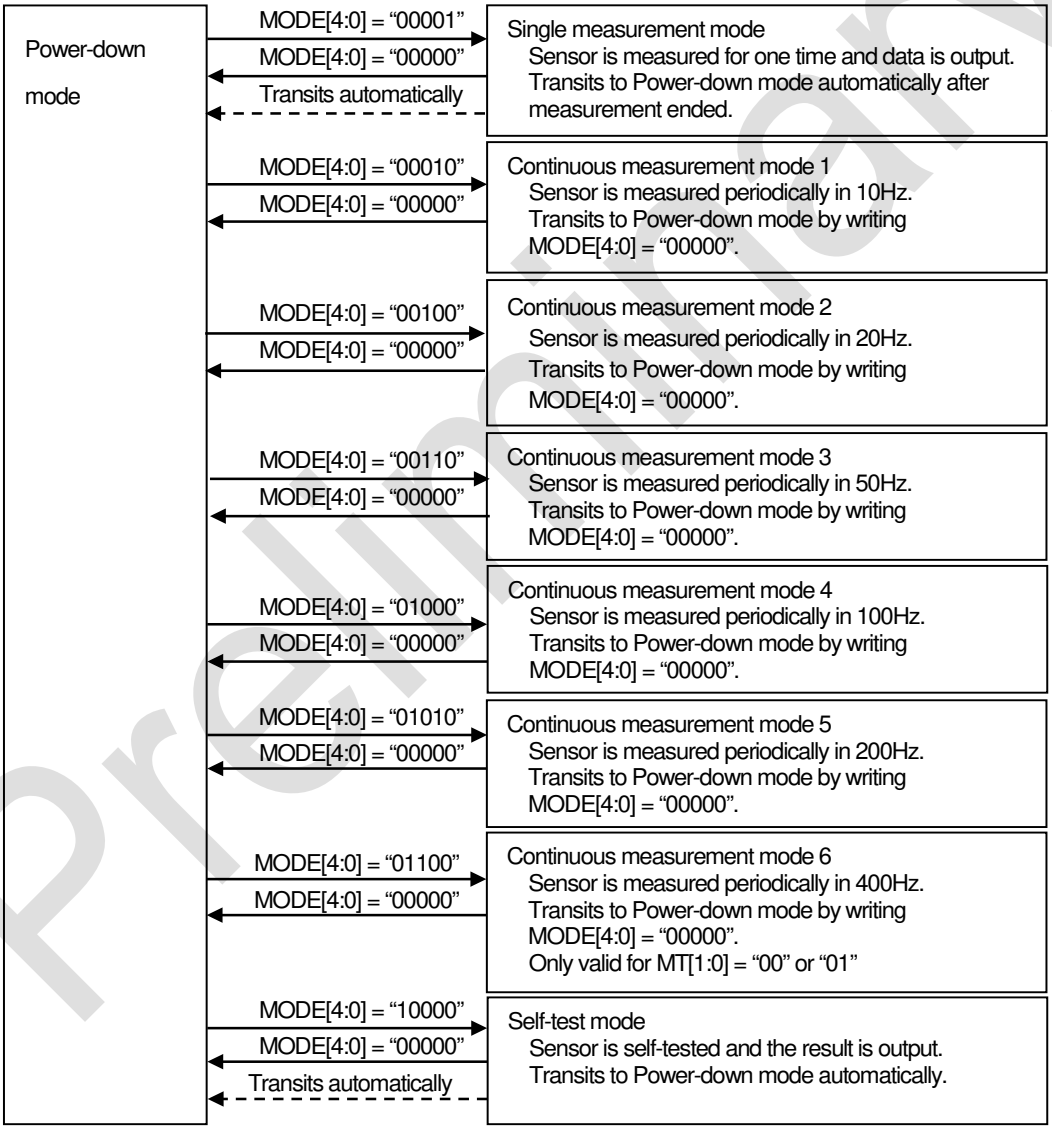


Figure 9.1. Operation mode

When power is turned ON, AK09940 is in Power-down mode. When a specified value is set to MODE[4:0] bits, AK09940 transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After Power-down mode is set, at least 100 μs (Twait) is needed before setting another mode.

9.4. Description of Each Operation Mode

9.4.1. Power-down Mode

Power to almost all internal circuits is turned off. All registers are accessible in Power-down mode. Data stored in read/write registers are remained. They can be reset by soft reset.

9.4.2. Single Measurement Mode

When Single measurement mode (MODE[4:0] = “00001”) is set, magnetic sensor measurement is started. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HXL to HZH), then AK09940 transits to Power-down mode automatically. On transition to Power-down mode, MODE[4:0] turns to “00000”. If temperature sensor is enabled (TEM = “1”), temperature sensor measurement is started together with magnetic sensor measurement and measurement temperature data is stored to measurement data registers (TMPS). At the same time, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When any of measurement data register (HXL to TMPS) or ST2 register is read, DRDY bit turns to “0”. It remains “1” on transition from Power-down mode to another mode. DRDY pin is in the same state as DRDY bit. (Figure 9.2.)
When sensor is measuring (Measurement period), measurement data registers (HXL to TMPS) keep the previous data. Therefore, it is possible to read out data even in measurement period. Data read out in measurement period are previous data. (Figure 9.3.)

When ST2 register is read, AK09940 judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

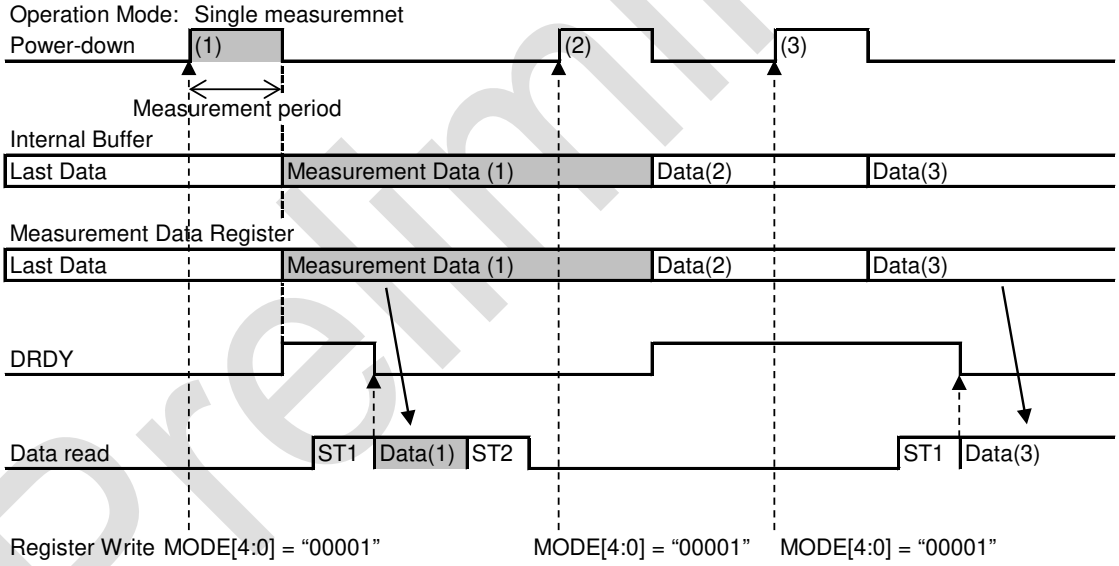


Figure 9.2. Single measurement mode when data is read out of measurement period

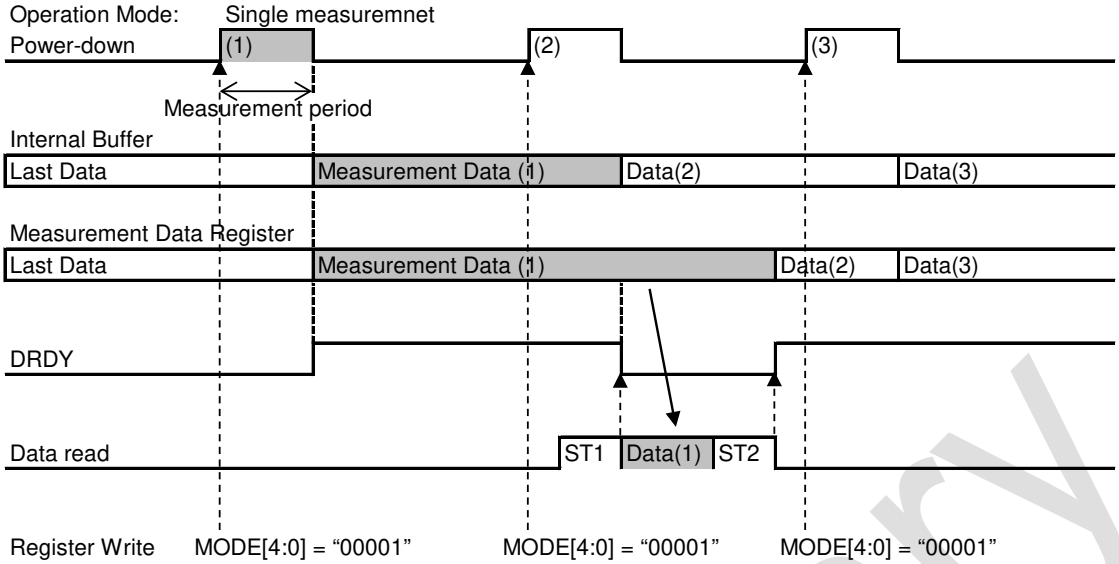


Figure 9.3. Single measurement mode when data read started during measurement period

9.4.3. Continuous Measurement Modes

When Continuous measurement mode 1 (MODE[4:0] = “00010”), 2 (MODE[4:0] = “00100”), 3 (MODE[4:0] = “00110”), 4 (MODE[4:0] = “01000”), 5 (MODE[4:0] = “01010”) or 6 (MODE[4:0] = “01100”) is set, magnetic sensor measurement is started periodically at 10 Hz, 20 Hz, 50 Hz, 100 Hz, 200 Hz or 400 Hz respectively. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HXL to HZH) and all circuits except for the minimum circuit required for counting cycle length are turned off (PD). When the next measurement timing comes, AK09940 wakes up automatically from PD and starts measurement again. If temperature sensor is enabled (TEM = “1”), temperature sensor measurement is started periodically at 5 Hz, and measurement temperature data is stored to measurement data registers (TMPS). For example, in the 10 Hz mode, measurement is performed once every 2 times. Continuous measurement mode ends when Power-down mode (MODE[4:0] = “00000”) is set. It repeats measurement until Power-down mode is set.

When Continuous measurement mode 1 (MODE[4:0] = “00010”), 2 (MODE[4:0] = “00100”), 3 (MODE[4:0] = “00110”), 4 (MODE[4:0] = “01000”), 5 (MODE[4:0] = “01010”) or 6 (MODE[4:0] = “01100”) is set again while AK09940 is already in Continuous measurement mode, a new measurement starts. ST1, ST2 and measurement data registers (HXL to TMPS) will not be initialized by this.

Table 9.2. Continuous measurement modes

Operation mode	Register setting (MODE[4:0] bits)	Measurement frequency [Hz]
Continuous measurement mode 1	00010	10
Continuous measurement mode 2	00100	20
Continuous measurement mode 3	00110	50
Continuous measurement mode 4	01000	100
Continuous measurement mode 5	01010	200
Continuous measurement mode 6	01100	400

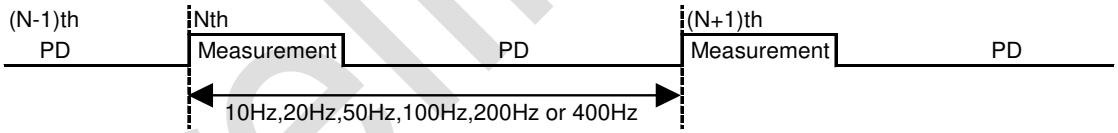


Figure 9.4. Continuous measurement mode

9.4.3.1. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. DRDY pin is in the same state as DRDY bit. When measurement is performed correctly, AK09940 becomes Data Ready on transition to PD after measurement.

9.4.3.2. Normal Read Sequence

(1) Check Data Ready or not by monitoring DRDY pin
When Data Ready, proceed to the next step.
(2) Read ST1 register
DRDY: Shows Data Ready or not. Not when "0", Data Ready when "1".
(3) Read measurement data
When any of measurement data register (HXL to TMPS) or ST2 register is read, AK09940 judges that data reading is started. When data reading is started, DRDY bit turns to "0".
(4) Read ST2 register (required)
DOR: Shows if any data has been skipped before the current data or not. There are no skipped data when "0", there are skipped data when "1". After reading ST2 register, DOR bit turns to "0".

When ST2 register is read, AK09940 judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

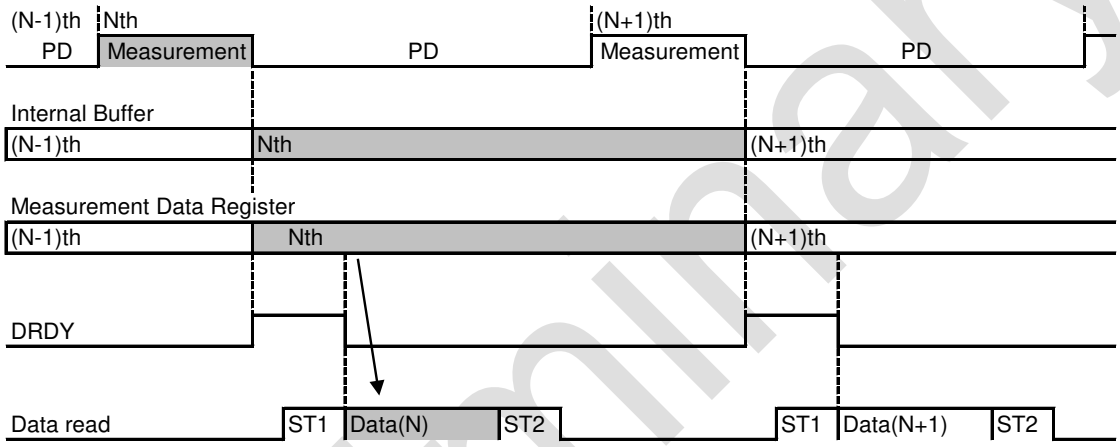


Figure 9.5. Normal read sequence

9.4.3.3. Data Read Start during Measurement

When sensor is measuring (Measurement period), measurement data registers (HXL to TMPS) keep the previous data. Therefore, it is possible to read out data even in measurement period. If data is started to be read during measurement period, previous data is read.

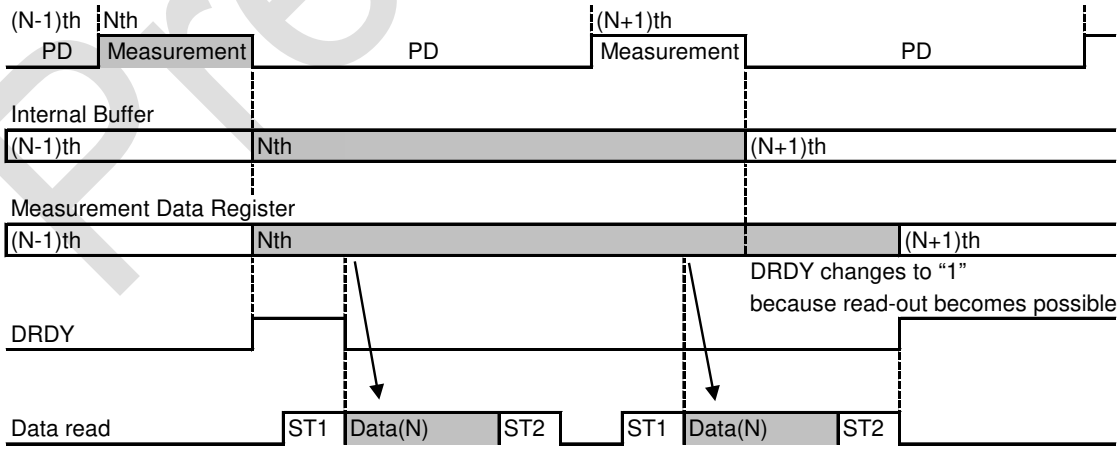


Figure 9.6. Data read start during measuring

9.4.3.4. Data Skip

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turns to “1”.
When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is skipped and not stored so that DOR bit turns to “1”.
In both case, DOR bit turns to “0” at the next start of data reading.

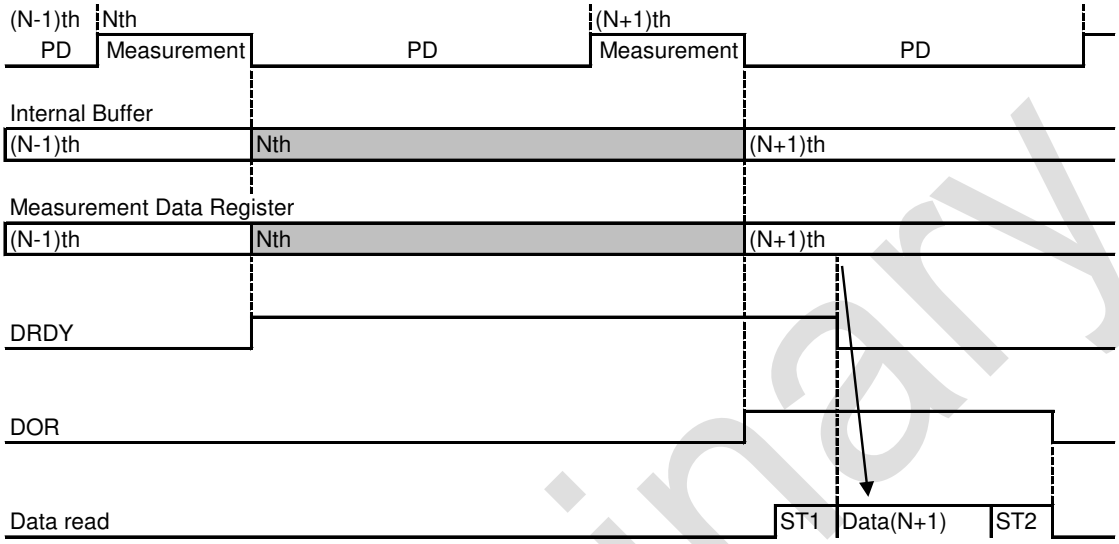


Figure 9.7. Data Skip: when data is not read

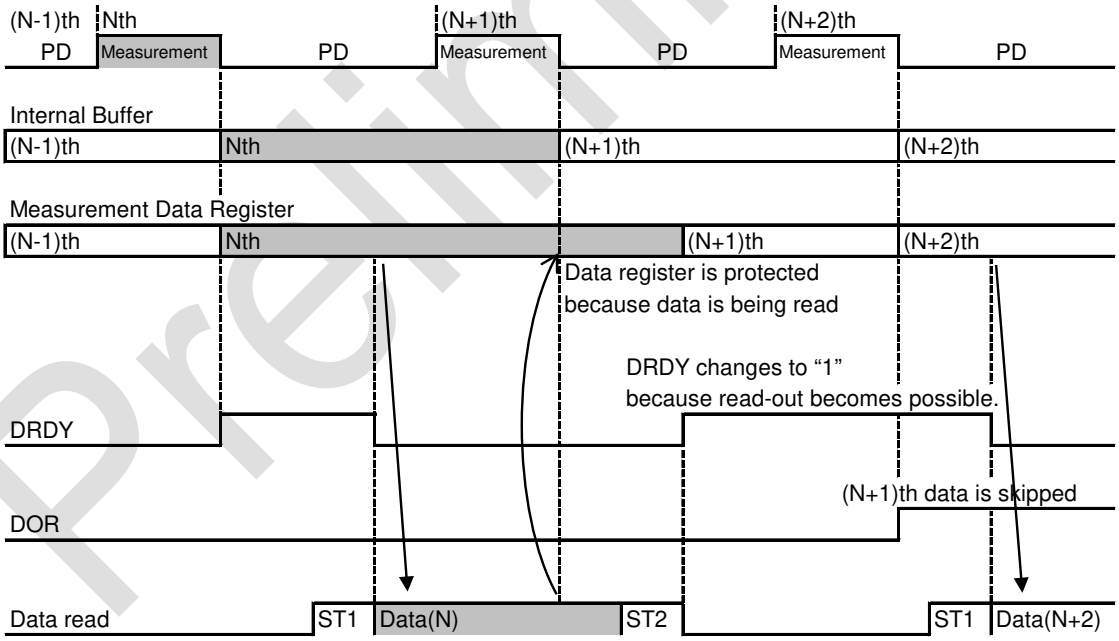


Figure 9.8. Data Skip: when data read has not been finished before the next measurement end

Although Nth data is read out when it is performed during (N+1)th measurement period, (N+1)th data is obtained by reading out again before completion of (N+2)th measurement.

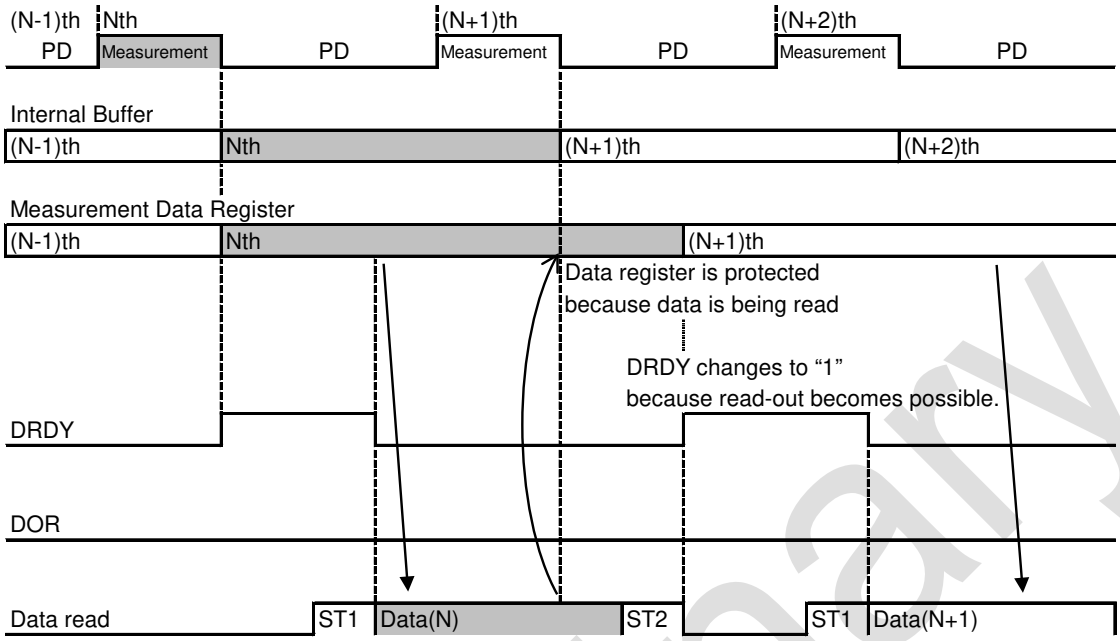


Figure 9.9. Read-out is performed before completion of the next measurement after data protection.

9.4.3.5. End Operation

Set Power-down mode (MODE[4:0] = "00000") to end Continuous measurement mode.

9.4.3.6. Magnetic Sensor Overflow

When magnetic sensor overflow occurs, measurement data register (HXL to HZH) is clipped to 1FFFFh.

9.4.4. Self-test Mode

Self-test mode is used to check if the magnetic sensor is working normally.
When Self-test mode (MODE[4:0] = “10000”) is set, magnetic field is generated by the internal magnetic source and magnetic sensor is measured. Measurement data is stored to measurement data registers (HXL to HZH), then AK09940 transits to Power-down mode automatically. (Temperature sensor is measured.)
Data read sequence and functions of read-only registers in Self-test mode is the same as Single measurement mode.

9.4.4.1. Self-test Sequence

(1) Set Power-down mode. (MODE[4:0] = “00000”)
(2) Set Low noise drive 2. (MT[1:0] = “11”)
(3) Set Self-test mode. (MODE[4:0] = “10000”)
(4) Check Data Ready or not by monitoring DRDY pin
When Data Ready, proceed to the next step.
(5) Read measurement data (HXL to HZH)
(6) Read ST2 register (required)

When ST2 register is read, AK09940 judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

9.4.4.2. Self-test Judgment

When measurement data read by the above sequence is in the range of following table, AK09940 is working normally.

	HX[17:0]	HY[17:0]	HZ[17:0]
Criteria	(TBD) ≤ HX ≤ (TBD)	(TBD) ≤ HY ≤ (TBD)	(TBD) ≤ HZ ≤ (TBD)

9.5. Temperature Sensor

In Single measurement mode, Continuous measurement mode 1, 2, 3, 4, 5 or 6 is set, AK09940 can measure temperature sensor together with magnetic sensor. When temperature sensor is enabled (TEM = “1”), temperature sensor measurement is started together with magnetic sensor measurement. In Continuous measurement mode 1, 2, 3, 4, 5 or 6, temperature sensor measurement is started periodically at 5 Hz. In Single measurement mode, temperature sensor measurement is stared at every measurement of magnetic sensor measurement. If user wants to change temperature sensor measurement enables or disables, please set to Power-down mode before change temperature sensor measurement.
Default TEM register is “enable” (TEM = “1”).

9.6. Sensor Drive Select

AK09940 can choose “Low power” or “Low noise” drive.
“Low power” is used to save the current consumption and “Low noise” is used to reduce the noise of the AK09940.

MT[1:0] bits can be changed in Power-down mode only. Default MT[1:0] bits is Low power drive 1 (MT[1:0] bits = “00”).

9.7. FIFO

FIFO function is available in Continuous measurement modes. FIFO function is enabled by setting FIFO bit = “1”. It is prohibited to enable FIFO function in any modes other than Continuous measurement modes.

When FIFO function is enabled, data register (HXL to TMPS) is stored to the buffer as a set of data. The buffer is capable up to 8 sets of data. If a new data is measured when 8 sets of data is already stored, the oldest data set is deleted and the new data set is stored. If data register is read when FIFO function is enabled, the oldest data set is read as first-in first-out method.

When reading out data from the buffer, always start with HXL register and finish with ST2 register. By accessing HXL register, the oldest data set is passed to the read register from the buffer. Reading ST2 register is regarded as the finish of reading out one set of data. Then the read data set is deleted and the next oldest data set will be ready to be read. If ST2 register is not read, the same set of data is kept in the read register.

When FIFO function is enabled, DRDY bit and DOR bit functions differently. DRDY bit informs that data set is stored up to Watermark. Refer to 9.7.1. for details. DOR bit informs that data set is overflowed from the buffer. If a set of new data is measured when the buffer is full, DOR bit turns to “1”. If at least one data set is read from the buffer, DOR bit turns to “0”.

If data is read out when there is no data in the buffer, INV bit is turned to “1”, data register (HXL to HZH) is clipped to 1FFFFh and data register (TMPS) is clipped to 7Fh. If a set of new data is measured, INV bit turns to “0”.

When AK09940 is reset (refer to 9.2.), FIFO buffer are initialized.

9.7.1. Watermark

When FIFO function is enabled, Watermark function is available. By setting WM[2:0] bits, AK09940 informs that data set is stored up to or more than Watermark. If the number of stored data set is equal to or more than the number set to WM[2:0] bits, DRDY bit turns to “1”. If the number of stored data set is less than the number set to WM[2:0] bits, DRDY bit turns to “0”. DRDY pin is the same state as DRDY bit.
WM[2:0] should be changed in the Power-down mode only. It is prohibited to write WM[2:0] in other modes.

9.7.2. FIFO status

When FIFO function is enabled, AK09940 can be use FNUM register for monitor of FIFO.

10. Serial Interface

AK09940 supports I²C bus interface and 4-wire SPI. A selection is made by CSB pin. When used as 3-wire SPI, set SI pin and SO pin wired-OR externally.

CSB pin = "L": 4-wire SPI
CSB pin = "H": I²C bus interface

10.1. 4-wire SPI

The 4-wire SPI consists of four digital signal lines: SK, SI, SO, and CSB, and is provided in 16bit protocol. Data consists of Read/Write control bit (R/W), register address (7-bit) and control data (8-bit). To read out all axes measurement data (X, Y, Z), an option to read out more than one byte data using automatic increment command is available. (Sequential read operation)

CSB pin is low active. Input data is taken in on the rising edge of SK pin, and output data is changed on the falling edge of SK pin. (SPI-mode3)
Communication starts when CSB pin transits to "L" and stops when CSB pin transits to "H". SK pin must be "H" during CSB pin is in transition. Also, it is prohibited to change SI pin during CSB pin is "H" and SK pin is "H".

10.1.1. Writing Data

Input 16 bits data on SI pin in synchronous with the 16-bit serial clock input on SK pin. Out of 16 bits input data, the first 8-bit specify the R/W control bit (R/W = "0" when writing) and register address (7-bit), and the latter 8-bit are control data (8-bit). When any of addresses listed on Table 11.1. is input, AK09940 recognizes that it is selected and takes in latter 8-bit as setting data.
If the number of clock pulses is less than 16, no data is written. If the number of clock pulses is more than 16, data after the 16th clock pulse on SI pin are ignored.
It is not compliant with serial write operation for multiple addresses.

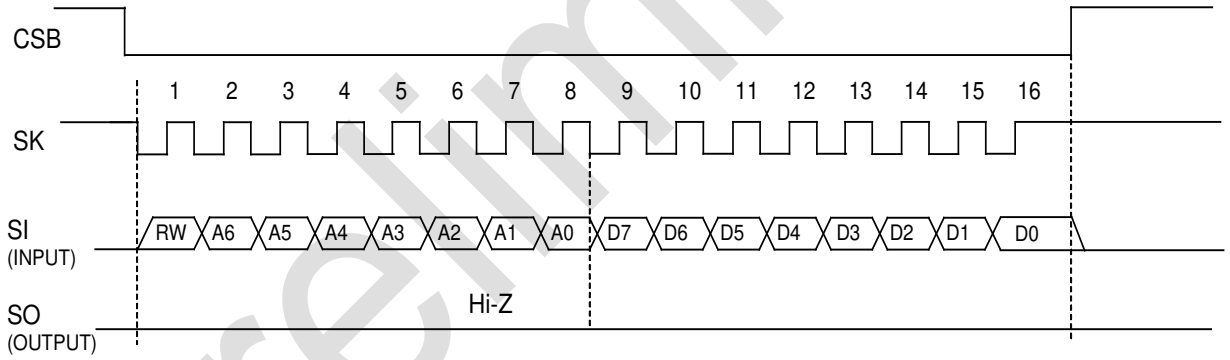


Figure 10.1. 4-wire SPI Writing Data

10.1.2. Reading Data

Input the R/W control bit (R/W = "1") and 7-bit register address on SI pin in synchronous with the first 8-bit of the 16 bits of a serial clock input on SK pin. Then AK09940 outputs the data held in the specified register with MSB first from SO pin.
When clocks are input continuously after one byte of data is read, the address is incremented and data in the next address is output. Accordingly, after the falling edge of the 16th clock and CSB pin is "L", the data in the next address is output on SO pin. When CSB pin is driven "L" to "H", SO pin is placed in the high-impedance state.
AK09940 has two incrementation lines; 00h to 1Bh and 30h to 33h. In line 00h to 1Bh, the incrementation depends on FIFO bit. When FIFO function is disabled, AK09940 increment as follows: 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh → 00h → 01h … When FIFO function is enabled: 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh → 11h → 12h ... In line 30h to 33h, it increments as: 30h → 31h → 32h → 33h → 30h …
37h is reserved address. Do not access to this address.
When specified address is other than 00h to 1Bh or 30h to 33h or 36h to 37h, AK09940 recognizes that it is not selected and keeps SO pin in high-impedance state. Therefore, user can use other addresses for other devices.

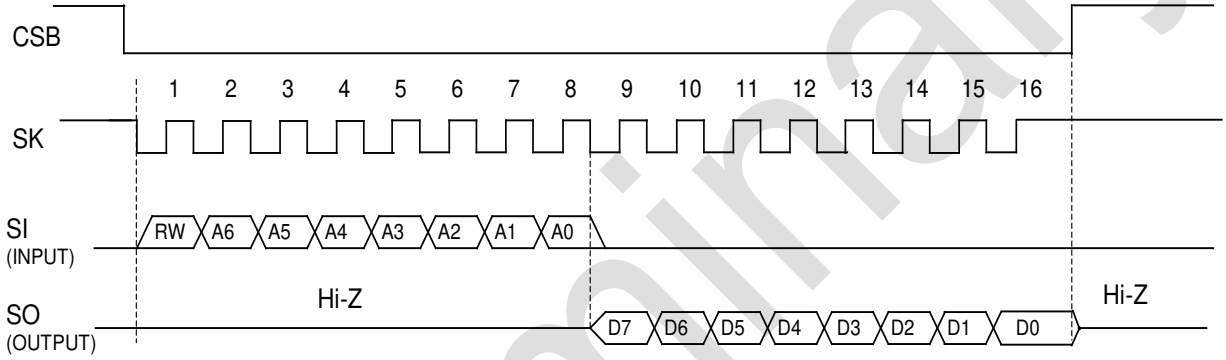


Figure 10.2. 4-wire SPI Reading Data

10.2. I²C Bus Interface

The I²C bus interface of AK09940 supports the Standard mode (100 kHz max.) and the Fast mode (400 kHz max.).

10.2.1. Data Transfer

To access AK09940 on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, AK09940 compares the slave address with its own address. If these addresses match, AK09940 generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

10.2.1.1. Change of Data

A change of data on the SDA line must be made during “Low” period of the clock on the SCL line. When the clock signal on the SCL line is “High”, the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is “Low”.)
During the SCL line is “High”, the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

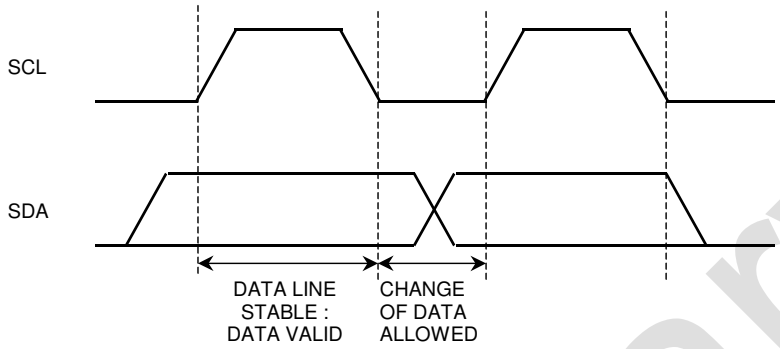


Figure 10.3. Data Change

10.2.1.2. Start/Stop Condition

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a start condition is generated. Every instruction starts with a start condition.
If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a stop condition is generated. Every instruction stops with a stop condition.

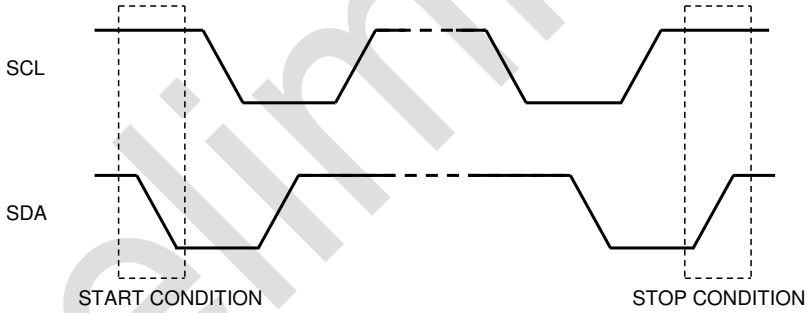


Figure 10.4. Start and Stop Condition

10.2.1.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data. The IC that receives the data drives the SDA line to “Low” on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked.
AK09940 generates an acknowledge after reception of a start condition and slave address.
When a WRITE instruction is executed, AK09940 generates an acknowledge after every byte is received.
When a READ instruction is executed, AK09940 generates an acknowledge then transfers the data stored at the specified address. Next, AK09940 releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK09940 transmits the 8-bit data stored at the next address. If no acknowledge is generated, AK09940 stops data transmission.

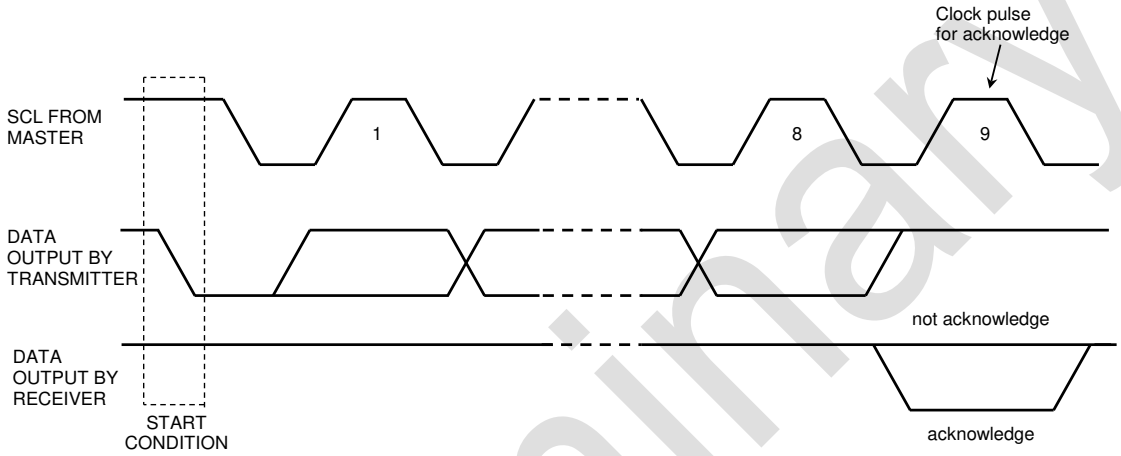


Figure 10.5. Generation of Acknowledge

10.2.1.4. Slave Address

The slave address of AK09940 can be selected from the following list by setting CAD0/1 pin. When CAD pin is fixed to VSS, the corresponding slave address bit is “0”. When CAD pin is fixed to VID, the corresponding slave address bit is “1”.

Table 10.1. Slave Address and CAD0/1 pin

CAD1	CAD0	Slave Address
0	0	0CH
0	1	0DH
1	0	0EH
1	1	0FH

MSB LSB

0	**0**	**0**	**1**	**1**	**CAD1**	**CAD0**	**R/W**

Figure 10.6. Slave Address

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.
When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to “1”, READ instruction is executed. When the R/W bit is set to “0”, WRITE instruction is executed.

10.2.2. WRITE Instruction

When the R/W bit is set to “0”, AK09940 performs write operation.
In write operation, AK09940 generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

MSB							LSB
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**

Figure 10.7. Register Address

After receiving the second byte (register address), AK09940 generates an acknowledge then receives the third byte.
The third and the following bytes represent control data. Control data consists of 8-bit and is based on the MSB-first configuration. AK09940 generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Figure 10.8. Control Data

AK09940 can write multiple bytes of data at a time.
After reception of the third byte (control data), AK09940 generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.
The address is incremented from 00h to 1Bh or from 30h to33h. When the address is between 00h and 1Bh, in case that FIFO function is disabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh, and the address goes back to 00h after 1Bh. In case that FIFO function is enabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh, and the address goes back to 11h after 1Bh. When the address is between 30h and 33h, the address goes back to 30h after 33h.
Actual data is written only to Read/Write registers. (Table 11.2.)

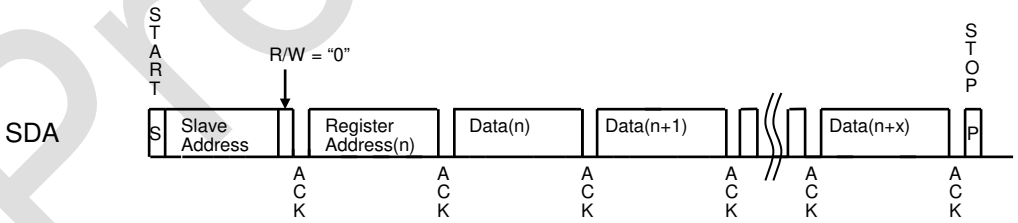


Figure 10.9. WRITE Instruction

10.2.3. READ Instruction

When the R/W bit is set to “1”, AK09940 performs read operation.
If a master IC generates an acknowledge instead of a stop condition after AK09940 transfers the data at a specified address, the data at the next address can be read.
Address can be 00h to 1Bh or 30h to 33h. When the address is between 00h and 1Bh, in case that FIFO function is disabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh, and the address goes back to 00h after 1Bh. In case that FIFO function is enabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh, and the address goes back to 11h after 1Bh. When the address is between 30h and 33h, the address goes back to 30h after 33h.
AK09940 supports one byte read and multiple byte read.

10.2.3.1. One Byte Read

AK09940 has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.
The internal address counter holds the next address of the most recently accessed address.
For example, if the address most recently accessed (for READ instruction) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read.
In one byte read operation, AK09940 generates an acknowledge after receiving a slave address for the READ instruction (R/W bit = “1”). Next, AK09940 transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK09940 transmits one byte of data, the read operation stops.

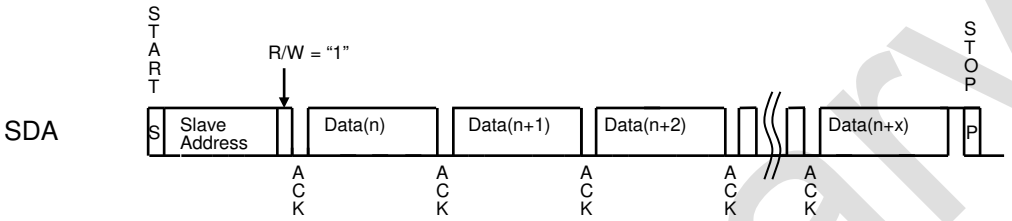


Figure 10.10. One Byte READ

10.2.3.2. Multiple Byte Read

By multiple byte read operation, data at an arbitrary address can be read.
The multiple byte read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit = “1”) is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.
After AK09940 generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit = “1”) are generated again. AK09940 generates an acknowledge in response to this slave address transmission. Next, AK09940 transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

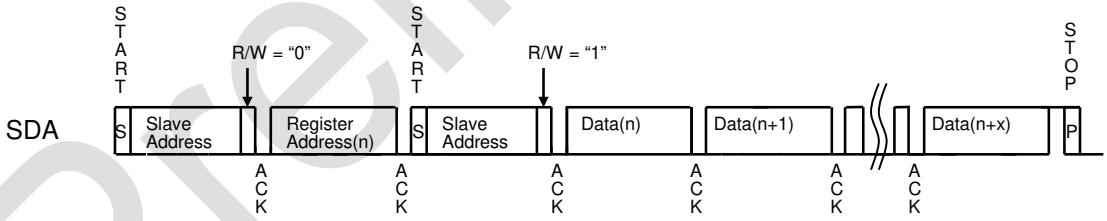


Figure 10.11. Multiple Byte READ

11. Registers

11.1. Description of Registers

AK09940 has registers of 22 addresses as indicated in Table 11.1.. Every address consists of 8-bit data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 11.1. Register Table

Name	Address	READ/ WRITE	Description	Bit width	Remarks
WIA1	00h	READ	Company ID	8	
WIA2	01h	READ	Device ID	8	
RSV1	02h	READ	Reserved 1	8	
RSV2	03h	READ	Reserved 2	8	
ST1	10h	READ	Status 1	8	Data status
HXL	11h	READ	Measurement Magnetic Data	8	X-axis data
HXM	12h	READ		8	
HXH	13h	READ		8	
HYL	14h	READ		8	Y-axis data
HYM	15h	READ		8	
HYH	16h	READ		8	
HZL	17h	READ		8	Z-axis data
HZM	18h	READ		8	
HZH	19h	READ		8	
TMPS	1Ah	READ	Measurement Temperature Data	8	Temperature data
ST2	1Bh	READ	Status 2	8	Data status
CNTL1	30h	READ/ WRITE	Control 1	8	Control settings
CNTL2	31h	READ/ WRITE	Control 2	8	Control settings
CNTL3	32h	READ/ WRITE	Control 3	8	Control settings
CNTL4	33h	READ/ WRITE	Control 4	8	Control settings
I2CDIS	36h	READ/ WRITE	I^2C disable	8	
TS	37h	READ/ WRITE	Test	8	DO NOT ACCESS

Addresses 00h to 1Bh and 30h to 33h are compliant with automatic increment function of serial interface respectively. When the address is in 00h to 1Bh, in case that FIFO function is disabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh, and the address goes back to 00h after 1Bh. In case that FIFO function is enabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 1Bh, and the address goes back to 11h after 1Bh. When the address is in 30h to 33h, the address goes back to 30h after 33h.

11.2. Register Map

Table 11.2. Register Map

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	1	0	1	0	0	0	0	1
02h	RSV1	RSV17	RSV16	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10
03h	RSV2	RSV27	RSV26	RSV25	RSV24	RSV23	RSV22	RSV21	RSV20
10h	ST1	0	0	0	FNUM3	FNUM2	FNUM1	FNUM0	DRDY
11h	HXL	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
12h	HXM	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
13h	HXH	HX17	HX17	HX17	HX17	HX17	HX17	HX17	HX16
14h	HYL	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
15h	HYM	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
16h	HYH	HY17	HY17	HY17	HY17	HY17	HY17	HY17	HY16
17h	HZL	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
18h	HZM	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
19h	HZH	HZ17	HZ17	HZ17	HZ17	HZ17	HZ17	HZ17	HZ16
1Ah	TMPS	TMPS7	TMPS6	TMPS5	TMPS4	TMPS3	TMPS2	TMPS1	TMPS0
1Bh	ST2	0	0	0	0	0	0	INV	DOR
Read/Write register									
30h	CNTL1	0	0	0	0	0	WM2	WM1	WM0
31h	CNTL2	0	TEM	0	0	0	0	0	0
32h	CNTL3	FIFO	MT1	MT0	MODE4	MODE3	MODE2	MODE1	MODE0
33h	CNTL4	0	0	0	0	0	0	0	SRST
36h	I2CDIS	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
37h	TS	-	-	-	-	-	-	-	-

When VDD is turned ON, POR function works and all registers of AK09940 are initialized regardless of VID status. To write data to or to read data from register, VID must be ON.
TS is test register for shipment test. Do not access this register.

11.3. Detailed Description of Registers

11.3.1. WIA: Who I Am

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	1	0	1	0	0	0	0	1

WIA1[7:0] bits: Company ID of AKM. It is described in one byte and fixed value.
48h: fixed
WIA2[7:0] bits: Device ID of AK09940. It is described in one byte and fixed value.
A1h: fixed

11.3.2. RSV: Reserved

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
02h	RSV1	RSV17	RSV16	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10
03h	RSV2	RSV27	RSV26	RSV25	RSV24	RSV23	RSV22	RSV21	RSV20

RSV1[7:0] bits/ RSV2[7:0] bits: Reserved register used internal of AKM.

11.3.3. ST1: Status 1

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
10h	ST1	0	0	0	FNUM3	FNUM2	FNUM1	FNUM0	DRDY
Reset		0	0	0	0	0	0	0	0

FNUM[3:0] bits: FIFO status
"0000": 0 set
"0001": 1 set
"0010": 2 sets
|
"1000": 8 sets

FNUM bits correspond to how many data sets are currently in the FIFO buffer.

DRDY: Data Ready
"0": Normal
"1": Data is ready

When FIFO is disabled (FIFO bit = "0");
DRDY bit turns to "1" when data is ready in Single measurement mode, Continuous measurement mode 1, 2, 3, 4, 5, 6 or Self-test mode. It returns to "0" when any one of ST2 register or measurement data register (HXL to TMPS) is read.

When FIFO is enabled (FIFO bit = "1");
If the number of stored data set is equal to or more than the number set to WM[2:0] bits, DRDY bit turns to "1". If the number of stored data set is less than the number set to WM[2:0] bits, DRDY bit turns to "0".

11.3.4. HXL to HZH: Measurement data

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
11h	HXL	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
12h	HXM	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
13h	HXH	HX17	HX17	HX17	HX17	HX17	HX17	HX17	HX16
14h	HYL	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
15h	HYM	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
16h	HYH	HY17	HY17	HY17	HY17	HY17	HY17	HY17	HY16
17h	HZL	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
18h	HZM	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
19h	HZH	HZ17	HZ17	HZ17	HZ17	HZ17	HZ17	HZ17	HZ16
Reset		0	0	0	0	0	0	0	0

Measurement data of magnetic sensor X-axis/Y-axis/Z-axis
HXL[7:0]: X-axis measurement data lower 8-bit
HXM[15:8]: X-axis measurement data middle 8-bit
HXH[17:16]: X-axis measurement data higher 2-bit
HYL[7:0]: Y-axis measurement data lower 8-bit
HYM[15:8]: Y-axis measurement data middle 8-bit
HYH[17:16]: Y-axis measurement data higher 2-bit
HZL[7:0]: Z-axis measurement data lower 8-bit
HZM[15:8]: Z-axis measurement data middle 8-bit
HZH[17:16]: Z-axis measurement data higher 2-bit

Measurement data is stored in two's complement and Little Endian format. Measurement range of each axis is -131072 to 131070 in 18-bit output.

Table 11.3. Measurement magnetic data format

Measurement data (each axis) [17:0]			Magnetic flux density [nT]
Two's complement	Hex	Decimal	
01 1111 1111 1111 1111	1FFFF	131071	overflow
01 1111 1111 1111 1110	1FFFE	131070	Magnetic sensor sensitivity (BSE) × Measurement data (Decimal)
|	|	|	
00 0000 0000 0000 0001	00001	1	
00 0000 0000 0000 0000	00000	0	
11 1111 1111 1111 1111	3FFFF	-1	
|	|	|	
10 0000 0000 0000 0000	20000	-131072	

When FIFO is enabled (FIFO bit = "1");
By accessing HXL register, the oldest data set is passed to the read register from the buffer. Reading ST2 register is regarded as the finish of reading out one set of data. Then the read data set is deleted and the next oldest data set will be ready to be read. If ST2 register is not read, the same set of data is kept in the read register. When reading out data, always start with HXL register and finish with ST2 register.

11.3.5. TMPS: Temperature Data

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
1Ah	TMPS	TMPS7	TMPS6	TMPS5	TMPS4	TMPS3	TMPS2	TMPS1	TMPS0
Reset		0	0	0	0	0	0	0	0

TMPS[7:0] bits: Measurement data of temperature sensor

Temperature [˚C] = 30 – (TMPS) / 1.72

Measurement data is stored in two's complement and Little Endian format.
Measurement range of temperature is -43.8˚C (maximum code) to +104.4˚C (minimum code). The data is clipped to 7Fh when temperature is -43.8˚C or less, and to 80h when +104.4˚C or higher.

Table 11.4. Measurement temperature data format

TMPS[7:0]	Temperature [˚C]
7Fh	-43.8
⋮	⋮
01h	29.4
00h	30.0
FFh	30.6
⋮	⋮
80h	104.4

11.3.6. ST2: Status 2

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
1Bh	ST2	0	0	0	0	0	0	INV	DOR
Reset		0	0	0	0	0	0	0	0

INV: Invalid data
"0": Normal
"1": Data is invalid

INV bit functions only when FIFO is enabled (FIFO bit = "1"). If data is read out when there is no data set in the buffer, INV bit is turned to "1", data register (HXL to HZH) is clipped to 1FFFFh and data register (TMPS) is clipped to 7Fh. If a set of new data is measured, INV bit turns to "0".

DOR: Data Overrun
"0": Normal
"1": Data overrun

When FIFO is disabled (FIFO bit = "0");
DOR bit turns to "1" when data has been skipped in Continuous measurement mode 1, 2, 3, 4, 5 or 6. It returns to "0" when ST2 register is read.

When FIFO is enabled (FIFO bit = "1");
If a set of new data is measured when the buffer is full, DOR bit turns to "1". If at least one data set is read from the buffer, DOR bit turns to "0".

When FIFO is disabled (FIFO bit = "0");
ST2 register has a role as data reading end register, also. When any of measurement data register (HXL to TMPS) is read in Continuous measurement mode 1, 2, 3, 4, 5 or 6, it means data reading start and taken as data reading until ST2 register is read. Therefore, when any of measurement data is read, be sure to read ST2 register at the end.

When FIFO is enabled (FIFO bit = "1");
ST2 register is a part of one set of data stored in the buffer. If any of data register (HXL to TMPS) is read, be sure to read ST2 register at the end. If there is no data set in the buffer, INV bit is "1".

11.3.7. CNTL1: Control 1

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
30h	CNTL1	0	0	0	0	0	WM2	WM1	WM0
Reset		0	0	0	0	0	0	0	0

WM[2:0] bits: Watermark level setting
"000": 1 step
"001": 2 steps
"010": 3 steps
|
"111": 8 steps (upper limit)

Watermark level can be set every 1 step. The upper limit of watermark level is 8 steps (WM[2:0] bits = "111").
It is prohibited to change WM[2:0] bits in any other modes than Power-down mode.

11.3.8. CNTL2: Control 2

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
31h	CNTL2	0	TEM	0	0	0	0	0	0
Reset		0	1	0	0	0	0	0	0

TEM: Temperature measurement setting
"0": disable (Not recommended)
"1": enable

When TEM bit is "1", temperature sensor measurement is enabled. Temperature sensor is measured together with magnetic sensor. Refer to 9.5. for detailed information.

11.3.9. CNTL3: Control 3

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
32h	CNTL3	FIFO	MT1	MT0	MODE4	MODE3	MODE2	MODE1	MODE0
Reset		0	0	0	0	0	0	0	0

MODE[4:0] bits: Operation mode setting
"00000": Power-down mode
"00001": Single measurement mode
"00010": Continuous measurement mode 1
"00100": Continuous measurement mode 2
"00110": Continuous measurement mode 3
"01000": Continuous measurement mode 4
"01010": Continuous measurement mode 5
"01100": Continuous measurement mode 6: Only valid for low power drive 1 or 2
"10000": Self-test mode
Other code settings are prohibited.

When each mode is set, AK09940 transits to the set mode. Refer to 9.3. for detailed information. If other value is set, AK09940 transits to power-down mode automatically.

FIFO: FIFO setting
"0": disable
"1": enable

By writing "1" to FIFO bit, FIFO function is enabled. By writing "0", FIFO function is disabled and the buffer is cleared at the same time. FIFO function is available only in Continuous measurement mode. It is prohibited to enable it other than Continuous measurement mode.

MT[1:0] bits: Sensor drive setting
"00": Low power drive 1
"01": Low power drive 2
"10": Low noise drive 1
"11": Low noise drive 2

When each drive is set, AK09940 transits to the set drive.

11.3.10. CNTL4: Control 4

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
33h	CNTL4	0	0	0	0	0	0	0	SRST
Reset		0	0	0	0	0	0	0	0

SRST: Soft reset
"0": Normal
"1": Reset

When "1" is set, all registers are initialized. After reset, SRST bit turns to "0" automatically.

11.3.11. I2CDIS: I²C Disable

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
36h	I2CDIS	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
Reset		0	0	0	0	0	0	0	0

This register disables I²C bus interface. I²C bus interface is enabled in default. To disable I²C bus interface, write "00011011" to I2CDIS register. Then I²C bus interface is disabled.
Once I²C bus interface is disabled, it is impossible to write other value to I2CDIS register. To enable I²C bus interface, reset AK09940 or input start condition 8 times continuously.

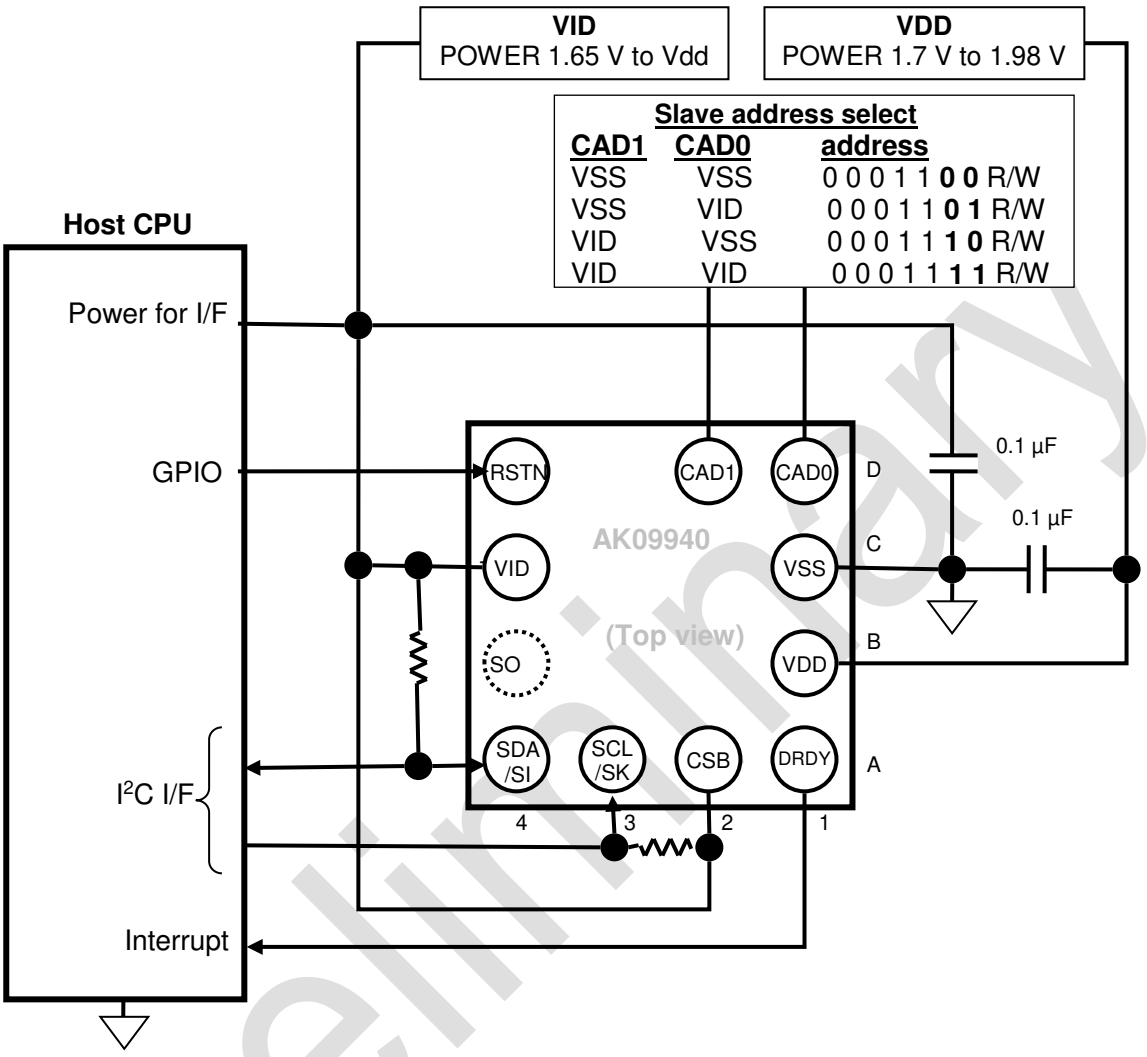
11.3.12. TS: Test

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
37h	TS	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

TS register is test register for shipment test. Do not access this register.

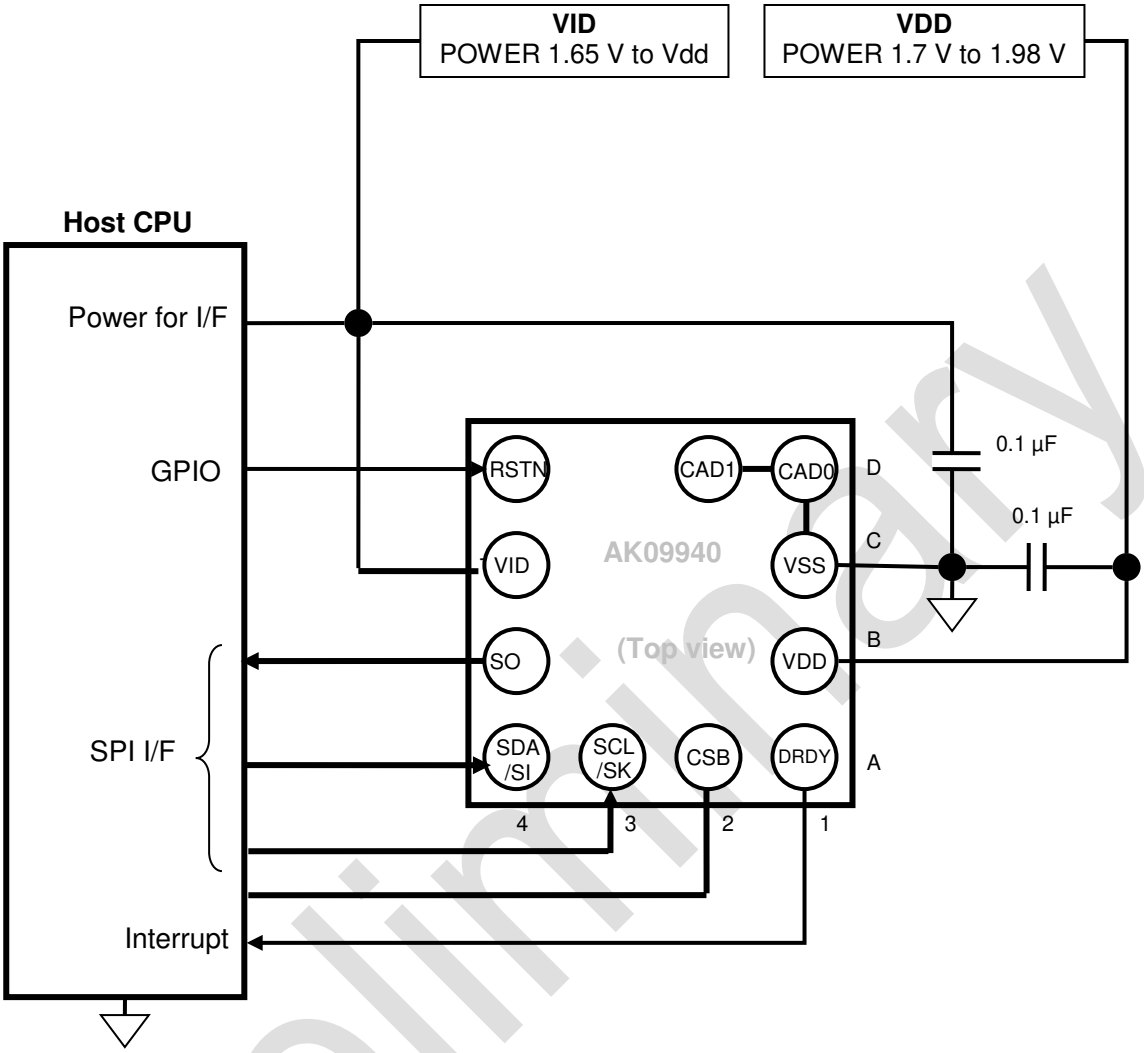
12. Recommended External Circuits

12.1. I²C Bus Interface



Pins of dot circle should be kept non-connected.

12.2. 4-wire SPI

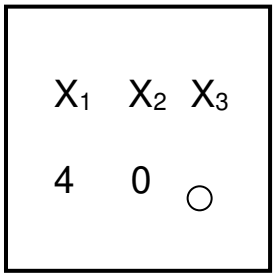


13. Package

13.1. Marking

Product name: 40
Date code: $X_1X_2X_3$

- X1 = Year code
- X2 = Month code
- X3 = Lot



<Top view>

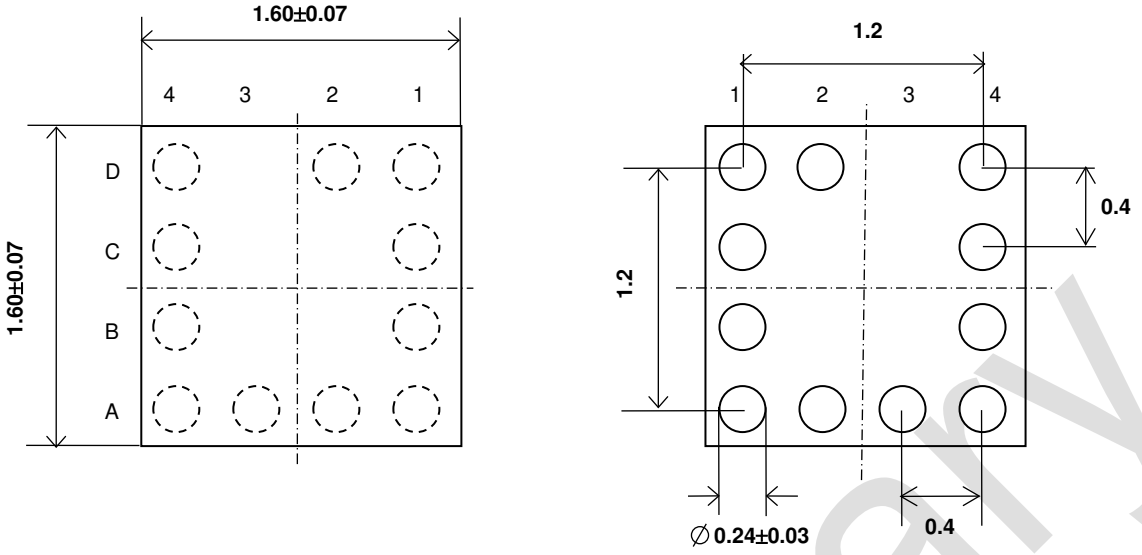
13.2. Pin Assignment

	4	3	2	1
D	RSTN		CAD1	CAD0
C	VID			VSS
B	SO			VDD
A	SDA/SI	SCL/SK	CSB	DRDY

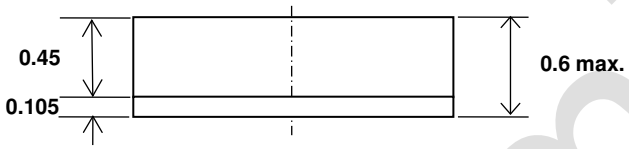
<Top view>

13.3. Outline Dimensions

[mm]



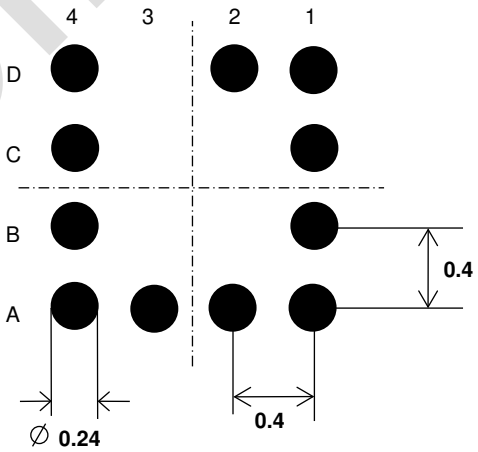
<Top view> <Bottom view>



<Side view>

13.4. Recommended Foot Print Pattern Outline

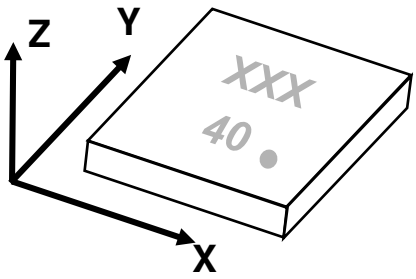
[mm]



<Top view>

14. Relationship between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions.



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