A5950

DC Motor Driver

FEATURES AND BENEFITS

- Overcurrent protection (OCP)
- Motor lead short-to-ground protection
- Motor lead short-to-battery protection
- Motor short protection
- Low-power standby mode
- Fault output
- Adjustable current limit option
- Current-to-voltage output
- Synchronous rectification – high-side
- Internal UVLO
- Crossover-current protection
- Thermal warning and shutdown function
- AEC-Q100 Grade 0 qualified – K version

DESCRIPTION

Designed for pulse-width-modulated (PWM) control of DC motors, the A5950 is capable of peak output currents up to ±3 A and operating voltages up to 40 V.

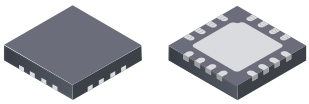
Input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to lower power dissipation during PWM operation.

Internal circuit protection includes overcurrent protection, motor lead short to ground or supply, thermal shutdown with hysteresis, undervoltage monitoring of VBB, and crossover-current protection.

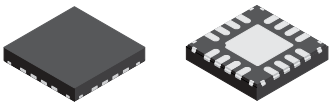
The A5950 is supplied in a low-profile 4 mm × 4 mm 16-contact QFN (suffix "EU") package with wettable flank option (suffix "-P"), or a 16-lead eTSSOP (suffix "LP"), all three with exposed power tab for enhanced thermal performance.

PACKAGES:

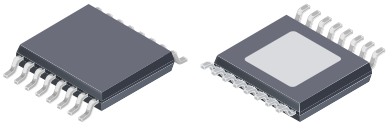
Not to scale



16-lead QFN
with exposed themal pad
(suffix EU, option -T)



16-lead QFN
with exposed themal pad
and wettable flank (suffix EU, option -P)



16-lead TSSOP
with exposed themal pad
(suffix LP)

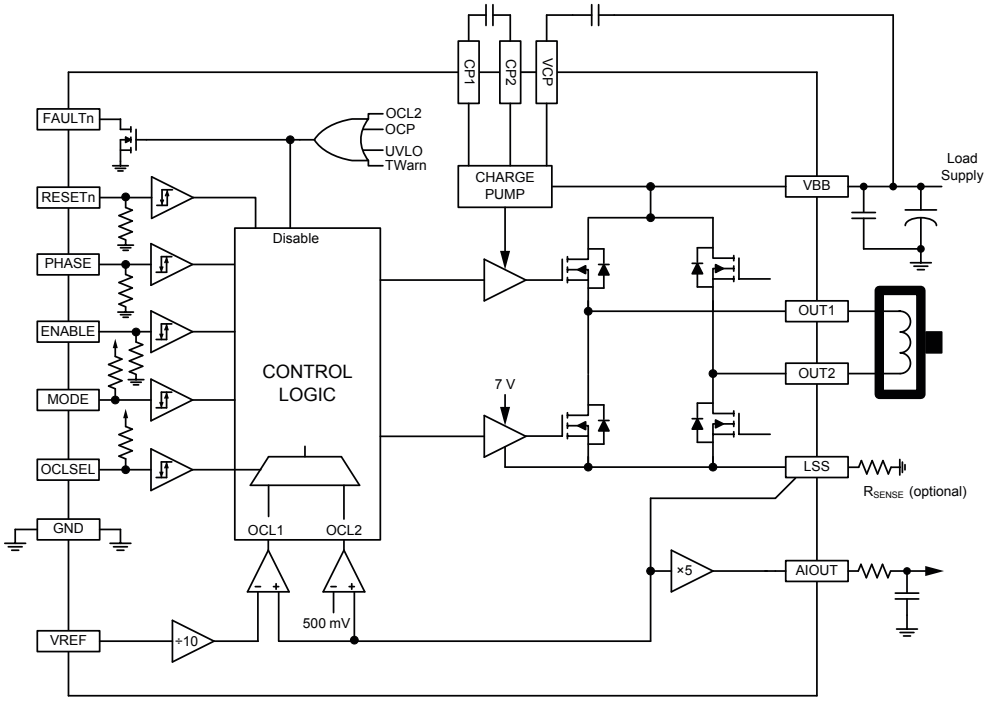


Figure 1: Functional Block Diagram

SPECIFICATIONS

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A (°C)	Packaging	Packing
A5950GEUSR-T	–40 to 105	16-lead QFN with exposed pad	6000 pieces per 13-in. reel
A5950GLPTR-T	–40 to 105	16-lead TSSOP with exposed pad	4000 pieces per 13-in. reel
A5950KEUSR-J	–40 to 150	16-lead QFN with exposed pad and wettable flank	6000 pieces per 13-in. reel
A5950KLPTR-T	–40 to 150	16-lead TSSOP with exposed pad	4000 pieces per 13-in. reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		40	V
Motor Outputs	V_{OUT}		–2 to 42	V
LSS	V_{LSS}		±0.5	V
		t_w < 200 ns	±2.5	V
Output Current	I_{OUT}	Continuous [1]	3	A
Transient Output Current	I_{OUTPK}	t_w < 500 ns	internally limited	A
VREF	V_{REF}		–0.3 to 6	V
Logic Input Voltage Range	V_{IN}		–0.3 to 6	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C
		Range K; limited by power dissipation	–40 to 150	°C

[1] Power dissipation and thermal limits must be observed.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]		Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	16-lead TSSOP (suffix LP)	JEDEC Hi-K board	34	°C/W
			2 layer PCB, 1-in.^{2} copper	51	°C/W
		16-lead QFN (suffix EU)	JEDEC Hi-K board	36	°C/W
			2 layer PCB, 1-in.^{2} copper	TBD	°C/W

[2] Additional thermal information available on the Allegro website.

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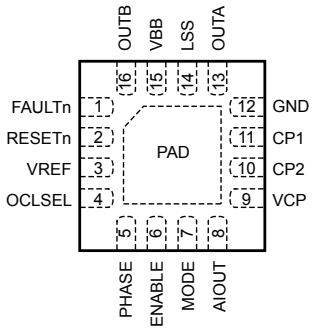
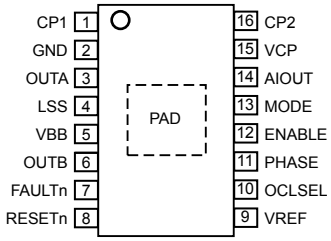
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



16-Lead QFN (EU) Package Pinout Diagram



16-Lead TSSOP (LP) Package Pinout Diagram

Terminal List Table

Name	Number		Function
	EU	LP	
AIOUT	8	14	Analog sense voltage output
CP1	11	1	Charge pump capacitor
CP2	10	16	Charge pump capacitor
ENABLE	6	12	Logic control input
FAULTn	1	7	Open drain logic output, active low
GND	12	2	Ground terminal
LSS	14	4	Sense voltage
MODE	7	13	Logic control input
OCLSEL	4	10	Logic control input
OUTA	13	3	Motor output
OUTB	16	6	Motor output
PHASE	5	11	Logic control input
RESETn	2	8	Logic control input, active low
VBB	15	5	Supply voltage
VCP	9	15	Charge pump capacitor
VREF	3	9	Analog input to set current limit
–	PAD	PAD	Exposed pad of the package providing enhanced thermal dissipation

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ELECTRICAL CHARACTERISTICS:

G Range Version: Valid at T_J = 25°C, V_{BB} = 5.5 to 40 V (unless noted otherwise)
K Range Version: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 40 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Supply Current	I_{BB}	Outputs off or Brake mode	–	5.8	9	mA
	$I_{BB(STANDBY)}$	Standby Mode, T_J = 25°C	–	1	5	µA
		Standby Mode, T_J = 150°C	–	10	25	µA
OUTPUT DRIVERS						
Source Driver On Resistance	$R_{DSON(source)}$	I = 3 A, T_J = 25°C, V_{BB} = 8 V	–	335	–	mΩ
		I = 3 A, T_J = 150°C, V_{BB} = 8 V	–	570	740	mΩ
		I = 3 A, T_J = 25°C, V_{BB} = 5.5 V	–	370	–	mΩ
		I = 3 A, T_J = 150°C, V_{BB} = 5.5 V	–	660	860	mΩ
Sink Driver On Resistance	$R_{DSON(sink)}$	I = 3 A, T_J = 25°C, V_{BB} = 8 V	–	365	–	mΩ
		I = 3 A, T_J = 150°C, V_{BB} = 8 V	–	640	835	mΩ
		I = 3 A, T_J = 25°C, V_{BB} = 5.5 V	–	390	–	mΩ
		I = 3 A, T_J = 150°C, V_{BB} = 5.5 V	–	730	950	mΩ
Body Diode Forward Voltage	V_F	I = 3 A	–	1.15	1.4	V
Output Rise time	t_R	V_{BB} = 12 V, 10% to 90%	50	100	200	ns
Output Fall Time	t_F	V_{BB} = 12 V, 90% to 10%	50	100	200	ns
Dead Time (Crossover)	t_D		–	350	550	ns
LOGIC INPUT AND OUTPUT						
Logic Output Voltage	V_O	I = 2 mA, fault asserted	–	0.2	0.5	V
Logic Output Leakage	I_{FLTn}	V = 5 V	–	–	5	µA
Logic Input Voltage	V_{IH}	PHASE, ENABLE, MODE, OCLSEL	2.0	–	5.5	V
	V_{IL}	PHASE, ENABLE, MODE, OCLSEL	0	–	0.8	V
	$V_{IHRESETn}$	RESETn	2.5	–	5.5	V
	$V_{ILRESETn}$	RESETn	0	–	0.4	V
Logic Input Hysteresis	V_{HYS}	PHASE, ENABLE, MODE, OCLSEL	200	355	500	mV
Logic Input Pull-Up Current	I_{PU}	OCLSEL, MODE; V_{IN} = 0 V	–20	–55	–90	µA
Logic Input Pull-Down Resistor	R_{PD}	RESETn, PHASE, ENABLE	25	50	80	kΩ

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2] For Range G devices, specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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ELECTRICAL CHARACTERISTICS (continued):
G Range Version: Valid at T_J = 25°C, V_{BB} = 5.5 to 40 V (unless noted otherwise)
K Range Version: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 40 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM TIMING						
Blank Time	t_{BLK}		2.7	3.2	3.7	µs
Fixed Off-time	t_{OFF}		22	25.5	29	µs
Percent Fast Decay	P_{FD}	Internal PWM chop	16	18	20	%
VREF Input Current	I_{VREF}		–5	<1	5	µA
VREF Input Range	V_{REF}		0	–	4.5	V
Current Sense Accuracy, External	A_{VREV}	V_{REF} = 2 V, V_{REF}/V_{LSS}	9.5	10	10.5	V/V
		V_{REF} = 250 mV, V_{REF}/V_{LSS}	8.4	10	11.6	V/V
SENSE Trip Level, Internal	V_{TRIP}	OCLSEL = low	450	500	550	mV
AIOUT Gain	A_V	I = 200 µA, V_{LSS} = 50 to 200 mV	4.3	5	5.7	V/V
		I = 200 µA, V_{LSS} = –50 to –200 mV	–4.3	–5	–5.7	V/V
Power Up Delay	t_{PU}		–	250	400	µs
PROTECTION CIRCUITS						
Overcurrent Threshold	I_{OCP}		3.0	–	–	A
Overcurrent Blank Time	t_{OCBLK}		2.9	3.4	3.9	µs
Overcurrent Off-Time	t_{OCP}		1.0	1.2	1.4	ms
UVLO Enable Threshold	V_{BBUVLO}	V_{BB} rising	5.1	–	5.4	V
UVLO Hysteresis	V_{BBUVLO}		250	300	350	mV
VCP Undervoltage	V_{CPUVLO}	V_{CP} falling	4.0	4.5	5.0	V
Thermal Warning Temperature	T_{JW}	Temperature increasing	–	160	–	°C
Thermal Warning Hysteresis	ΔT_{JWHYS}	Recovery = $T_{JW} - \Delta T_J$	–	20	–	°C
Thermal Shutdown Temperature	T_{JSD}	Temperature increasing	155	175	–	°C
Thermal Shutdown Hysteresis	ΔT_{JSDHYS}	Recovery = $T_{JSD} - \Delta T_J$	–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2] For Range G devices, specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

Device Operation

The A5950 is designed to operate DC motors. The output drivers are capable of 40 V and 3 A peak operating currents. Actual 100% steady-state DC current capability depends on thermal capability of the package and PCB, and ambient temperature. N-channel DMOS drivers feature internal synchronous rectification to reduce power dissipation. Peak current can be regulated by fixed off-time pulse-width-modulated (PWM) control circuitry.

Protection circuitry includes thermal shutdown, protection against shorted loads, or protection against output shorts to ground or supply. Undervoltage lockout prevents damage by keeping the outputs off until the driver has enough power supply voltage to operate normally.

Internal PWM Current Control

When the OCLSEL input is left open or tied high, peak output current is set by sensing the current through an external sense resistor.

$$I_{PEAK} = V_{REF} / (10 \times R_{SENSE})$$

When the peak current is exceeded, the driver will operate in mixed decay mode for fixed time t_{OFF} before re-enabling the next drive cycle.

To disable the current control feature, leave OCLSEL open or tie OCLSEL high, and connect LSS to GND.

Blank Function

The internal current sense circuit is ignored for some time after PWM transitions so as not to falsely sense overcurrent events due to motor capacitance and switching transients. This blank time, typically 3 µs, results in a minimum on-time of the PWM.

Standby Mode

Low-power standby mode is activated when RESETn is low. Low-power standby mode disables most of the internal circuitry, including the charge pump and the regulator. When the A5950 is coming out of standby mode, the charge pump should be allowed to reach its regulated voltage (a maximum delay of 400 µs) before any PWM commands are issued to the device.

Overcurrent Protection

A current monitor will protect the IC from damage due to output shorts. If a short is detected, the IC will disable the outputs. The fault latch is cleared after a timer of duration t_{OCP} expires, and the outputs are re-enabled. During OCP events, the absolute maximum ratings may be exceeded for a short time before the device latches off.

Thermal Monitoring

If the die temperature increases to approximately T_{JSD}, the full bridge outputs will be disabled unit the internal temperature falls below a hysteresis level of T_{JSDHYS}. Thermal warning occurs approximately 20 degrees less than T_{JSD}. Thermal warning triggers a fault but does not disable the drivers.

OCL Option

If the OCLSEL input is left open or tied high, inrush and stall current can be controlled by selection of VREF and the sense resistor value. If the OCLSEL input is connected to GND, the VREF pin is ignored, and the bridge outputs are latched off when the voltage on SENSE exceeds 500 mV typically. While the outputs are latched off in this condition, the FAULTn output will be asserted and pulled low. As with OCP events, the device will then be re-enabled after a timer of duration TOCP expires.

FAULTn Output

FAULTn is an open-drain output and is driven low to indicate any of the following conditions:

1. OCP fault event – Short to VBB, GND, shorted load
2. OCL event (if OCLSEL = low)
3. Thermal warning
4. Undervoltage (VBB or VCP)

AIOUT

An analog output can be used to monitor the load current flowing through the external sense resistor (if a sense resistor is installed). Positive voltage on the sense resistor is gained by 5 and output on the AIOUT terminal. Negative voltage on the sense resistor is gained by –5 and output on the AIOUT terminal. As the load current does not flow through the sense resistor during a slow-decay (brake) condition, the AIOUT output is approximately 0 V when in slow-decay.

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Table 1: Control Logic

RESETn	PHASE	ENABLE	MODE	$I > I_{CL}$	OUT1	OUT2	Function
1	1	1	X	false	H	L	Forward
1	0	1	X	false	L	H	Reverse
1	X	0	1	false	H	H	Brake (slow decay)
1	1	0	0	false	L	H	Fast Decay SR [1]
1	0	0	0	false	H	L	Fast Decay SR [1]
1	1	1	X	true	L/H	H	Chop (mixed decay) [1]
1	0	1	X	true	H	L/H	Chop (mixed decay) [1]
0	X	X	X	X	Z	Z	Standby Mode

[1] Outputs change to Hi-Z state when in fast decay and load current approaches zero.

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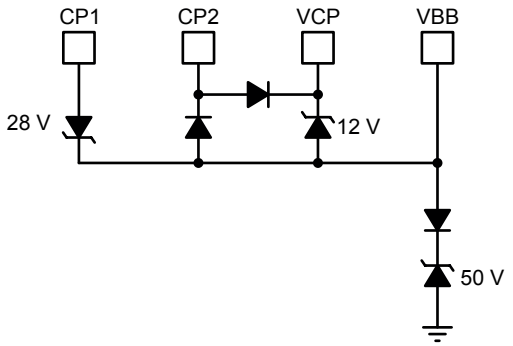
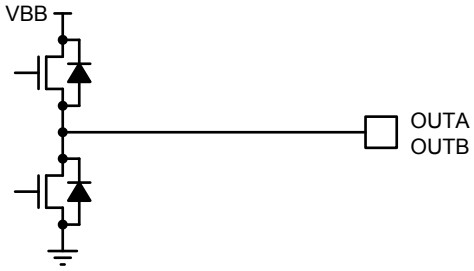
PIN STRUCTURES

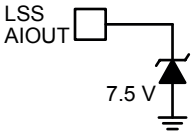
CP1, CP2, OUTA, OUTB, VBB, VCP



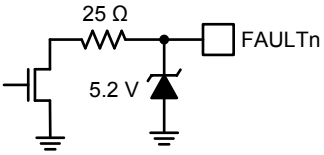
OUTA, OUTB



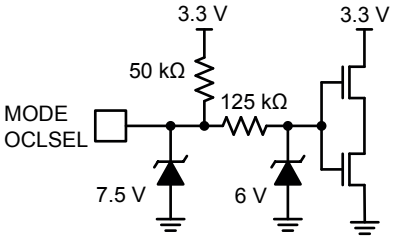
AIOUT, LSS



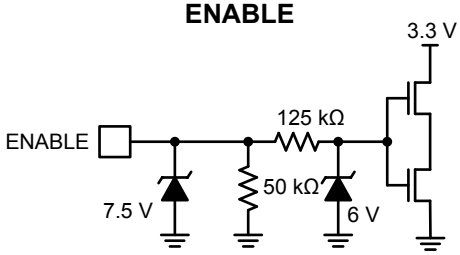
FAULTn



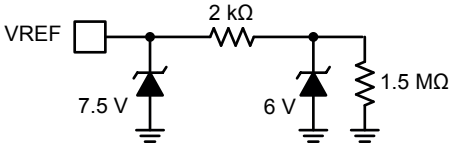
MODE, OCLSEL



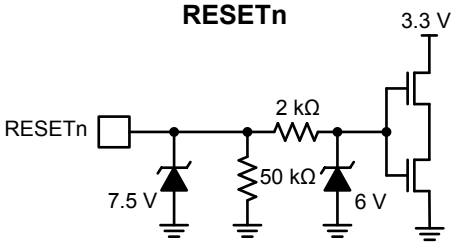
ENABLE



VREF



RESETn



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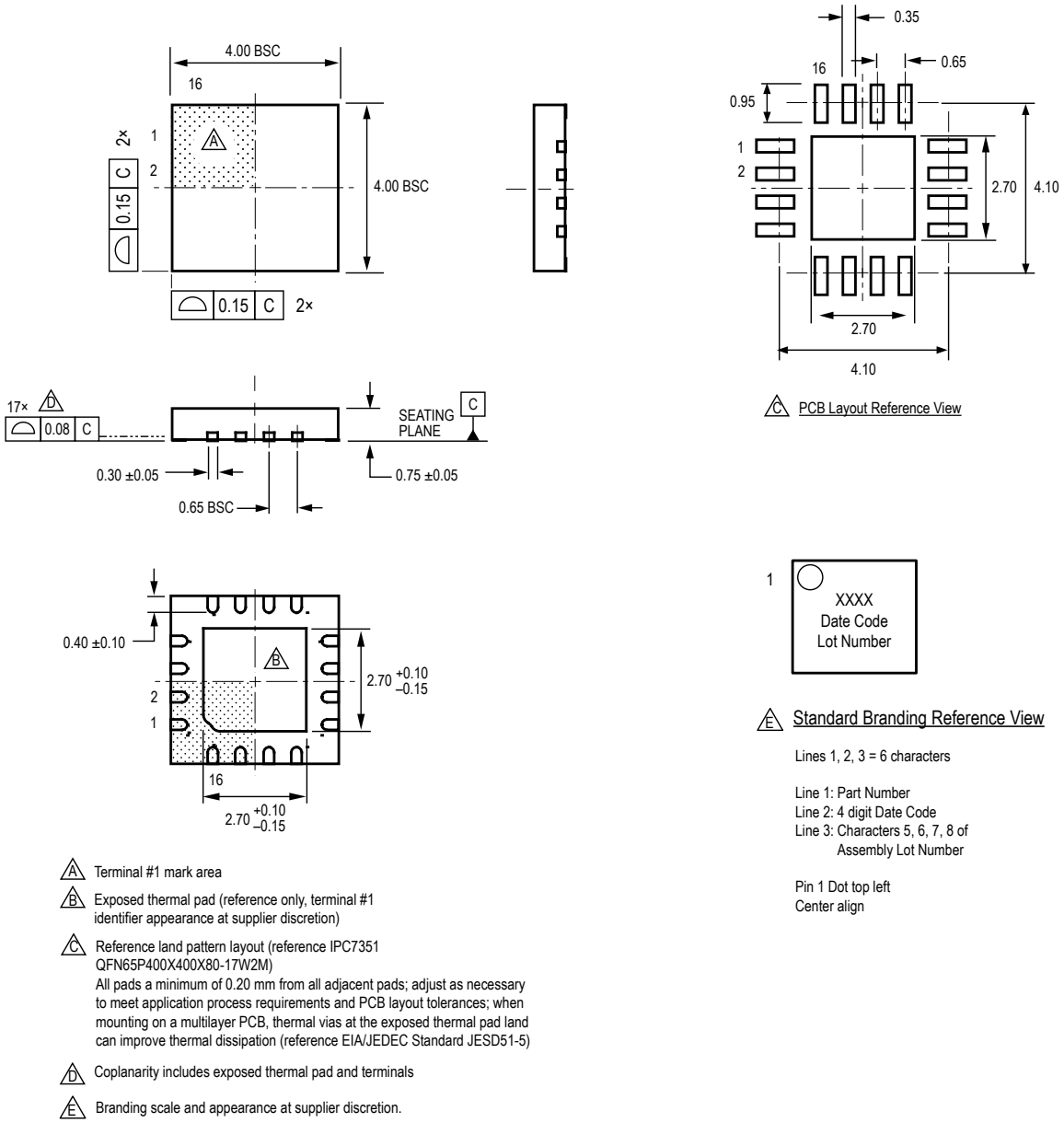
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGC.)
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN65P400X400X80-17W2M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 2: EU Package, 16-Lead QFN with Exposed Thermal Pad

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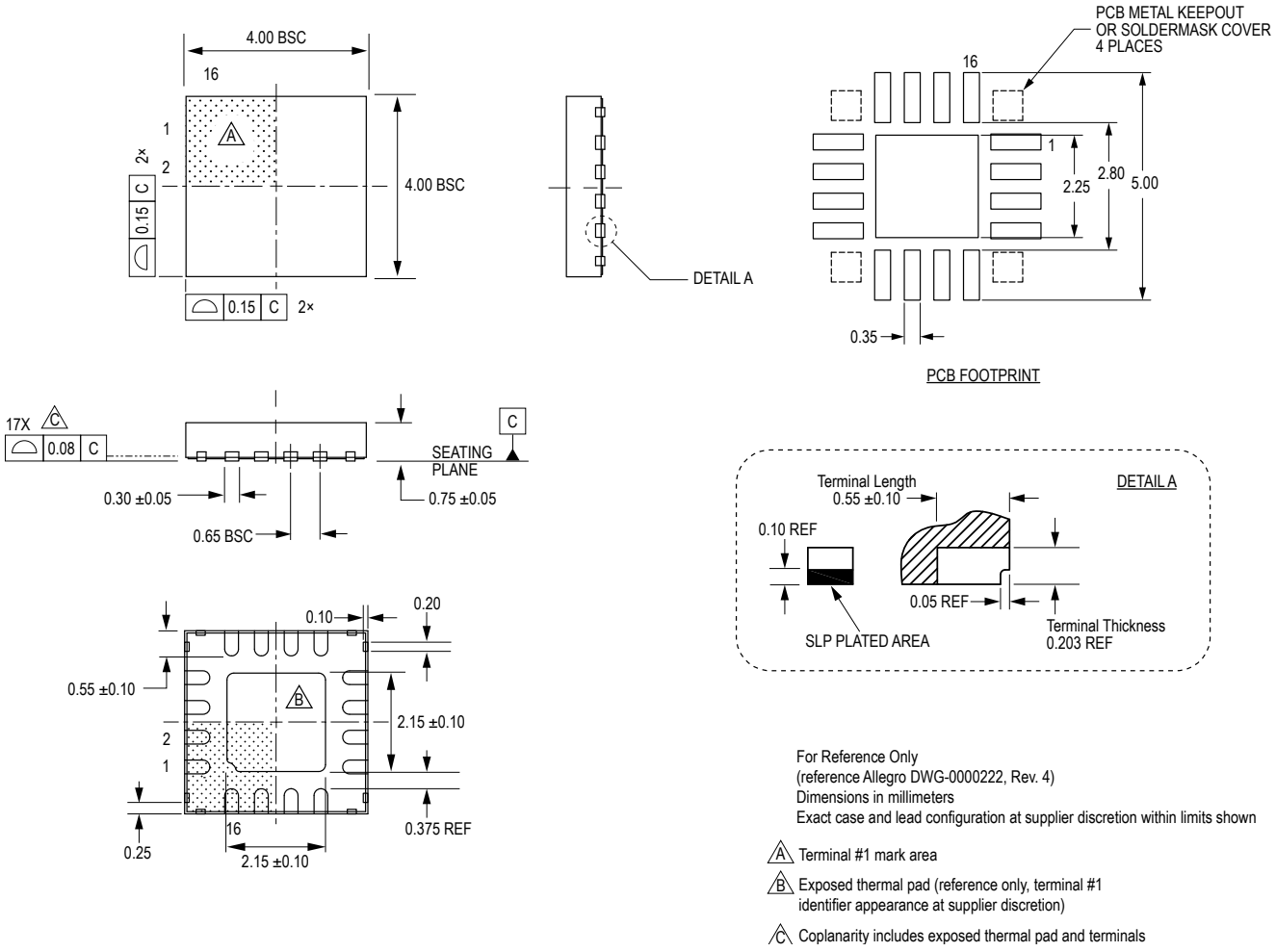

Figure 3: EU Package, 16-Lead QFN with Exposed Thermal Pad and Wettable Flank

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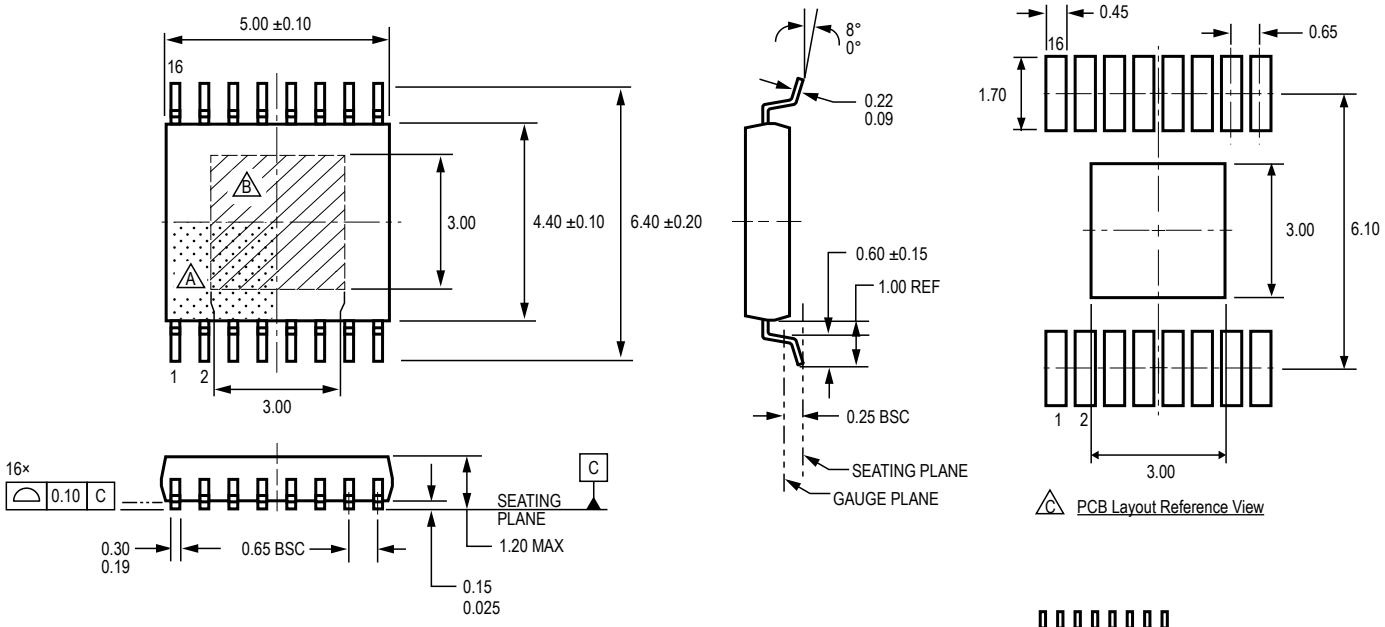
For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 4: LP Package, 16-Lead TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	November 14, 2016	Initial release
1	April 24, 2017	Updated Selection Guide
2	May 11, 2017	Corrected packing options in Selection Guide
3	June 22, 2017	Added Pin Structures
4	September 8, 2017	Update automotive qualification to grade 0 (p. 1); updated test conditions Junction Temperature maximum, Standby Bias Current, and R_{DSON} values (p. 4-5)
5	September 12, 2018	Minor editorial updates
6	September 16, 2019	Minor editorial updates
7	January 6, 2021	Added PCB Layout to EU-16 wettable flank package drawing (p. 10)
8	February 9, 2022	Updated package drawings (pages 9-11)

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