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# FDZ375P

## P-Channel 1.5 V Specified PowerTrench® Thin WL-CSP MOSFET -20 V, -3.7 A, 78 mΩ

### Features

- Max  $r_{DS(on)}$  = 78 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -2.0$  A
- Max  $r_{DS(on)}$  = 92 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -1.5$  A
- Max  $r_{DS(on)}$  = 112 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -1.0$  A
- Max  $r_{DS(on)}$  = 150 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -1.0$  A
- Occupies only 1.0 mm<sup>2</sup> of PCB area. Less than 30% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.4 mm height when mounted to PCB
- RoHS Compliant

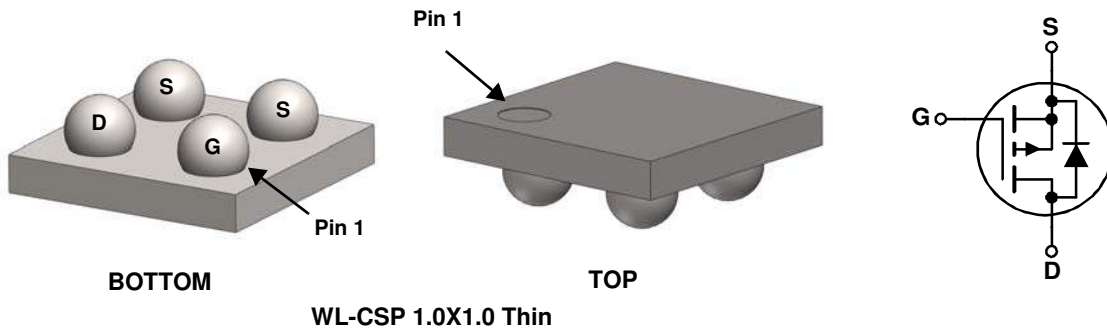


### General Description

Designed on Fairchild's advanced 1.5 V PowerTrench® process with state of the art "fine pitch" Thin WLCSP packaging process, the FDZ375P minimizes both PCB space and  $r_{DS(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low  $r_{DS(on)}$ .

### Applications

- Battery management
- Load switch
- Battery protection



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated Value	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	-3.7
	-Pulsed		-12
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	1.7
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	0.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

Symbol	Parameter	Rated Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	75
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	260

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
N	FDZ375P	WL-CSP 1.0X1.0 Thin	7"	8 mm	5000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-12		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.3	-0.5	-1.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		2		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\ \text{V}, I_D = -2.0\ \text{A}$		65	78	m $\Omega$
		$V_{GS} = -2.5\ \text{V}, I_D = -1.5\ \text{A}$		77	92	
		$V_{GS} = -1.8\ \text{V}, I_D = -1.0\ \text{A}$		92	112	
		$V_{GS} = -1.5\ \text{V}, I_D = -1.0\ \text{A}$		112	150	
		$V_{GS} = -4.5\ \text{V}, I_D = -2.0\ \text{A}, T_J = 125^\circ\text{C}$		98	143	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\ \text{V}, I_D = -3.3\ \text{A}$		11		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		650	865	pF
$C_{oss}$	Output Capacitance			110	145	pF
$C_{rss}$	Reverse Transfer Capacitance			95	150	pF

### Switching Characteristics

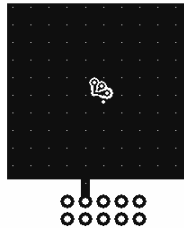
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\ \text{V}, I_D = -3.3\ \text{A}, V_{GS} = -4.5\ \text{V}, R_{GEN} = 6\ \Omega$		5.3	11	ns
$t_r$	Rise Time			8.2	15	ns
$t_{d(off)}$	Turn-Off Delay Time			138	221	ns
$t_f$	Fall Time			84	124	ns
$Q_g$	Total Gate Charge		$V_{GS} = -4.5\ \text{V}, V_{DD} = -10\ \text{V}, I_D = -3.3\ \text{A}$		11	15
$Q_{gs}$	Gate to Source Charge			0.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.1	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = -1.3\ \text{A}$ (Note 2)		-0.7	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -3.3\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		68	109	ns
$Q_{rr}$	Reverse Recovery Charge			43	69	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



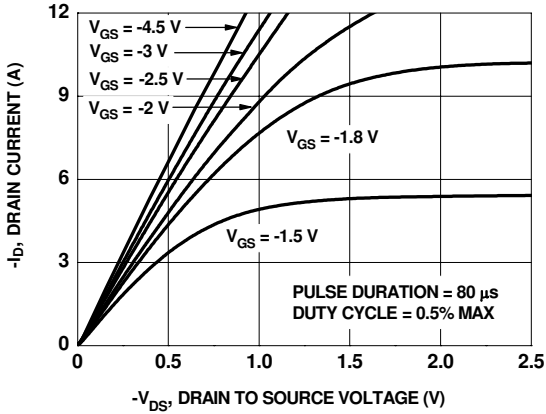
a. 75 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



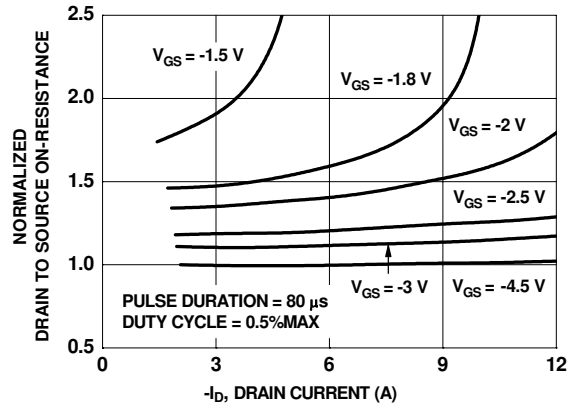
b. 260 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

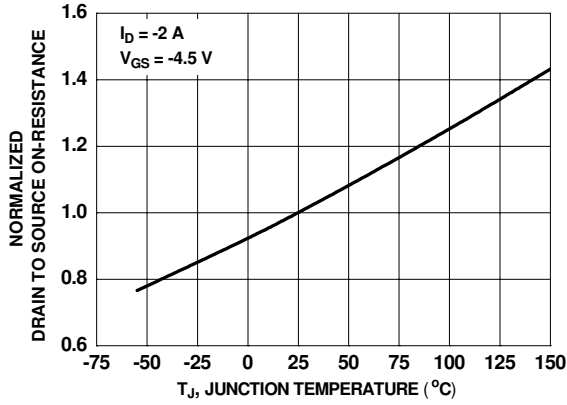
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



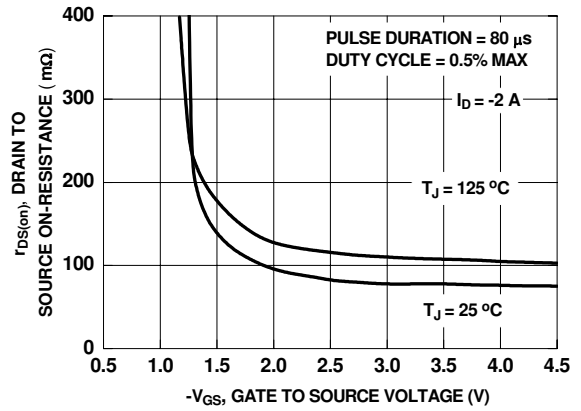
**Figure 1. On Region Characteristics**



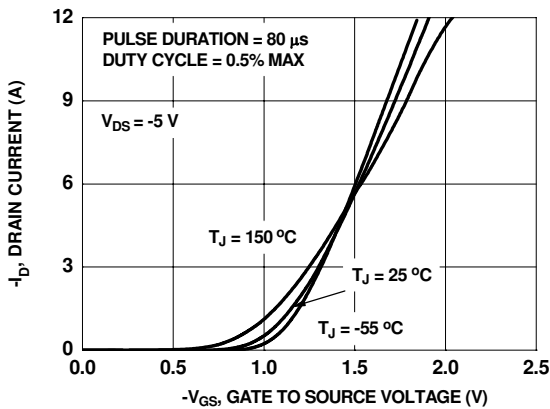
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



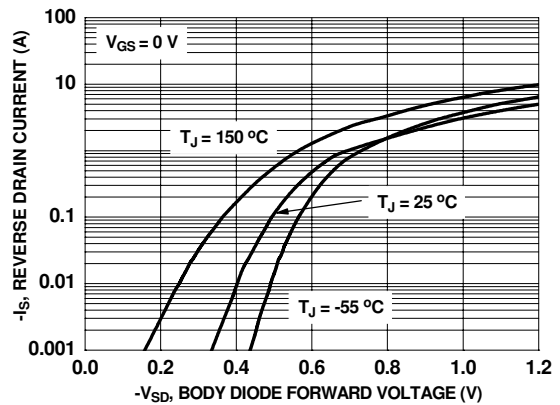
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

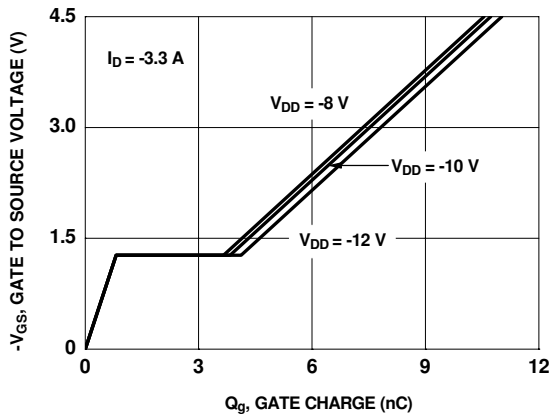


**Figure 5. Transfer Characteristics**

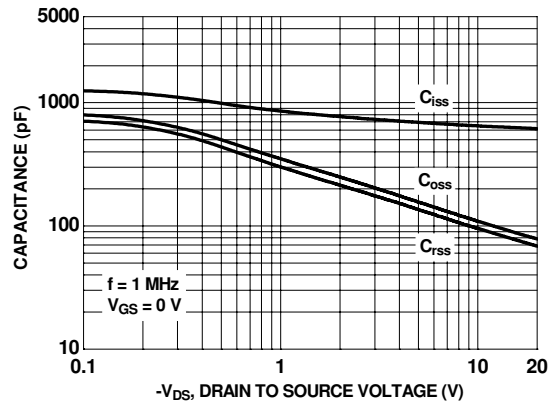


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

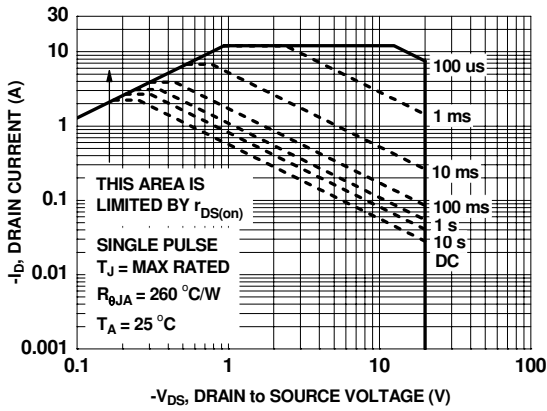
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



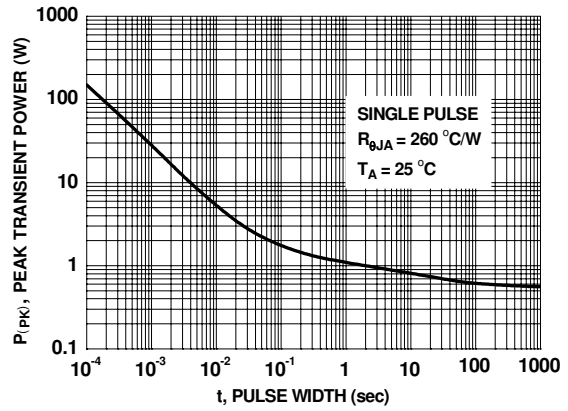
**Figure 7. Gate Charge Characteristics**



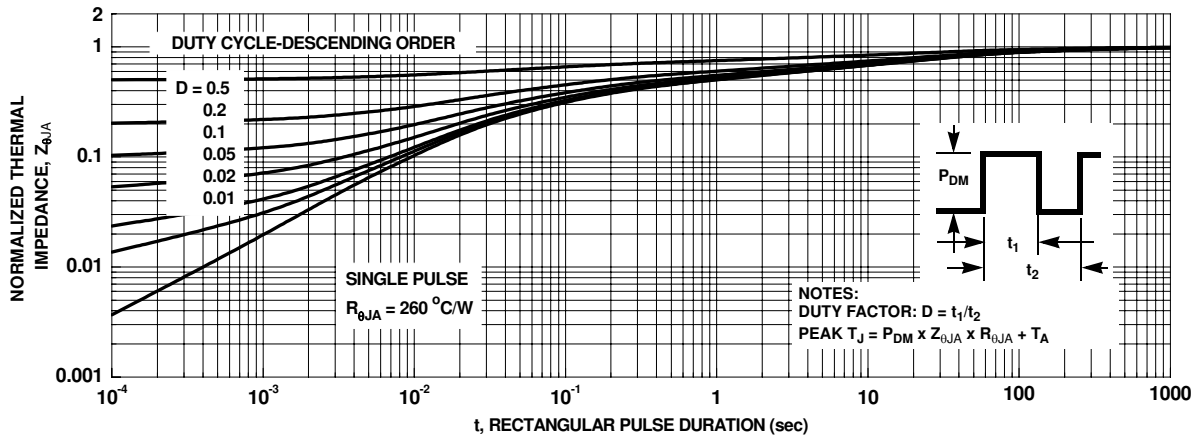
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

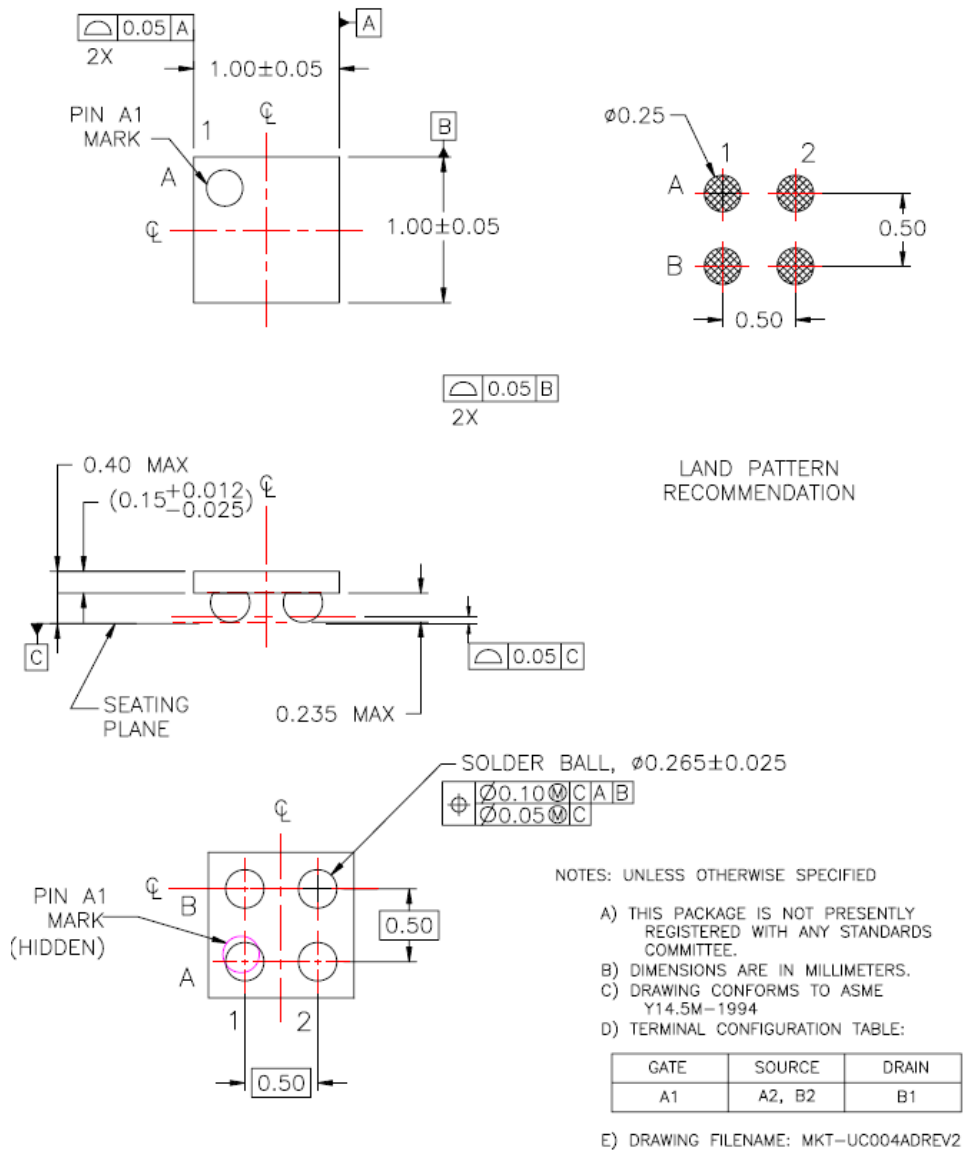


**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout





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