

T-46-07-09

175

54/74175
54S/74S175
54LS/74LS175
 QUAD D FLIP-FLOP

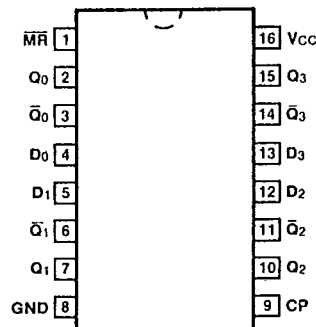
DESCRIPTION — The '175 is a high speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- TRUE AND COMPLEMENT OUTPUT

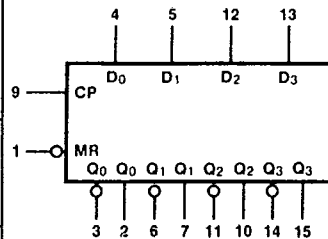
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5% T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74175PC, 74S175PC 74LS175PC		9B
Ceramic DIP (D)	A	74175DC, 74S175DC 74LS175DC	54175DM, 54S175DM 54LS175DM	6B
Flatpak (F)	A	74175FC, 74S175FC 74LS175FC	54175FM, 54S175FM 54LS175FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D ₀ — D ₃	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
MR	Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
Q ₀ — Q ₃	True Outputs	20/10	25/12.5	10/5.0 (2.5)
Q ₀ — Q ₃	Complement Outputs	20/10	25/12.5	10/5.0 (2.5)

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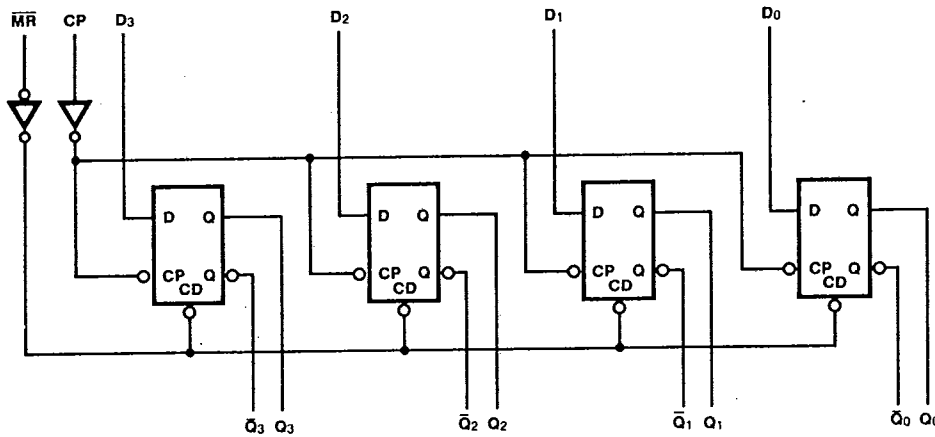
FUNCTIONAL DESCRIPTION — The '175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A LOW input on the Master Reset (\bar{MR}) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs. The '175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

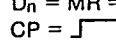
INPUTS		OUTPUTS	
@ $t_n, \bar{MR} = H$		@ t_{n+1}	
D_n		Q_n	\bar{Q}_n
L		L	H
H		H	L

t_n = Bit time before clock positive-going transition
 t_{n+1} = Bit time after clock positive-going transition
 H = HIGH Voltage Level
 L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I _{CC}	Power Supply Current	45		96		18		mA	V _{CC} = Max D _n = $\overline{\text{MR}}$ = 4.5 V CP = 

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω		C _L = 15 pF R _L = 280 Ω		C _L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	25		75		30		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	30 35		12 17		25 25		ns	Figs. 3-1, 3-8
t _{PHL}	Propagation Delay $\overline{\text{MR}}$ to Q _n	35		22		33		ns	Figs. 3-1, 3-16
t _{PLH}	Propagation Delay $\overline{\text{MR}}$ to Q _n	25		15		24		ns	Figs. 3-1, 3-16

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AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW D _n to CP	20		5.0		10		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW D _n to CP	5.0		3.0		5.0		ns	
t _w (H)	CP Pulse Width HIGH	20		7.0		15		ns	Fig. 3-8
t _w (L)	$\overline{\text{MR}}$ Pulse Width LOW	20		7.0		18		ns	Fig. 3-16
t _{rec}	Recovery Time MR to CP	25		5.0		12		ns	Fig. 3-16