ACNU-4803

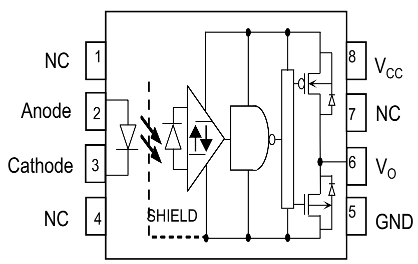
Inverted Logic High CMR Intelligent Power Module (IPM) and Gate Drive Interface Optocoupler

Description

The Broadcom® ACNU-4803 is a single-channel fast-speed optocoupler in SSO8 footprint. It contains a AlGaAs LED and photo detector with a built-in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The totem pole output eliminates the need for a pull-up resistor and allows for direct drive intelligent power modules. Minimized propagation delay differences between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead times.

The ACNU-4803 is suitable for IPM interface isolation, AC and brushless DC motor drives, industrial inverters and space-constrained industrial applications. This SSO8 package platform features wide 11-mm creepage and 10.5-mm clearance, high insulation voltage of V_{iorm} = 1414 V_{peak} and compact footprint which is 40% smaller than the 400-mil DIP8 package.

Functional Diagram



NOTE: A 0.1-µF bypass capacitor must be connected between pins V_{CC} and GND. Truth Table guaranteed: Vcc from 4.5V to 30V.

Features

- 11-mm creepage, 10.5-mm clearance in compact SSO8 package
- Positive output type (totem pole output)
- Wide supply voltage: 4.5V to 30V
- Maximum propagation delays, t_{PHL}/t_{PLH} at 150 ns/ 120 ns
- Propagation delay difference (PDD): minimum/ maximum at –130 ns/+130 ns
- Maximum pulse width distortion (PWD), 90 ns
- Hysteresis
- 50 kV/µs minimum common-mode rejection at V_{CM} = 1500V
- Guaranteed performance within temperature range: –40°C to +105°C
- Worldwide safety approval (pending):
  - UL1577 recognized, 5000Vrms/1min
  - CSA Approval
  - IEC 60747-5-5 Approval for Reinforced Insulation

Applications

- IPM interface isolation
- AC and brushless DC motor drives
- Industrial inverters
- General digital isolation

Truth Table

LED	Output
ON	Low
OFF	High

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

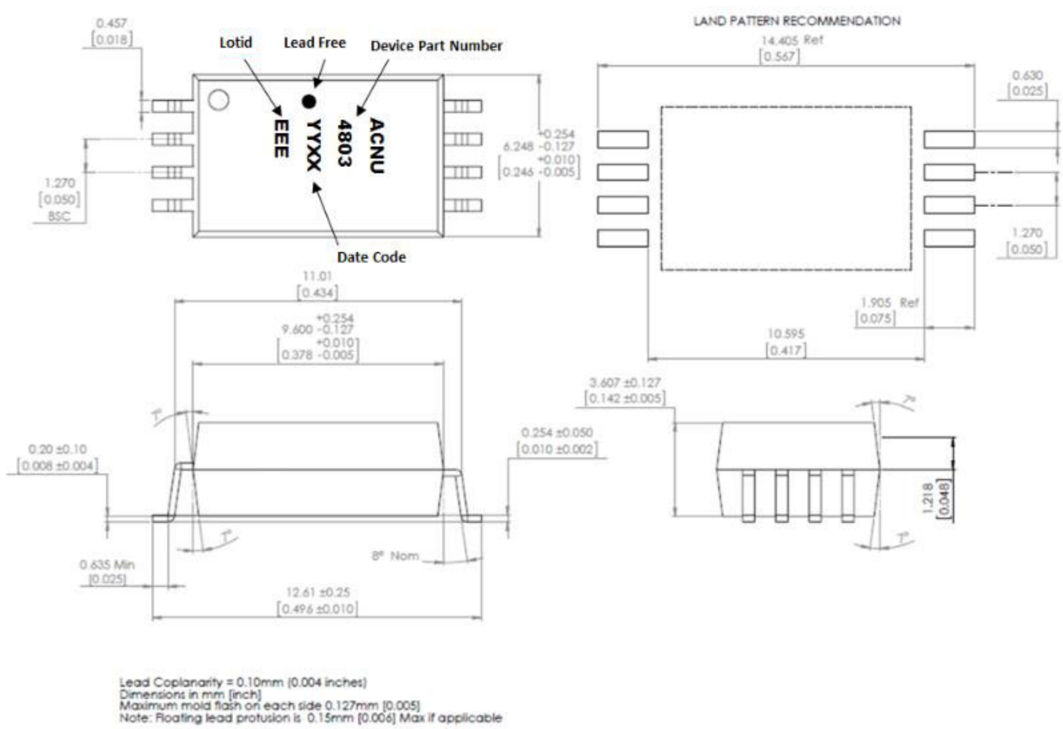
ACNU-4803 is UL Recognized with 5000 V_{rms} for 1 minute per UL1577.

Part Number	Option RoHs Compliant	Package	Surface Mount	Tape and Reel	UL 1577	IEC 60747-5-5	Quantity
ACNU-4803	-000E	11-mm Stretched SO8	X		X	X	80 per tube
	-500E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Package Outline Drawing

ACNU-4803 SSO8 Package



Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACNU-4803 is pending approval by the following organizations:

UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS} File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.
IEC 60747-5-5	Maximum Working Insulation Voltage V_{iorm} = 1414V_{peak}

Insulation and Safety Related Specifications

Parameter	Symbol	ACNU-4803	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	10.5	mm	Measured from the input terminals to the output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	11.0	mm	Measured from the input terminals to the output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>300	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC 60747-5-5 Insulation Characteristics[1]

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/39, Table 1			
for rated mains voltage ≤ 600 V_{rms}		I - IV	
for rated mains voltage ≤ 1000 V_{rms}		I - III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} ×1.875 = V_{PR}, 100% Production Test with t_m = 1s, Partial discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10s, Partial discharge < 5 pC	V_{PR}	2262	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

1. These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety limit data shall be ensured by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	125	°C
Operating Temperature	T_A	–40	105	°C
Average Forward Input Current	$I_{F(avg)}$	—	20	mA
Peak Transient Input Current (≤1 µs pulse width, 300 pps) (<200 µs pulse width, <1% duty cycle)	$I_{F(trans)}$	 — —	 1.0 40	 A mA
Reversed Input Voltage	V_R	—	5	V
Average Output Current	I_O	—	50	mA
Supply Voltage	V_{CC}	0	35	V
Output Voltage	V_O	–0.5	35	V
Input Power Dissipation	P_I	37		mW
Output Power Dissipation	P_O	173		mW
Solder Reflow Temperature Profile	Refer to Solder Reflow Profile			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.5	30	V
Input Current, High Level	I_{FH}	12	20	mA
Operating Temperature	T_A	–40	105	°C
Forward Input Voltage (OFF)	$V_{F(OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over recommended operating T_A = –40°C to 105°C, V_{CC} = 4.5V to 30V, $I_{F(ON)}$ = 12 mA to 20 mA, $V_{F(OFF)}$ =0V to 0.8V and unless otherwise specified. All typicals are at T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions	Figure	Note
Logic Low Output Voltage	V_{OL}	—	—	0.3	V	I_{OL} = 3.5 mA	1, 3	
		—	—	0.5	V	I_{OL} = 6.5 mA		
Logic High Output Voltage	V_{OH}	V_{CC}–0.3	V_{CC}–0.04	—	V	I_{OH} = –3.5 mA	2, 3, 8	
		V_{CC}–0.5	V_{CC}–1.07	—	V	I_{OH} = –6.5 mA		
Logic Low Supply Current	I_{CCL}	—	1.5	3.0	mA	V_{CC} = 5.5V, I_F = 12 mA, I_O = 0 mA		
		—	1.7	3.0	mA	V_{CC} = 30V, I_F = 12 mA, I_O = 0 mA		
Logic High Supply Current	I_{CCH}	—	1.5	3.0	mA	V_{CC} = 5.5V, V_F = 0V, I_O = 0 mA		
		—	1.7	3.0	mA	V_{CC} = 30V, V_F = 0V, I_O = 0 mA		
Threshold Input Current Low to High	I_{FLH}	—	4.0	8.7	mA			
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V			
Logic Low Output Current	I_{OL}	125	200	—	mA	V_{CC} = 5.5V, I_F = 12 mA, V_O = 5.5V		a
		125	200	—	mA	V_{CC} = 30V, I_F = 12 mA, V_O = 30V		
Logic High Output Current	I_{OH}	—	–200	–125	mA	V_{CC} = 5.5V, V_F = 0V, V_O = 0V		a
		—	–200	–125	mA	V_{CC} = 30V, V_F = 0V, V_O = 0V		
Input Forward Voltage	V_F	1.3	1.5	1.7	V	T_A = 25°C, I_F= 12 mA	4	
		—	—	1.85	V	I_F= 12 mA		
Input Reversed Breakdown Voltage	BV_R	5	—	—	V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$	—	1.7	—	mV/°C	I_F = 12 mA		
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0		b

a. Output is sourced at –125 mA/125 mA with a maximum pulse width of 500 µs.

b. Input capacitance is measured between pin 2 and pin 3.

Switching Specifications

Over recommended operating T_A = –40°C to 105°C, V_{CC} = 4.5V to 30V, $I_{F(ON)}$ = 12 mA to 20 mA, $V_{F(OFF)}$ = 0V to 0.8V and unless otherwise specified. All typicals are at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	—	95	150	ns	C_L = 100 pF, V_F = 0V → $I_{F(ON)}$ = 12 mA	6, 7, 9	a
		—	—	150	ns	Loaded as per Figure 5	5	b
Propagation Delay Time to Logic High at Output	t_{PLH}	—	75	120	ns	C_L = 100 pF, $I_{F(ON)}$ = 12 mA → V_F = 0V	6, 7, 9	a
		—	—	120	ns	Loaded as per Figure 5	5	b
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$ = PWD	—	—	90	ns	C_L = 100 pF		c
		—	—	90		Loaded as per Figure 5		
Propagation Delay Difference Between Any Two Parts	PDD	–130	—	130	ns	C_L = 100 pF		d
		–130	—	130	ns	Loaded as per Figure 5		
Output Rise Time (10% to 90%)	t_r	—	6	—	ns		5, 6	
Output Fall time (90% to 10%)	t_f	—	6	—	ns		5, 6	
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	50	—	—	kV/µs	T_A = 25°C V_{CM} = 1500V, I_F = 12 mA, V_{CC} = 5V	10	e
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	50	—	—	kV/µs	T_A = 25°C, V_{CM} = 1500V, V_F = 0V, V_{CC} = 5V	10	e

a. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 50% point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 50% point on the trailing edge of the output pulse.

b. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

c. Pulse Width Distortion (PWD) is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.

d. The difference of t_{PLH} and t_{PHL} between any two devices under the same test condition.

e. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8V. Note: Split resistors (R1 / R2) must be used at both ends of the LED.

Package Characteristics

All Typical at T_A = 25 C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions Note	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH ≤ 50%, t = 1 min., T_A = 25°C	a, b, c
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 Vdc	b
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C	b

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

b. In device considered a two-terminal device: pins 1, 2, 3, and 4 are shorted together and pins 5, 6, 7, and 8 are shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage. 4500 V_{RMS} for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.

UVLO

Figure 11 and Figure 12 show typical output waveforms during power-up and power-down processes.

Figure 1: Typical Logic Low Output Voltage vs. Temperature

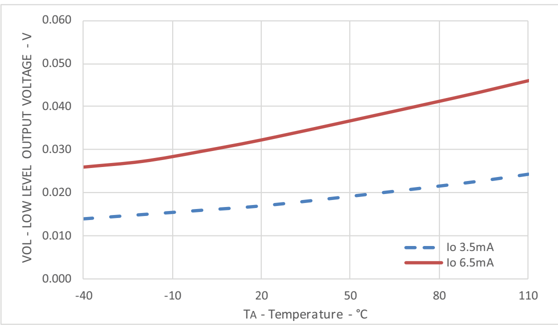


Figure 2: Typical Logic High Output Voltage vs. Temperature

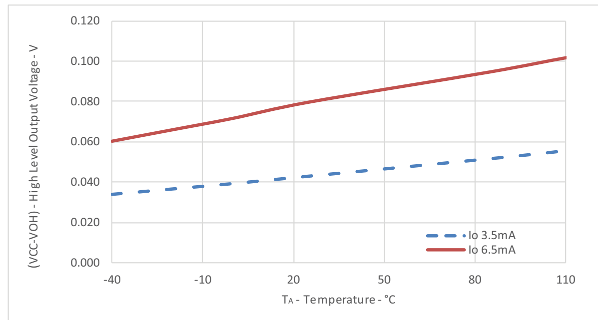


Figure 3: Typical Output Voltage vs. Forward Input Current

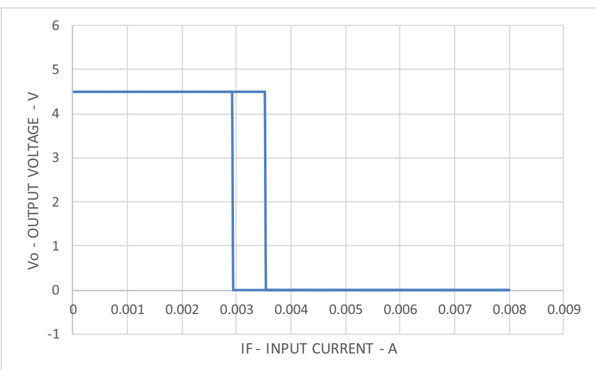


Figure 4: Typical Input Diode Forward Characteristic

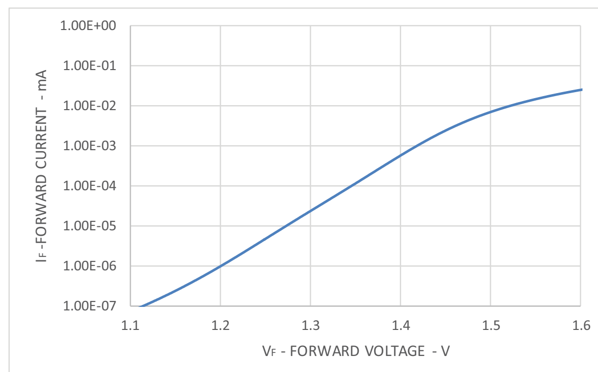


Figure 5: Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

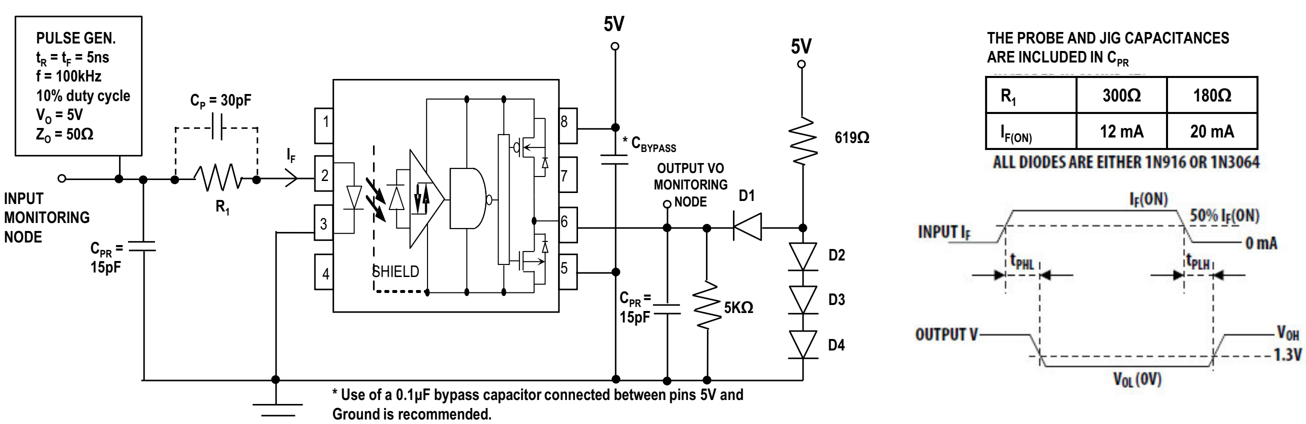


Figure 6: Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

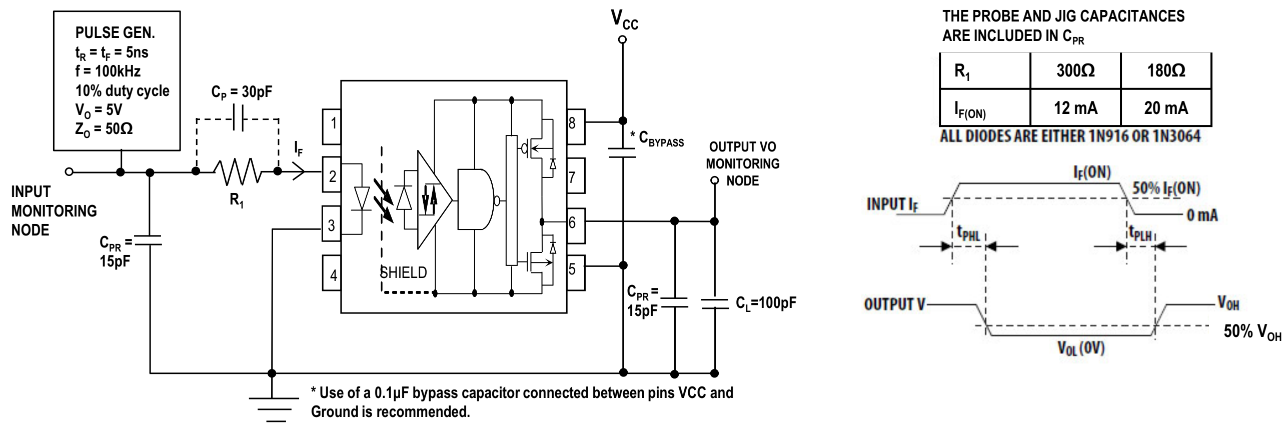


Figure 7: Typical Propagation Delay vs. Temperature

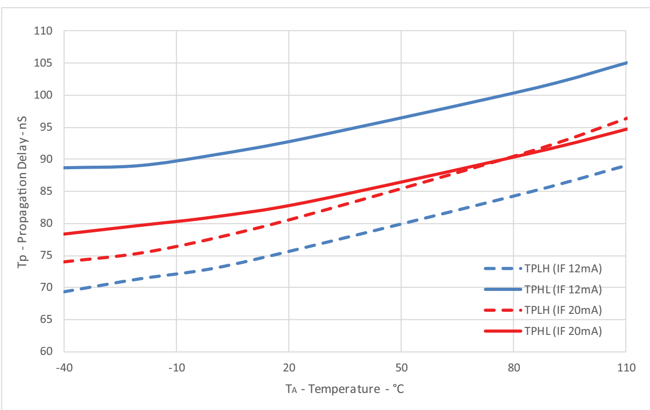


Figure 8: Typical Logic High Output Voltage vs. Supply Voltage

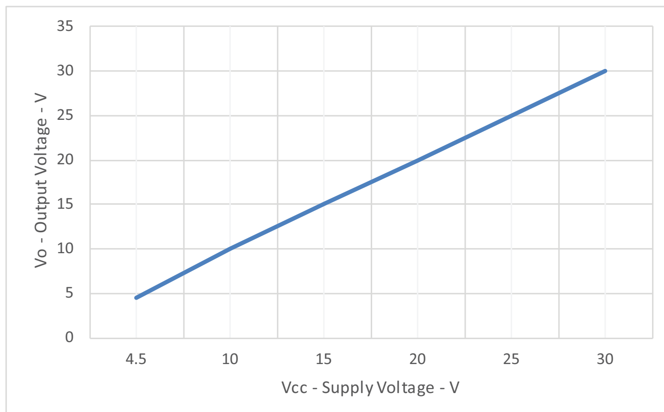


Figure 9: Typical Propagation Delay vs. Supply Voltage

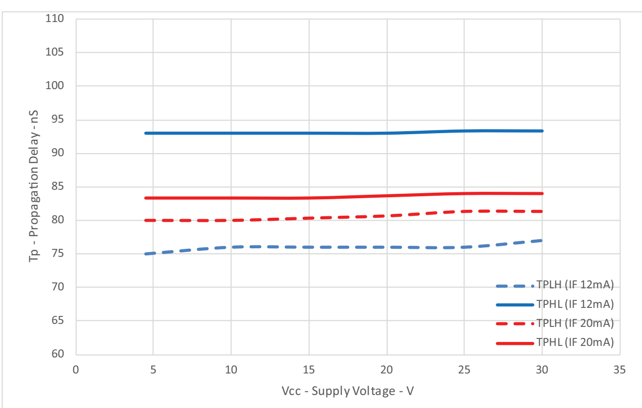


Figure 10: Test Circuit for Common Mode Transient Immunity and Typical Waveforms

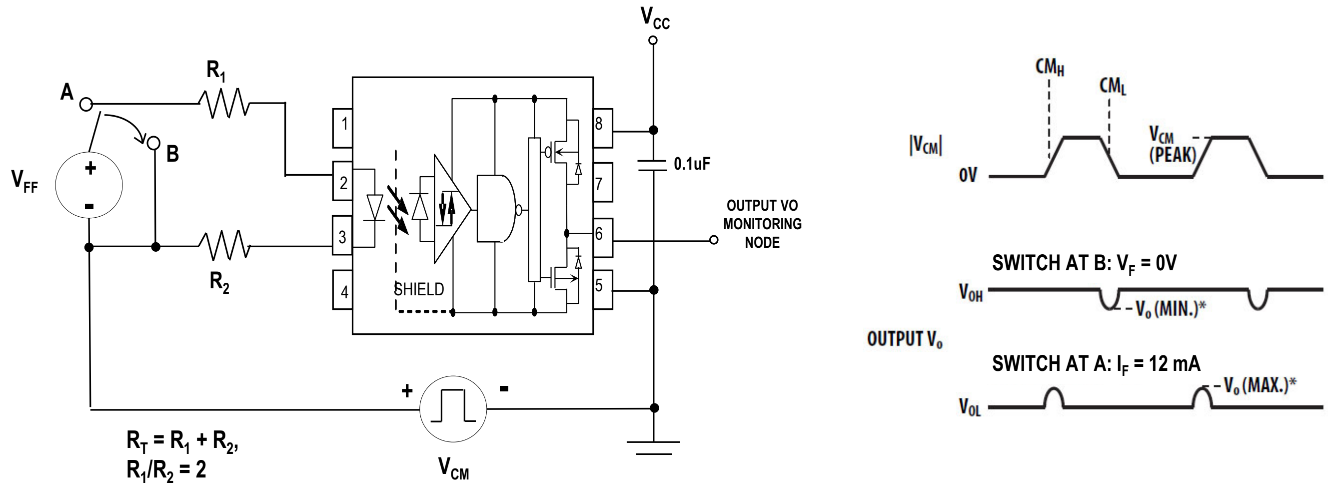


Figure 11: V_{CC} Ramp When LED OFF

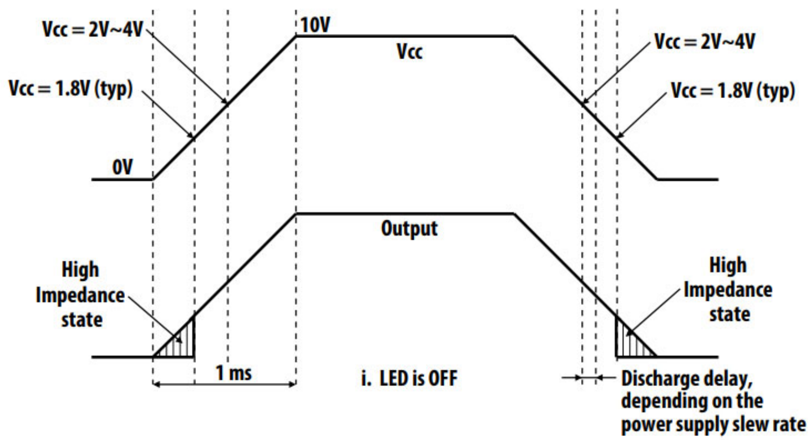


Figure 12: V_{CC} Ramp When LED ON