*Click **here** to ask an associate for production status of specific part numbers.*

MAX78002

Artificial Intelligence Microcontroller with Low-Power Convolutional Neural Network Accelerator

General Description

Artificial intelligence (AI) requires extreme computational horsepower, but Analog Devices is cutting the power cord from AI insights. The MAX78002 is a new breed of AI microcontroller that enables neural networks to execute at ultra-low power and live at the edge of the IoT. This device combines the most energy-efficient AI processing with Analog Devices' proven ultra-low-power microcontrollers. Our hardware-based CNN accelerator enables battery-powered applications to execute AI inferences while expending only millijoules of energy.

The MAX78002 is an advanced system-on-chip featuring an Arm® Cortex®-M4 with FPU CPU for efficient system control with an ultra-low-power deep neural-network accelerator. The CNN engine has a weight storage memory of 2MB, and can support 1-, 2-, 4-, and 8-bit weights (supporting networks of up to 16 million weights). The CNN weight memory is SRAM-based so that AI network updates can be made on the fly. The CNN engine also has 1.3MB of data memory. The CNN architecture is highly flexible, allowing networks to be trained in conventional toolsets like PyTorch® and TensorFlow®, then converted for execution on the MAX78002 using tools provided by Analog Devices.

In addition to the memory in the CNN engine, the MAX78002 has large on-chip system memory for the microcontroller core with 2.5MB flash and up to 384KB SRAM. Multiple high-speed and low-power communications interfaces are supported, including I^2S, MIPI® CSI-2® serial camera, parallel camera (PCIF), and SD 3.0/SDIO 3.0/eMMC 4.51 secure digital.

The device is available in a 144 CSBGA, 12mm x 12mm, 0.8mm pitch package.

Applications

- Factory Robot and Drone Navigation
- Industrial Sensors and Process Control
- Inline Quality Assurance Vision Systems
- Smart Security Cameras
- Portable Medical Diagnostics Equipment

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Coremark is a registered trademark of EEMBC.

CSI-2 and MIPI are registered trademarks of MIPI Alliance, Inc.

PyTorch is a registered trademark of Facebook, Inc.

TensorFlow is a registered trademark of Google, Inc.

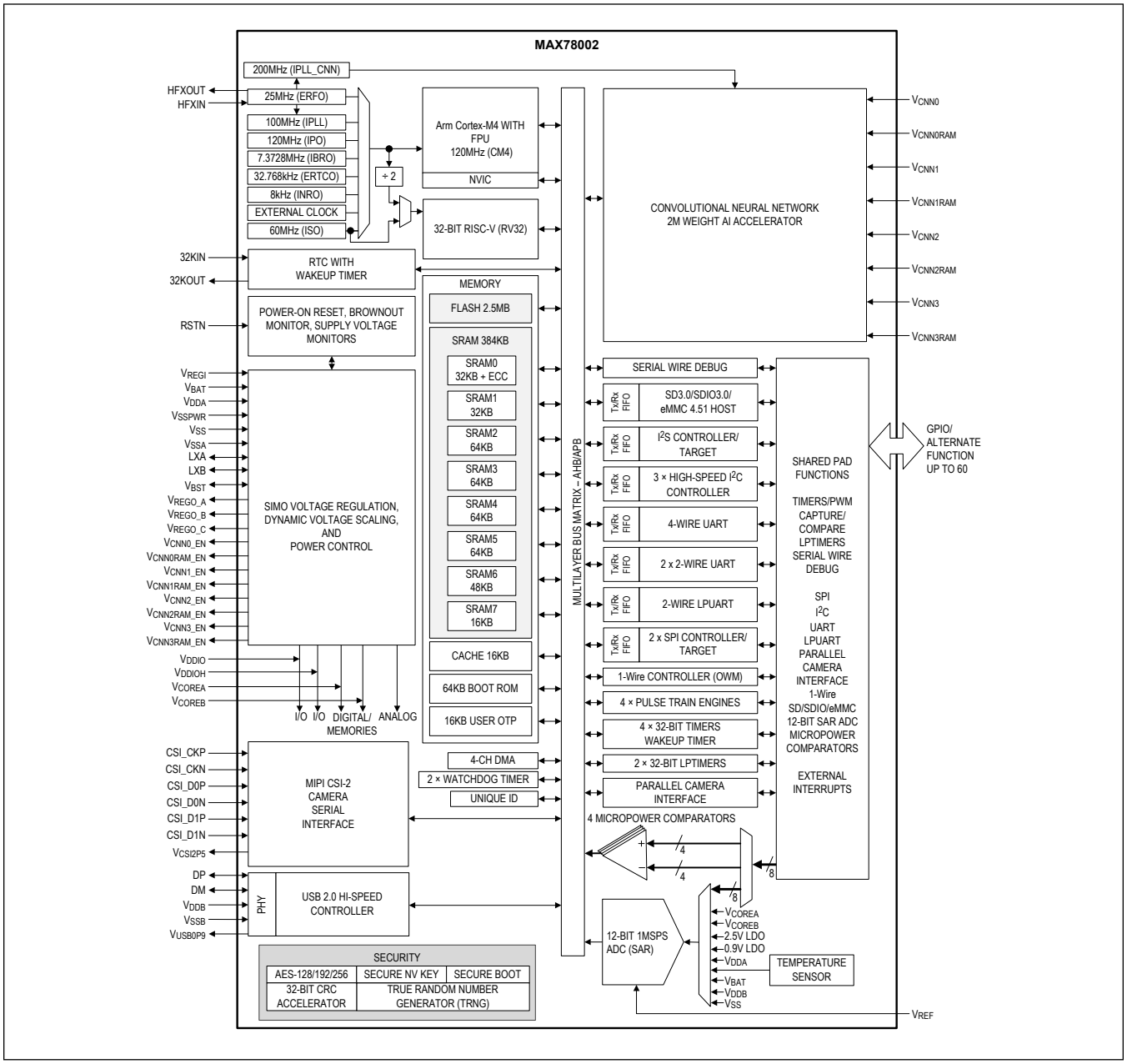
Benefits and Features

- Dual-Core, Low-Power Microcontroller
  - Arm Cortex-M4 Processor with FPU up to 120MHz
  - 2.5MB Flash, 64KB ROM, and 384KB SRAM
  - Optimized Performance with 16KB Instruction Cache
  - Optional Error Correction Code (ECC SEC-DED) for SRAM
  - 32-Bit RISC-V Coprocessor up to 60MHz
  - Up to 60 General-Purpose I/O Pins
  - MIPI Camera Serial Interface 2 (MIPI CSI-2) Controller V2.1 – Support for Two Data Lanes
  - 12-Bit Parallel Camera Interface
  - I^2S Controller/Target for Digital Audio Interface
  - Secure Digital Interface Supports SD 3.0/SDIO 3.0/eMMC 4.51
- Convolutional Neural Network (CNN) Accelerator
  - Highly Optimized for Deep CNNs
  - 2 Million 8-Bit Weight Capacity with 1-, 2-, 4-, and 8-bit Weights
  - 1.3MB CNN Data Memory
  - Programmable Input Image Size up to 2048 x 2048 Pixels
  - Programmable Network Depth up to 128 Layers
  - Programmable per Layer Network Channel Widths up to 1024 Channels
  - 1- and 2-Dimensional Convolution Processing
  - Capable of Processing VGA Images at 30fps
- Power Management for Extending Battery Life
  - Integrated Single-Inductor Multiple-Output (SIMO) Switch-Mode Power Supply (SMPS)
  - 2.85V to 3.6V Supply Voltage Range
  - Support of Optional External Auxiliary CNN Power Supply
  - Dynamic Voltage Scaling Minimizes Active Core Power Consumption
  - 23.9µA/MHz While Loop Execution at 3.3V from Cache (CM4 only)
  - Selectable SRAM Retention in Low-Power Modes with Real-Time Clock (RTC) Enabled
- Security and Integrity
  - Available Secure Boot
  - AES 128/192/256 Hardware Acceleration Engine
  - True Random Number Generator (TRNG) Seed Generator

***Ordering Information** appears at the end of the data sheet.*

19-101571; Rev 0; 6/22

Simplified Block Diagram



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V_{DDIO} ..... -0.3V to +1.89V
V_{DDIOH} ..... -0.3V to +3.6V
V_{BAT} ..... -0.3V to +3.6V
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V_{DDIOH} Combined Pins (sink) 100mA
V_{SSA} 100mA
V_{SS} 6A
V_{SSPWR} 100mA
Output Current (sink) by any GPIO Pin.....25mA
Output Current (source) by any GPIO Pin ..... -25mA
Continuous Package Power Dissipation CSBGA (multilayer board) T_A = +70°C (derate 39.37mW/°C above +70°C)(Note 1).....3149.61mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-65°C to +125°C
Soldering Temperature ..... +260°C

Note 1: Continuous Package Power Dissipation CSBGA can be exceeded with special cooling considerations.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

144 CSBGA

Package Code	X14422+2C
Outline Number	21-0163
Land Pattern Number	90-0185
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25.4°C/W
Junction to Case (θ_{JC})	5.6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Input Supply Voltage, Battery	V_{BAT}	V_{REGI}, V_{BAT}, and V_{DDIOH} must be connected together at the circuit-board level.	2.85	3.3	3.6	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage, SIMO	V_{REGI}	V_{REGI}, V_{BAT}, and V_{DDIOH} must be connected together at the circuit-board level.	2.85	3.3	3.6	V
Input Supply Voltage Core A	V_{COREA}		0.9	1.1	1.21	V
Input Supply Voltage Core B	V_{COREB}		0.9	1.1	1.21	V
Input Supply Voltage, Analog	V_{DDA}	V_{DDA} and V_{DDIO} must be connected at the circuit-board level.	1.71	1.8	1.89	V
Input Supply Voltage, GPIO	V_{DDIO}	V_{DDA} and V_{DDIO} must be connected at the circuit-board level.	1.71	1.8	1.89	V
Input Supply Voltage, GPIO (High)	V_{DDIOH}	V_{REGI}, V_{BAT}, and V_{DDIOH} must be connected together at the circuit-board level.	2.85	3.3	3.6	V
Input Supply Voltage, CNN	V_{CNNX}	Switched off by V_{CNNX_EN}. When switched on, the voltage applied must be the same as V_{COREA}.	0.99	1.1	1.21	V
Input Supply Voltage, CNN RAM	$V_{CNNXRAM}$	Switched off by $V_{CNNXRAM\_EN}$. When switched on, the voltage applied must be the same as V_{COREA}.	0.99	1.1	1.21	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{COREA}		0.76		V
		Monitors V_{COREB}	0.72	0.76		
		Monitors V_{DDA}	1.56	1.64	1.69	
		Monitors V_{DDIO}	1.56	1.64	1.69	
		Monitors V_{DDIOH}	1.56	1.64	1.69	
		Monitors V_{BAT}		2.74		
Power-On Reset Voltage	V_{POR}	Monitors V_{COREA}		0.63		V
		Monitors V_{DDA}		1.25		

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Current, ACTIVE Mode	I_{REGI_DACT}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, total current into V_{REGI} pin, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 in Active mode executing CoreMark®, RV32 in ACTIVE mode executing While(1), ECC disabled, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		32		µA/MHz
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, total current into V_{REGI} pin, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4, and RV32 in ACTIVE mode executing While(1), ECC disabled, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		27.7		
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, total current into V_{REGI} pin, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode executing While(1), RV32 in SLEEP mode, ECC disabled, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		23.9		
		Dynamic, total current into V_{REGI} pin, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, f_{SYS_CLK} = ISO; CM4 in SLEEP mode, RV32 in ACTIVE mode running from PCLK executing While(1), ECC disabled, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		20.9		
	I_{REGI_FACT}	Fixed, IPO enabled, ISO enabled, total current into V_{REGI}, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode 0MHz, RV32 in ACTIVE mode 0MHz, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		823		µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Current, SLEEP Mode	I_{REGI_DSLP}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, ECC disabled, all CNN quadrants disabled, all CNN memory disabled, standard DMA with 2 channels active; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		11.8		µA/MHz
	I_{REGI_FSLP}	Fixed, IPO enabled, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, ECC disabled, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		1.3		mA
V_{REGI} Current, LOW POWER Mode	I_{REGI_DLP}	Dynamic, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 powered off, RV32 in ACTIVE mode executing While(1), $f_{SYS\_CLK(MAX)}$ = 60MHz, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		18.9		µA/MHz
	I_{REGI_FLP}	Fixed, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, CM4 powered off, RV32 in ACTIVE mode 0MHz, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		393		µA
V_{REGI} Current, MICRO POWER Mode	I_{REGI_DMP}	Dynamic, ERTCO enabled, IBRO enabled, total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, LPUART active, f_{LPUART} = 32.768kHz, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		230		µA
V_{REGI} Current, STANDBY Mode	I_{REGI_STBY}	Fixed, total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		9.8		µA

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REGI} Current, BACKUP Mode	I_{REGI_BK}	Total current into V_{REGI} pins, V_{REGI} = 3.3V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled, all CNN quadrants disabled, all CNN memory disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	All SRAM retained		8.2		µA
			No SRAM retention		3		
			SRAM0 retained		3.5		
			SRAM0 and SRAM1 retained		4		
			SRAM0, SRAM1, and SRAM2 retained		4.8		
V_{REGI} Current, POWER DOWN Mode	I_{REGI_PDM}	Total current into V_{REGI} pins, V_{REGI} = 3.3V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			0.76		µA
V_{REGO_A} Output Voltage Range	$V_{REGO\_A\_RANGE}$	$V_{REGI} \geq V_{REGO\_A}$ + 200mV		0.5	1.8	1.85	V
V_{REGO_B} Output Voltage Range	$V_{REGO\_B\_RANGE}$	$V_{REGI} \geq V_{REGO\_B}$ + 200mV		0.5	1.0	1.25	V
V_{REGO_C} Output Voltage Range	$V_{REGO\_C\_RANGE}$	$V_{REGI} \geq V_{REGO\_C}$ + 200mV		0.5	1.0	1.25	V
V_{REGO_A} Output Current	$V_{REGO\_A\_IOUT}$	V_{REGO_A} output current			5	50	mA
V_{REGO_B} Output Current	$V_{REGO\_B\_IOUT}$	V_{REGO_B} output current			5	50	mA
V_{REGO_C} Output Current	$V_{REGO\_C\_IOUT}$	V_{REGO_C} output current			10	100	mA
V_{REGO_X} Output Current Combined	$V_{REGO\_X\_IOUT\_TOT}$	All three V_{REGO_X} outputs combined			20	100	mA
V_{REGO_X} Efficiency	$V_{REGO\_X\_EFF}$	V_{REGI} = 3.3V, V_{REGO_X} = 1.1V, load = 30mA			90		%
SLEEP Mode Resume Time	t_{SLP_ON}	Time from power mode exit to execution of first user instruction			0.74		µs
LOW-POWER Mode Resume Time	t_{LP_ON}	Time from power mode exit to execution of first user instruction			1.62		µs
MICROPOWER Mode Resume Time	t_{MP_ON}	Time from power mode exit to execution of first user instruction			17.4		µs
STANDBY Mode Resume Time	t_{STBY_ON}	Time from power mode exit to execution of first user instruction			29.6		µs
BACKUP Mode Resume Time	t_{BKU_ON}	Time from power mode exit to execution of first user instruction			1.9		ms
POWER-DOWN Mode Resume Time	t_{PDM_ON}	Time from power mode exit to execution of first user instruction			5		ms

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0		120	MHz
Internal Phase Locked Loop (IPLL)	f_{IPLL}	External 25MHz crystal connected to HFXIN and HFXOUT		100		MHz
	f_{IPLL_CNN}	External 25MHz crystal connected to HFXIN and HFXOUT		200		
Internal Primary Oscillator (IPO)	f_{IPO}			120		MHz
Internal Secondary Oscillator (ISO)	f_{ISO}			60		MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}			7.3728		MHz
Internal Nanoring Oscillator (INRO)	f_{INRO}	8kHz selected		8		kHz
		16kHz selected		16		
		30kHz selected		30		
External RTC Oscillator (ERTCO)	f_{ERTCO}	32kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 ≤ 2pF		32.768		kHz
RTC Operating Current	I_{RTC}	All power modes		0.3		µA
RTC Power-Up Time	$t_{RTC\_ ON}$			250		ms
External I^2S Clock Input Frequency	$f_{EXT\_I2S\_CLK}$	I2S_CLKEXT selected			25	MHz
External System Clock Input Frequency	f_{EXT_CLK}	EXT_CLK selected			80	MHz
External Low Power Timer1 Clock Input Frequency	$f_{EXT\_LPTMR1\_CLK}$	LPTMR1_CLK selected			8	MHz
External Low Power Timer2 Clock Input Frequency	$f_{EXT\_LPTMR2\_CLK}$	LPTMR2_CLK selected			8	MHz
CONVOLUTIONAL NEURAL NETWORK						
CNN Current Mode A	$I_{VCNN\_ALL\_A}$	CNN inactive current, CNN enabled/ inactive, CNN clocks disabled, all CNN quadrants and SRAMs powered		15.3		mA
	$I_{CNN0RAM\_A}$			0.12		
	$I_{CNN1RAM\_A}$			0.12		
	$I_{CNN2RAM\_A}$			0.12		
	$I_{CNN3RAM\_A}$			0.12		
	I_{COREA_A}			8.4		
	$I_{CNN\_TOTAL\_A}$			**24.4**		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CNN Current Mode B	$I_{VCNN\_ALL\_B}$	50MHz clock rate, CNN active current, max power network, random data and random mask configuration, CNN quadrant 0 enabled, CNN quadrant 1/2/3 disabled, all CNN quadrants and SRAMs powered		59.5		mA
	$I_{CNN0RAM\_B}$			11.9		
	$I_{CNN1RAM\_B}$			0.13		
	$I_{CNN2RAM\_B}$			0.13		
	$I_{CNN3RAM\_B}$			0.13		
	I_{COREA_B}			4.5		
	$I_{CNN\_TOTAL\_B}$			**76.2**		
CNN Current Mode C	$I_{VCNN\_ALL\_C}$	50MHz clock rate, CNN active current, all CNN quadrants and SRAMs powered, unet_v5 functional test		89.1		mA
	$I_{CNN0RAM\_C}$			7.5		
	$I_{CNN1RAM\_C}$			4.9		
	$I_{CNN2RAM\_C}$			4.5		
	$I_{CNN3RAM\_C}$			4.5		
	I_{COREA_C}			4.5		
	$I_{CNN\_TOTAL\_C}$			**115**		
CNN Current Mode D	$I_{VCNN\_ALL\_D}$	50MHz clock rate, CNN active current, max power network, random data and random mask configuration, all CNN quadrants and SRAMs powered		187		mA
	$I_{CNN0RAM\_D}$			13		
	$I_{CNN1RAM\_D}$			13		
	$I_{CNN2RAM\_D}$			13		
	$I_{CNN3RAM\_D}$			13		
	I_{COREA_D}			4.5		
	$I_{CNN\_TOTAL\_D}$			**243**		
CNN Current Mode E	$I_{VCNN\_ALL\_E}$	50MHz clock rate, CNN active current, max power network, data, mask configuration, all CNN quadrants and SRAMs powered		254		mA
	$I_{CNN0RAM\_E}$			13.8		
	$I_{CNN1RAM\_E}$			13.9		
	$I_{CNN2RAM\_E}$			13.8		
	$I_{CNN3RAM\_E}$			13.8		
	I_{COREA_E}			4.5		
	$I_{CNN\_TOTAL\_E}$			**313**		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CNN Current Mode F	$I_{VCNN\_ALL\_F}$	200MHz clock rate, CNN active current, max power network, random data, and random mask configuration, CNN quadrant 0 enabled, CNN quadrant 1/2/3 disabled, all CNN quadrants and SRAMs powered		117		mA
	$I_{CNN0RAM\_F}$			24.5		
	$I_{CNN1RAM\_F}$			0.132		
	$I_{CNN2RAM\_F}$			0.131		
	$I_{CNN3RAM\_F}$			0.128		
	I_{COREA_F}			7.9		
	$I_{CNN\_TOTAL\_F}$			**150**		
CNN Current Mode G	$I_{VCNN\_ALL\_G}$	200MHz clock rate, CNN active current, all CNN quadrants and SRAMs powered, unet_v5 functional test		242		mA
	$I_{CNN0RAM\_G}$			16		
	$I_{CNN1RAM\_G}$			10.4		
	$I_{CNN2RAM\_G}$			9.5		
	$I_{CNN3RAM\_G}$			9.5		
	I_{COREA_G}			7.9		
	$I_{CNN\_TOTAL\_G}$			**295**		
CNN Current Mode H	$I_{VCNN\_ALL\_H}$	200MHz clock rate, CNN active current, max processing configuration, max power network, random data, and random mask configuration, all CNN quadrants and SRAMs powered		1060		mA
	$I_{CNN0RAM\_H}$			94		
	$I_{CNN1RAM\_H}$			94		
	$I_{CNN2RAM\_H}$			94		
	$I_{CNN3RAM\_H}$			94		
	I_{COREA_H}			8.2		
	$HI_{CNN\_TOTAL\_7}$			**1440**		
CNN Current Mode J	$I_{VCNN\_ALL\_J}$	200MHz clock rate, CNN active current, max processing configuration, max power network, data, mask configuration, all CNN quadrants and SRAMs powered		1450		mA
	$I_{CNN0RAM\_J}$			99		
	$I_{CNN1RAM\_J}$			99		
	$I_{CNN2RAM\_J}$			99		
	$I_{CNN3RAM\_J}$			99		
	I_{COREA_J}			8.4		
	$I_{CNN\_TOTAL\_J}$			**1852**		
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIOs Except P3.0 and P3.1	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply; P3.0 and P3.1 can only use V_{DDIOH} as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIOs	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Low Voltage for RSTN	V_{IL_RSTN}				0.5 x V_{DDIOH}		V
Input High Voltage for All GPIOs Except P3.0 and P3.1	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply; P3.0 and P3.1 can only use V_{DDIOH} as I/O supply		0.7 × V_{DDIO}			V
Input High Voltage for All GPIOs	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply		0.7 × V_{DDIOH}			V
Input High Voltage for RSTN	V_{IH_RSTN}				0.5 x V_{DDIOH}		V
Output Low Voltage for All GPIOs Except P3.0 and P3.1	V_{OL_VDDIO}	P3.0 and P3.1 can only use V_{DDIOH} as I/O supply	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Output Low Voltage for All GPIOs	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA			0.2	0.4	V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA			0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA			0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA			0.2	0.4	
Combined I_{OL}, All GPIOs	I_{OL_TOTAL}					48	mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage for All GPIOs Except P3.0 and P3.1	V_{OH_VDDIO}	P3.0 and P3.1 can only use V_{DDIOH} as I/O supply	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIOs Except P3.0 and P3.1	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA		V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA		V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -4mA		V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA		V_{DDIOH} - 0.4			
Output High Voltage for P3.0 and P3.1	V_{OH_VDDIOH}	V_{DDIOH} = 2.85V, GPIOn_DS_SEL[1:0] fixed at 00, I_{OL} = -1mA		V_{DDIOH} - 0.4			V
Combined I_{OH}, All GPIOs	I_{OH_TOTAL}					-48	mA
Input Hysteresis (Schmitt)	V_{HYS}				300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pull-up disabled		-200		+200	nA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pull-down disabled	-1000		+1000	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = 1.71V, V_{DDIOH} = 2.85V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pull-up Resistor RSTN	R_{PU_R}	Pull-up to V_{DDIOH}		25		kΩ
Input Pull-up/Pull-down Resistor for All GPIO	R_{PU1}	Normal resistance, P1M = 0		25		kΩ
	R_{PU2}	Highest resistance, P1M = 1		1		MΩ
12-BIT SAR ADC						
Resolution				12		bits
Effective Number of Bits	ENOB	ADC_CLKCTRL.clksel = 11; AINx input pk--pk = V_{REF} - 10mV		10		bits
External Reference Voltage	V_{REF}	$V_{REF} \le V_{DDIOH}$	2.048		V_{DDIOH}	V
Internal Reference Voltage	V_{INT_REF}	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 0		1.25		V
	V_{INT_REF}	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 1		2.048		
ADC Clock Rate	f_{ACLK}			1		MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[7:0], ADC_DATA.chan = [7:0], MCR_ADCCFG2.chX = 00	V_{SSA} + 0.05		V_{REF}	V
		AIN[7:0], ADC_DATA.chan = [7:0], MCR_ADCCFG2.chX = 01	V_{SSA} + 0.05		MIN(2 x V_{REF},V_{DDIOH})	
		AIN[7:0], ADC_DATA.chan = [7:0], MCR_ADCCFG2.chX = 10	V_{SSA} + 0.05		MIN(2 x V_{REF},V_{DDIOH})	
Input Impedance	R_{AIN}	MCR_ADCCFG2.chX = 01		5		kΩ
		MCR_ADCCFG2.chX = 10		50		
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		2		pF
		Dynamically switched capacitance		1.2		pF
Integral Nonlinearity	INL			±1.5		LSb
Differential Nonlinearity	DNL			±0.75		LSb
Offset Error	V_{OS}	Chopping disabled		±9		LSb
		Chopping enabled		±0.2		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, ADC_CLKCTRL.clksel = 11, ADC_CLKCTRL.clkdiv = 100	MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.ref_sel = 0, V_{BAT} = 3.3V		361		µA
			MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.ref_sel = 1, V_{BAT} = 3.3V		361		
			MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 0, V_{BAT} = 3.3V		229		
			MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.ref_sel = 1, V_{BAT} = 3.3V		229		
			MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.ref_sel = 0, V_{BAT} = 3.3V		162		
			MCR_ADCCFG0.ext_ref = 0, MCR_ADCCFG0.ref_sel = 1, V_{BAT} = 3.3V		162		
ADC Sample Rate	f_{ADC}	ADC_CLKCTRL.clkdiv = 0bX00				1	Msps
		ADC_CLKCTRL.clkdiv = 0bX01				0.625	
		ADC_CLKCTRL.clkdiv = 0bX10				0.125	
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to ADC_STATUS.ready = 1				500	µs
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected			1.5		nA
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method			± 45		ppm
COMPARATORS							
Input Offset Voltage	V_{OFFSET}				±7		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00			22		mV
		AINCOMPHYST[1:0] = 01			50		
		AINCOMPHYST[1:0] = 10			2		
		AINCOMPHYST[1:0] = 11			7		
Input Voltage Range	V_{IN_CMP}	Common-mode range		0.6		1.35	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB						
USB Transceiver Supply Voltage	V_{DDB}		3.0	3.3	3.6	V
Pin Capacitance (DP, DM)	C_{IN_USB}	Pin to V_{SSB}		8		pF
Driver Output Resistance	R_{DRV}	Steady state drive		44 ±10%		Ω
USB / FULL SPEED						
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}		2.1			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}				0.5	V
Output High Voltage (DP, DM)	V_{OH_USB}	R_L = 1.5kΩ from DP and DM to V_{SSB}, I_{OH} = -4mA	2.8		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	R_L = 1.5kΩ from DP to V_{DDB}, I_{OL} = 4mA	V_{SS}		0.3	V
Differential Input Sensitivity	V_{DI}	|DP to DM|	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Transition Time (Rise/ Fall) DP, DM	t_{RF}	C_L = 50pF	4		20	ns
Pull-up Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	kΩ
USB / HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low-Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High-Level Output Voltage	V_{HSOH}			400 ±40		mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ±200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ±200		mV

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, f_{FLC_CLK} = 1MHz		42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +105°C	10			years
MIPI CSI-2						
Data Rate per CSI-2 Lane					600	Mbps
Frequency (CSI_CKP, CSI_CKN)	f_{CK}				300	MHz
MIPI CSI-2 / HIGH-SPEED DC SPECIFICATIONS						
DC Common-Mode Voltage (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	V_{CMDC}		70		330	mV
Differential Input High Threshold (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	V_{DIHT}			40		mV
Differential Input Low Threshold (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	V_{DILT}			-40		mV
Differential Input Impedance (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	Z_{DI}		80	100	120	Ω
MIPI CSI-2 / HIGH-SPEED AC SPECIFICATIONS						
Data to Clock Setup Time (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	t_{SETUP}		$0.15 \times \frac{1}{f_{CK}}$			ns
Data to Clock Hold Time (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	t_{HOLD}		$0.15 \times \frac{1}{f_{CK}}$			ns

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MIPI CSI-2 / LOW-POWER DC SPECIFICATIONS						
Input High Voltage (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	V_{IH}		850			mV
Input Low Threshold (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	V_{IL}				550	mV
Input Hysteresis (CSI_D0P, CSI_D0N, CSI_D1P, CSI_D1N, CSI_CKP, CSI_CKN)	V_{HYS}		25			mV

Electrical Characteristics—I^2C

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD-MODE						
Output Fall Time	t_{OF}	Standard-mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs

Electrical Characteristics—I²C (continued)

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST-MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST-MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns

Electrical Characteristics—I²C (continued)

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—SD/SDIO/SDHC/MMC

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency in Data Transfer Mode	f_{SDHC_CLK}		0		f_{PCLK}	MHz
Clock Period	t_{CLK}			$1/f_{SDHC\_CLK}$		ns
Clock Low Time	t_{WCL}			7		ns
Clock High Time	t_{WCH}			7		ns
Input Setup Time	t_{ISU}			5		ns
Input Hold Time	t_{IHLD}			1		ns
Output Valid Time	t_{OVLD}			5		ns
Output Hold Time	t_{OHLD}			6		ns

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER MODE						
SPI Controller Operating Frequency for SPI0	f_{MCK0}	f_{SYS_CLK} = 120MHz, $f_{MCK0(MAX)} = f_{SYS\_CLK}/2$			60	MHz
SPI Controller Operating Frequency for SPI1	f_{MCK1}	f_{SYS_CLK} = 120MHz, $f_{MCK1(MAX)} = f_{SYS\_CLK}/4$			30	MHz
SPI Controller SCK Period	t_{MCKX}			$1/f_{MCKX}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCKX}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCKX}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCKX}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCKX}/2$		ns

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCKX}/2$		ns
TARGET MODE						
SPI Target Operating Frequency	f_{SCK}				60	MHz
SPI Target SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			3		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			3		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			10		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		ns
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I^2S

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TARGET						
Bit Clock Frequency	f_{BCLKS}				25	MHz
Bit Clock Period	t_{BCLKS}		$1/f_{BCLKS}$			µs
BCLK High Time	$t_{WBCLKHS}$			$0.5 \times \frac{1}{f_{BCLKS}}$		µs
BCLK Low Time	$t_{WBCLKLS}$			$0.5 \times \frac{1}{f_{BCLKS}}$		µs
Setup Time for LRCLK	t_{LRCLK_BLCKS}			20		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOS}			20		ns
Setup Time for SD (Input)	t_{SU_SDIS}			10		ns
Hold Time SD (Input)	t_{HD_SDIS}			10		ns

Electrical Characteristics—I²S (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER						
Bit Clock Frequency	f_{BCLKM}	Source only from I2S_EXTCLK (P0.14 Alternate Function 2)			80	MHz
Bit Clock Period	t_{BCLKM}		$1/f_{BCLKM}$			µs
BCLK High Time	$t_{WBCLKHM}$			$0.5 \times \frac{1}{f_{BCLKM}}$		µs
BCLK Low Time	$t_{WBCLKLM}$			$0.5 \times \frac{1}{f_{BCLKM}}$		µs
Delay Time BCLK to LRCLK Valid	t_{BLCK_LRCLKM}			20		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOM}			20		ns
Setup Time for SD (Input)	t_{SU_SDIM}			10		ns
Hold Time SD (Input)	t_{HD_SDIM}			10		ns

Electrical Characteristics—PCIF

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCIF						
PCIF Operating Frequency	f_{CLK}				10	MHz
PCIF Clock Period	t_{CLK}			$1/f_{CLK}$		ns
PCIF_PCLK Output Pulse-Width High/Low	t_{WCH}, t_{WCL}		$t_{CLK}/2$			ns
PCIF_VSYNC, PCIF_HSYNC Setup Time	t_{SSU}			5		ns
PCIF_VSYNC, PCIF_HSYNC Hold Time	t_{SHLD}			5		ns
PCIF_D0-PCIF_D11 Setup TIme	t_{DSU}			5		ns
PCIF_D0-PCIF_D11 Hold Time	t_{DHLD}			5		ns

Electrical Characteristics—1-Wire Controller

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		

Electrical Characteristics—1-Wire Controller (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

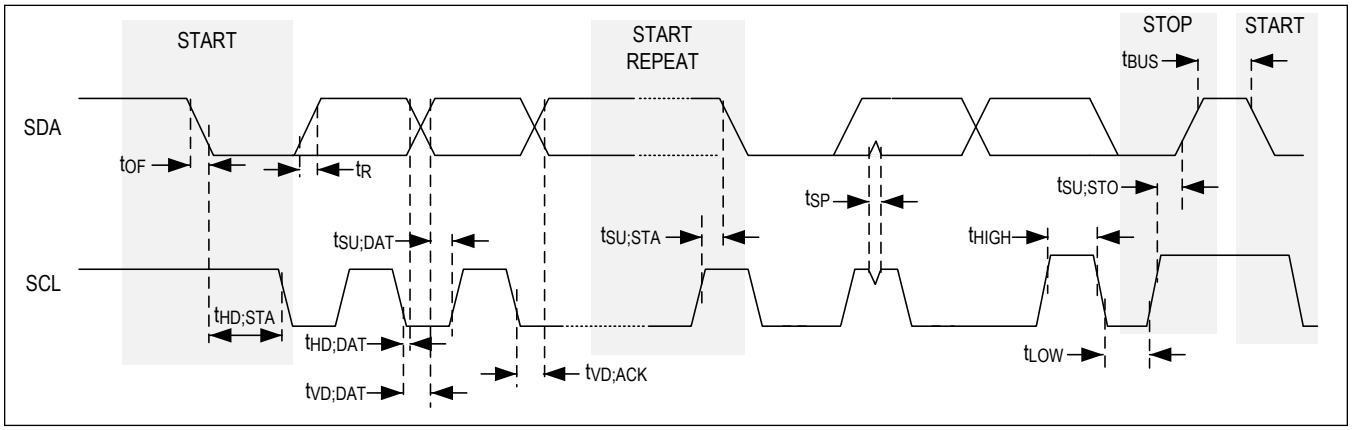

Figure 1. I^2C Timing Diagram

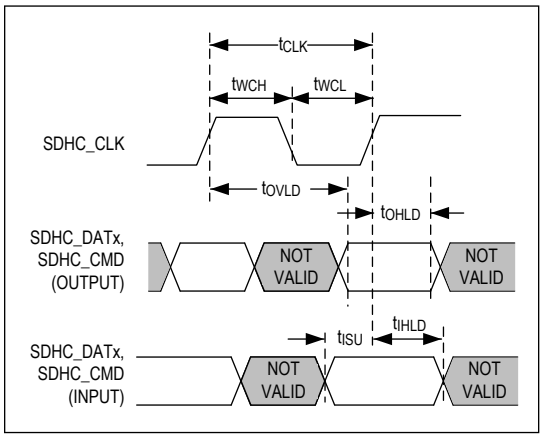

Figure 2. SD/SDIO/SDHC/MMC Timing Diagram

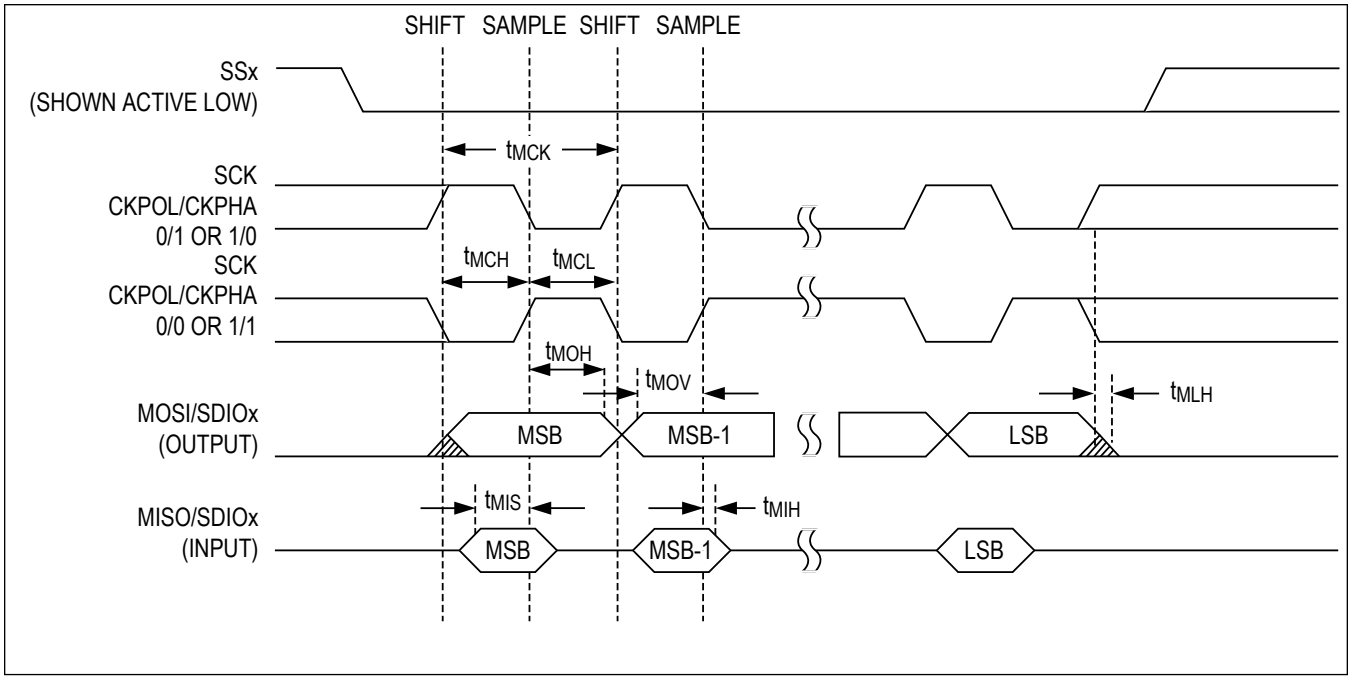

Figure 3. SPI Controller Mode Timing Diagram

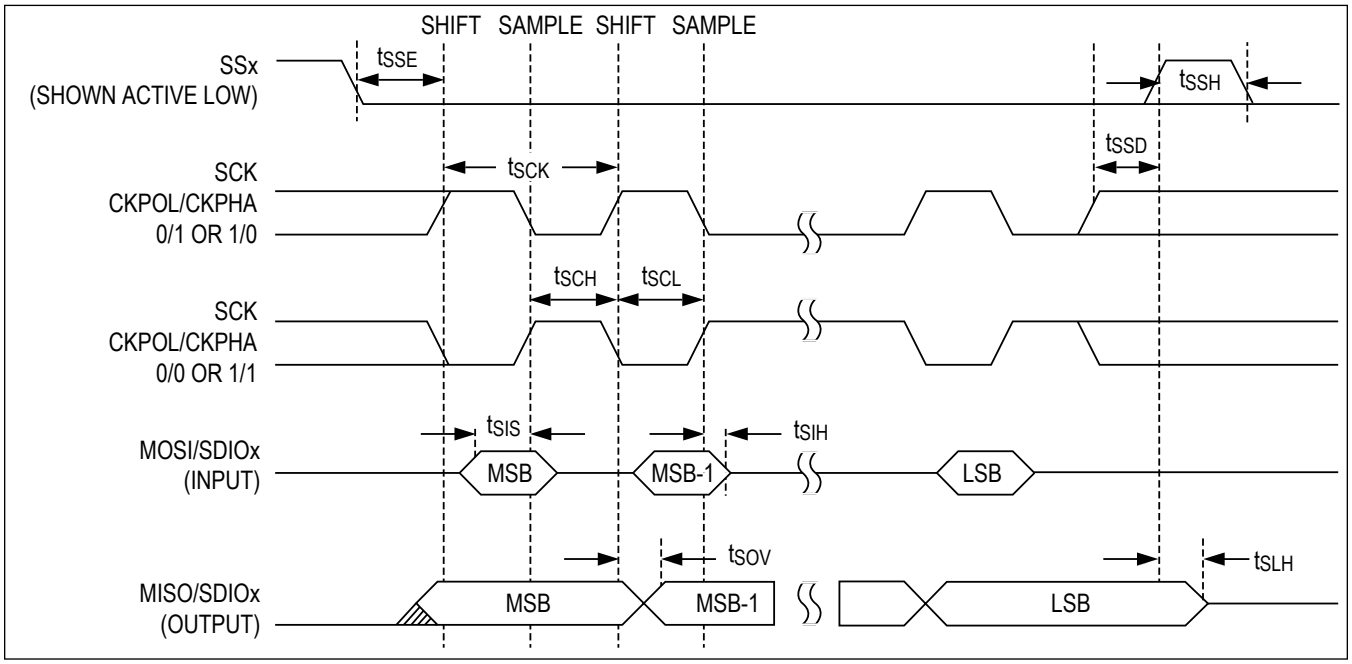

Figure 4. SPI Target Mode Timing Diagram

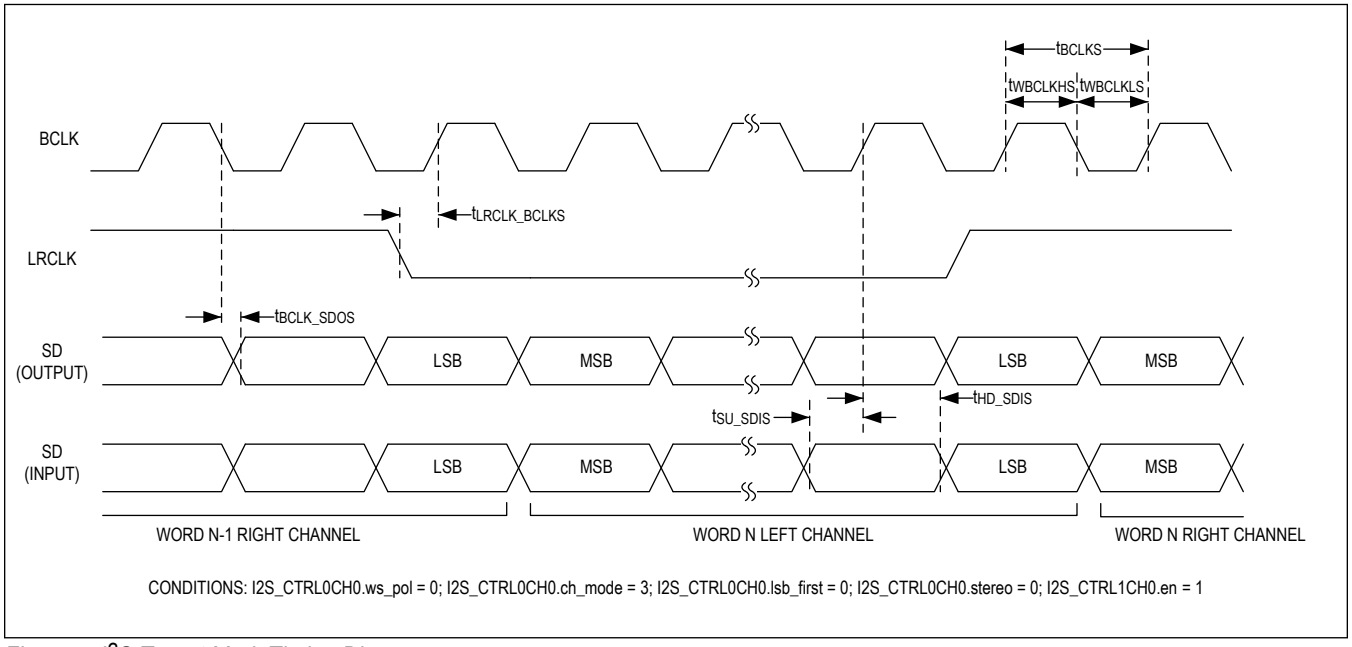

Figure 5. I^2S Target ModeTiming Diagram

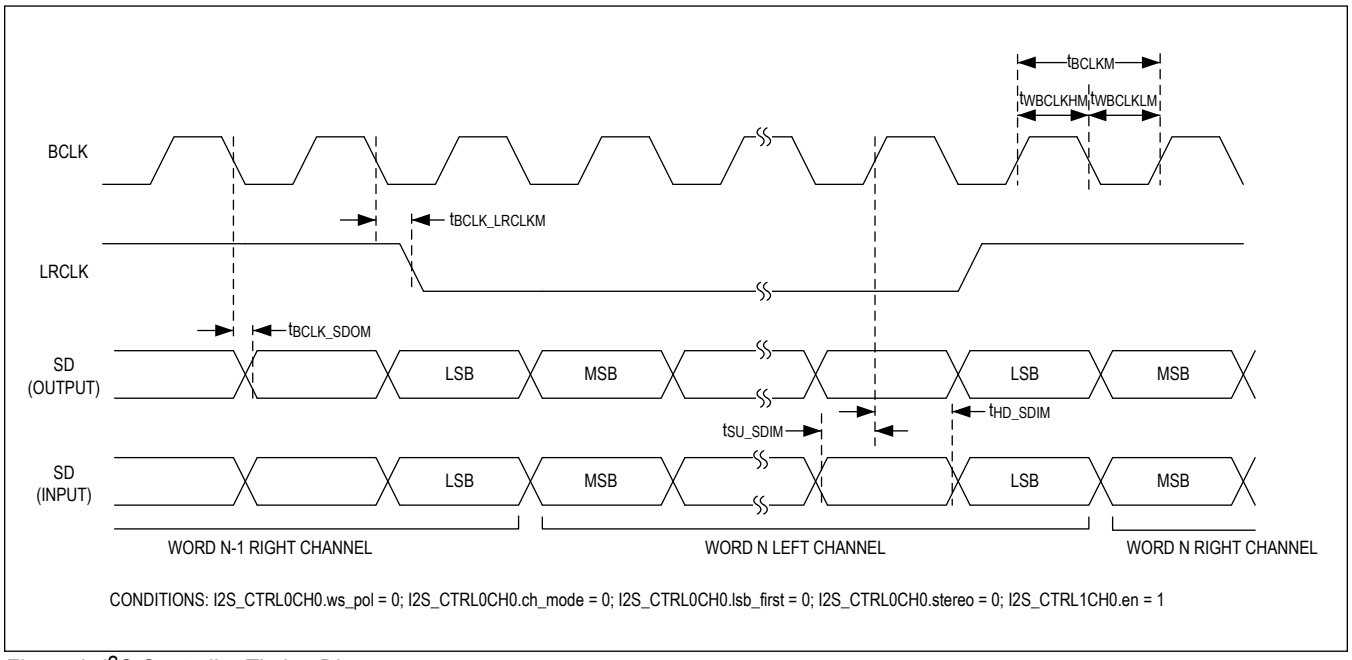

Figure 6. I²S Controller Timing Diagram

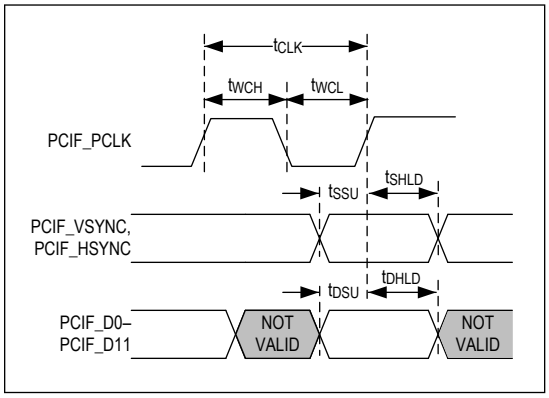

Figure 7. Parallel Camera Interface Timing Diagram

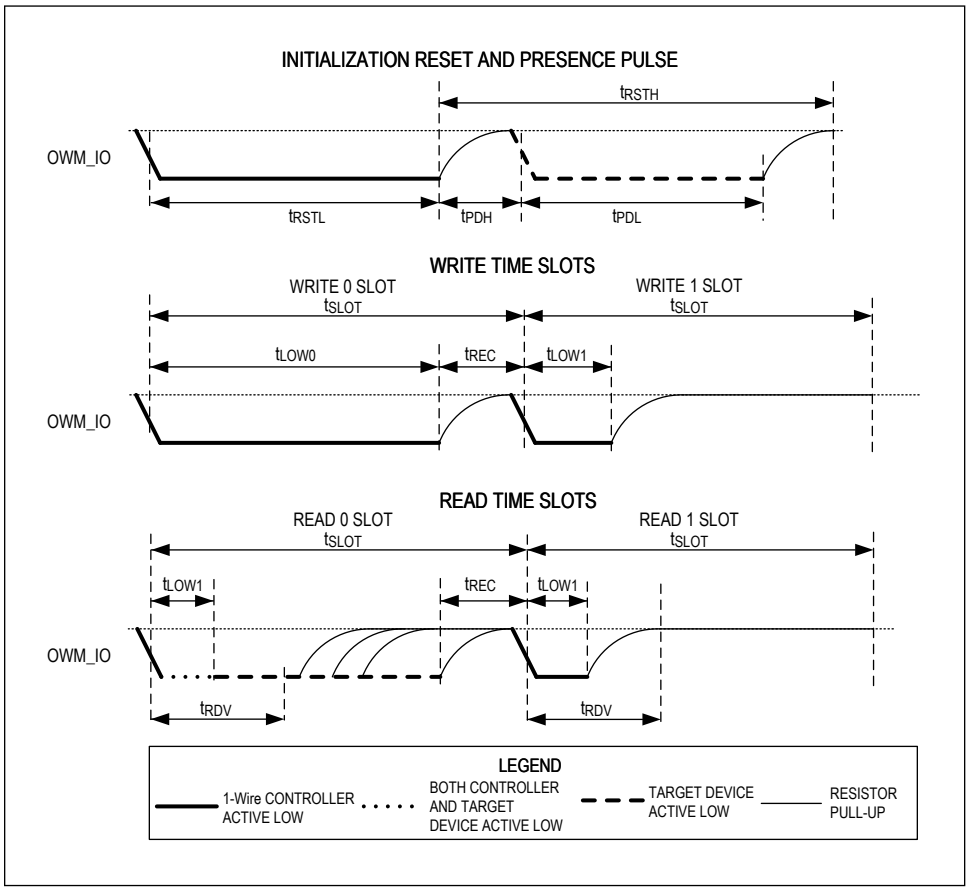

Figure 8. 1-Wire Controller Data Timing Diagram

Pin Configuration

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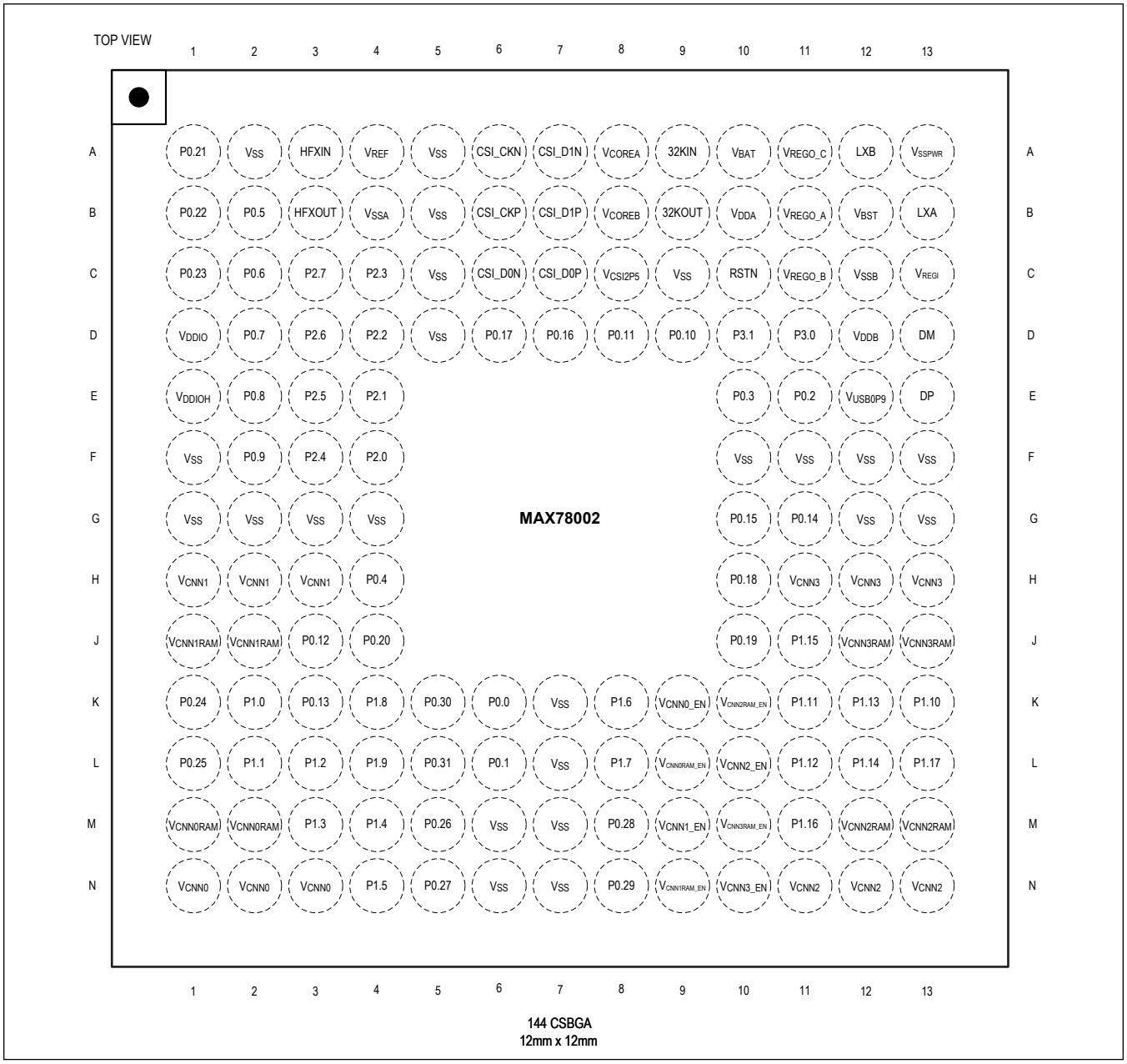

Pin Description

PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
POWER (See the Applications Information section for bypass capacitor recommendations.)					
A10	V_{BAT}	—	—	—	Battery Power Supply. Bypass device pin A10 with a 1µF capacitor placed as close as possible to this pin and the V_{SSPWR} pin. This pin must be connected to V_{REGI} and V_{DDIOH} at the circuit board level.
C13	V_{REGI}	—	—	—	Battery Power Supply for the SIMO Switch-Mode Power Supply (SMPS). Bypass this pin with 2 x 47µF capacitors placed as close as possible to this pin and the V_{SSPWR} pin. This pin must be connected to V_{BAT} and V_{DDIOH}. If the power to the device is cycled, the voltage applied to this pin must reach V_{REGI_POR}.
B10	V_{DDA}	—	—	—	1.8V Analog Power Supply. Bypass this pin with a 1µF capacitor placed as close as possible to this pin and V_{SSA}. This device pin must be connected to V_{DDIO}.
D12	V_{DDB}	—	—	—	USB Transceiver Supply Voltage. Bypass this pin to V_{SSB} with a 1.0µF capacitor as close as possible to the package.
A4	V_{REF}	—	—	—	ADC External Reference Input. Bypass this pin with a 1µF capacitor placed as close as possible to this pin and V_{SSA} as possible. This is the reference input for the analog-to-digital converter (ADC). If the external reference is not used, tie this pin to V_{SSA} through a 500Ω resistor.
A8	V_{COREA}	—	—	—	Digital Core Supply Voltage A. Bypass this pin to V_{SS} with a 1µF capacitor placed as close to this pin as possible.
B8	V_{COREB}	—	—	—	Digital Core Supply Voltage B. Bypass this pin to V_{SS} with a 1µF capacitor placed as close to this pin as possible.
B12	V_{BST}	—	—	—	Boosted Supply Voltage for the Gate Drive of High-Side Switches. Bypass V_{BST} to LXB with a 3.3nF capacitor.
B11	V_{REGO_A}	—	—	—	Buck Converter A Voltage Output. Bypass this pin with a 22µF capacitor to V_{SS} placed as close as possible to this pin.
C11	V_{REGO_B}	—	—	—	Buck Converter B Voltage Output. Bypass this pin with a 22µF capacitor to V_{SS} placed as close as possible to this pin.
A11	V_{REGO_C}	—	—	—	Buck Converter C Voltage Output. Bypass this pin with a 22µF capacitor to V_{SS} placed as close as possible to this pin.
D1	V_{DDIO}	—	—	—	GPIO Supply Voltage. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
E1	V_{DDIOH}	—	—	—	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package. This device pin must be connected to V_{REGI} and V_{BAT}.
E12	V_{USB0P9}	—	—	—	Bypass with 1µF capacitor to V_{SSB}. Do not connect this device pin to any other external circuitry.
C8	V_{CSI2P5}	—	—	—	Bypass with 1µF capacitor to V_{SS}. Do not connect this device pin to any other external circuitry.
F1, G1, A2, G2, G3, G4, A5, B5, C5, D5, M6, N6, K7, L7, M7, N7, C9, F10, F11, F12, G12, F13, G13	V_{SS}	—	—	—	Digital Ground.
B4	V_{SSA}	—	—	—	Analog Ground. This pin is the return path for V_{REF} and V_{DDA}.
A13	V_{SSPWR}	—	—	—	Ground for the SIMO Switch-Mode Power Supply (SMPS). This device pin is the return path for the V_{REG}.
C12	V_{SSB}	—	—	—	USB Transceiver Ground.
B13	LXA	—	—	—	Switching Inductor Input A. Connect a 2.2µH inductor between LXA and LXB.
A12	LXB	—	—	—	Switching Inductor Input B. Connect a 2.2µH inductor between LXA and LXB.
N1, N2, N3	V_{CNN0}	—	—	—	Voltage Supply for CNN x16 Processor Quadrant 0. Bypass this pin with 3 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
H1, H2, H3	V_{CNN1}	—	—	—	Voltage Supply for CNN x16 Processor Quadrant 1. Bypass this pin with 3 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
N11, N12, N13	V_{CNN2}	—	—	—	Voltage Supply for CNN x16 Processor Quadrant 2. Bypass this pin with 3 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
H11, H12, H13	V_{CNN3}	—	—	—	Voltage Supply for CNN x16 Processor Quadrant 3. Bypass this pin with 3 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
M1, M2	$V_{CNN0RAM}$	—	—	—	Voltage Supply for the RAM for the CNN x16 Processor Quadrant 0. Bypass this pin with 2 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
J1, J2	$V_{CNN1RAM}$	—	—	—	Voltage Supply for the RAM for the CNN x16 Processor Quadrant 1. Bypass this pin with 2 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
M12, M13	$V_{CNN2RAM}$	—	—	—	Voltage Supply for the RAM for the CNN x16 Processor Quadrant 2. Bypass this pin with 2 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
J12, J13	$V_{CNN3RAM}$	—	—	—	Voltage Supply for the RAM for the CNN x16 Processor Quadrant 3. Bypass this pin with 2 x 1µF capacitors as close to this pin as possible and a 22µF capacitor as close as possible to the package.
K9	V_{CNN0_EN}	—	—	—	Enable Output for the Voltage Supply for CNN x16 Processor Quadrant 0.
M9	V_{CNN1_EN}	—	—	—	Enable Output for the Voltage Supply for CNN x16 Processor Quadrant 1.
L10	V_{CNN2_EN}	—	—	—	Enable Output for the Voltage Supply for CNN x16 Processor Quadrant 2.
N10	V_{CNN3_EN}	—	—	—	Enable Output for the Voltage Supply for CNN x16 Processor Quadrant 3.
L9	$V_{CNN0RAM\_EN}$	—	—	—	Enable Output for the Voltage Supply for the RAM for the CNN x16 Processor Quadrant 0.
N9	$V_{CNN1RAM\_EN}$	—	—	—	Enable Output for the Voltage Supply for the RAM for the CNN x16 Processor Quadrant 1.
K10	$V_{CNN2RAM\_EN}$	—	—	—	Enable Output for the Voltage Supply for the RAM for the CNN x16 Processor Quadrant 2.
M10	$V_{CNN3RAM\_EN}$	—	—	—	Enable Output for the Voltage Supply for the RAM for the CNN x16 Processor Quadrant 3.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
RESET AND CONTROL					
C10	RSTN	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for RTC circuitry) and begins execution. This pin has an internal pull-up to the V_{DDIOH} supply.
CLOCK					
B9	32KOUT	—	—	—	32kHz Crystal Oscillator Output.
A9	32KIN	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
A3	HFXIN	—	—	—	25MHz Crystal Oscillator Input. Connect a 25MHz crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
B3	HFXOUT	—	—	—	25MHz Crystal Oscillator Output.
GPIO AND ALTERNATE FUNCTION (See the Applications Information section for GPIO and Alternate Function Matrices.)					
K6	P0.0	P0.0	UART0A_RX	—	UART0 Receive Port Map A. See *Bootloader Activation* for details on this pin's usage and suggested pull-up.
L6	P0.1	P0.1	UART0A_TX	—	UART0 Transmit Port Map A.
E11	P0.2	P0.2	TMR0A__IOA	UART0B_CTS	Timer0 I/O 32 Bits or Lower 16 Bits Port Map A; UART0 Clear to Send Port Map B.
E10	P0.3	P0.3/EXT_CLK	TMR0A_IOB	UART0B_RTS	External Clock for Use as SYS_OSC/Timer0 I/O Upper 16 Bits Port Map A; UART0 Request to Send Port Map B.
H4	P0.4	P0.4	SPI0A_SS0	TMR0B_IOAN	SPI0 Port Map A Target Select 0; Timer0 Inverted Output Port Map B.
B2	P0.5	P0.5	SPI0A_MOSI	TMR0B_IOBN	SPI0 Port Map A Controller-Out Target-In Serial Data 0; Timer0 Inverted Output Upper 16 Bits Port Map B.
C2	P0.6	P0.6	SPI0A_MISO	OWM_IO	SPI0 Port Map A Controller-In Target-Out Serial Data 1; 1-Wire Controller Data I/O.
D2	P0.7	P0.7	SPI0A_SCK	OWM_PE	SPI0 Port Map A Clock; 1-Wire Controller Pull-up Enable Output.
E2	P0.8	P0.8	SPI0A_SDIO2	TMR0B_IOA	SPI0 Port Map A Data 2 I/O; Timer0 I/O 32 Bits or Lower 16 Bits Port Map B.
F2	P0.9	P0.9	SPI0A_SDIO3	TMR0B_IOB	SPI0 Port Map A Data 3 I/O; Timer0 I/O Upper 16 Bits Port Map B.
D9	P0.10	P0.10	I2C0A_SCL	SPI0_SS2	I2C0 Port Map A Clock; SPI0 Target Select 2.
D8	P0.11	P0.11	I2C0A_SDA	SPI0_SS1	I2C0 Port Map A Serial Data; SPI0 Target Select 1.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
J3	P0.12	P0.12	UART1A_RX	TMR1B_IOAN	UART1 Receive Port Map A; Timer1 Inverted Output Port Map B.
K3	P0.13	P0.13	UART1A_TX	TMR1B_IOBN	UART1 Transmit Port Map A; Timer1 Inverted Output Upper 16 Bits Port Map B.
G11	P0.14	P0.14	TMR1A_IOA	I2S_CLKEXT	Timer1 I/O 32 Bits or Lower 16 Bits Port Map A; I^2S External Clock Input.
G10	P0.15	P0.15	TMR1A_IOB	PCIF_VSYNC	Timer1 I/O Upper 16 Bits Port Map A; Parallel Camera Interface Vertical Sync.
D7	P0.16	P0.16	I2C1A_SCL	PT2	I2C1 Port Map A Clock; Pulse Train 2.
D6	P0.17	P0.17	I2C1A_SDA	PT3	I2C1 Port Map A Serial Data; Pulse Train 3.
H10	P0.18	P0.18	PT0	OWM_IO	Pulse Train 0; 1-Wire Controller Data I/O.
J10	P0.19	P0.19	PT1	OWM_PE	Pulse Train 1; 1-Wire Controller Pull-up Enable Output.
J4	P0.20	P0.20	SPI1A_SS0	PCIF_D0	SPI1 Port Map A Target Select 0; Parallel Camera Interface Data 0.
A1	P0.21	P0.21	SPI1A_MOSI	PCIF_D1	SPI1 Port Map A Controller-Out Target-In Serial Data 0; Parallel Camera Interface Data 1.
B1	P0.22	P0.22	SPI1A_MISO	PCIF_D2	SPI1 Port Map A Controller-In Target-Out Serial Data 1; Parallel Camera Interface Data 2.
C1	P0.23	P0.23	SPI1A_SCK	PCIF_D3	SPI1 Port Map A Clock; Parallel Camera Interface Data 3.
K1	P0.24	P0.24	SPI1A_SDIO2	PCIF_D4	SPI1 Port Map A Data 2; Parallel Camera Interface Data 4.
L1	P0.25	P0.25	SPI1A_SDIO3	PCIF_D5	SPI1 Port Map A Data 3; Parallel Camera Interface Data 5.
M5	P0.26	P0.26	TMR2A_IOA	PCIF_D6	Timer2 I/O 32 Bits or Lower 16 Bits Port Map A; Parallel Camera Interface Data 6.
N5	P0.27	P0.27/ USB_EXTCLK	TMR2A_IOB	PCIF_D7	USB External Clock/Timer2 I/O Upper 16 Bits Port Map A; Parallel Camera Interface Data 7.
M8	P0.28	P0.28/SWDIO	—	—	Serial Wire Debug Data I/O. Following any reset, this device pin defaults to AF1 SWDIO.
N8	P0.29	P0.29/SWDCLK	—	—	Serial Wire Debug Clock. Following any reset, this device pin defaults to AF1 SWDCLK. See *Bootloader Activation* for details on this pin's usage and suggested pullup.
K5	P0.30	P0.30	I2C2A_SCL	PCIF_D8	I2C2 Port Map A Clock; Parallel Camera Interface Data 8.
L5	P0.31	P0.31	I2C2A_SDA	PCIF_D9	I2C2 Port Map A Serial Data; Parallel Camera Interface Data 9.
K2	P1.0	P1.0	UART2A_RX	RV_TCK	UART2 Receive Port Map A; 32-bit RISC-V Test Port Clock.
L2	P1.1	P1.1	UART2A_TX	RV_TMS	UART2 Transmit Port Map A; 32-bit RISC-V Test Port Select.
L3	P1.2	P1.2	I2S0A_SCK	RV_TDI	I2S0 Port Map A Bit Clock; 32-bit RISC-V Test Port Data Input.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
M3	P1.3	P1.3	I2S0A_WS	RV_TDO	I2S0 Port Map A Left/Right Clock; 32-bit RISC-V Test Port Data Output.
M4	P1.4	P1.4	I2S0A_SDI	TMR3B_IOA	I2S0 Port Map A Serial Data Input; Timer3 I/O 32 Bits or Lower 16 Bits Port Map B.
N4	P1.5	P1.5	I2S0A_SDO	TMR3B_IOB	I2S0 Port Map A Serial Data Output; Timer3 I/O Upper 16 Bits Port Map B.
K8	P1.6	P1.6	TMR3A_IOA	PCIF_D10	Timer3 I/O 32 Bits or Lower 16 Bits Port Map A; Parallel Camera Interface Data 10.
L8	P1.7	P1.7	TMR3A_IOB	PCIF_D11	Timer3 I/O Upper 16 Bits Port Map A; Parallel Camera Interface Data 11.
K4	P1.8	P1.8	PCIF_HSYNC	RXEV0	Parallel Camera Interface Horizontal Sync; CM4 Rx Event Input.
L4	P1.9	P1.9	PCIF_PCLK	TXEV0	Parallel Camera Interface Pixel Clock; CM4 Tx Event Output.
K13	P1.10	P1.10	SDHC_CDN	ADC_CLK_EXT	Secure Digital Interface Card Present; ADC External Clock Input.
K11	P1.11	P1.11	SDHC_DAT3	—	Secure Digital Interface Data Bus Bit 3.
L11	P1.12	P1.12	SDHC_DAT2	ADC_HW_TRIG_A	Secure Digital Interface Data Bus Bit 2; ADC Trigger Input A.
K12	P1.13	P1.13	SDHC_DAT1	ADC_HW_TRIG_B	Secure Digital Interface Data Bus Bit 1; ADC Trigger Input B.
L12	P1.14	P1.14	SDHC_DAT0	ADC_HW_TRIG_C	Secure Digital Interface Data Bus Bit 0; ADC Trigger Input C.
J11	P1.15	P1.15	SDHC_WP	—	Secure Digital Interface Write Protect.
M11	P1.16	P1.16	SDHC_CMD	—	Secure Digital Interface Bus Command.
L13	P1.17	P1.17	SDHC_CLK	—	Secure Digital Interface Clock.
F4	P2.0	P2.0	AIN0/AIN0N	—	ADC Input 0/Comparator 0 Negative Input.
E4	P2.1	P2.1	AIN1/AIN0P	—	ADC Input 1/Comparator 0 Positive Input.
D4	P2.2	P2.2	AIN2/AIN1N	—	ADC Input 2/Comparator 1 Negative Input.
C4	P2.3	P2.3	AIN3/AIN1P	—	ADC Input 3/Comparator 1 Positive Input.
F3	P2.4	P2.4	AIN4/AIN2N	LPTMR0B_IOA	ADC Input 4/Comparator 2 Negative Input; Low-Power Timer0 I/O Port Map B.
E3	P2.5	P2.5	AIN5/AIN2P	LPTMR1B_IOA	ADC Input 5/Comparator 2 Positive Input; Low-Power Timer1 I/O Port Map B.
D3	P2.6	P2.6/ LPTMR0_CLK	AIN6/AIN3N	LPUARTB_RX	Low-Power Timer0 External Clock Input/ADC Input 6/Comparator 3 Negative Input; Low-Power UART0 Receive Port Map B.
C3	P2.7	P2.7/ LPTMR1_CLK	AIN7/AIN3P	LPUARTB_TX	Low-Power Timer1 External Clock Input/ADC Input 7/Comparator 3 Positive Input; Low-Power UART Transmit Port Map B.
D11	P3.0	P3.0/PDOWN/ WAKEUP	—	—	Power-Down Output; Wakeup Input. This device pin can only be powered by V_{DDIOH}.
D10	P3.1	P3.1/SQWOUT/ WAKEUP	—	—	RTC Square-Wave Output; Wakeup Input. This device pin can only be powered by V_{DDIOH}.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
USB					
E13	DP	—	—	—	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
D13	DM	—	—	—	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
MIPI CSI-2					
B6	CSI_CKP	—	—	—	MIPI CSI-2 receiver differential clock positive input.
A6	CSI_CKN	—	—	—	MIPI CSI-2 receiver differential clock negative input.
C7	CSI_D0P	—	—	—	MIPI CSI-2 receiver differential data lane 0 positive input.
C6	CSI_D0N	—	—	—	MIPI CSI-2 receiver differential data lane 0 negative input.
B7	CSI_D1P	—	—	—	MIPI CSI-2 receiver differential data lane 1 positive input.
A7	CSI_D1N	—	—	—	MIPI CSI-2 receiver differential data lane 1 negative input.

Detailed Description

Artificial intelligence (AI) requires extreme computational horsepower, but Analog Devices is cutting the power cord from AI insights. The MAX78002 is a new breed of AI microcontroller built to enable neural networks to execute at ultra-low power and live at the edge of the IoT. This product combines the most energy-efficient AI processing with Analog Devices' proven ultra-low-power microcontrollers. Our hardware-based convolutional neural network (CNN) accelerator enables battery-powered applications to execute AI inferences while spending only microjoules of energy.

The MAX78002 is an advanced system-on-chip featuring an Arm Cortex-M4 with FPU CPU for efficient system control with an ultra-low-power deep neural network accelerator. The CNN engine has a weight storage memory of 2MB, and can support 1-, 2-, 4-, and 8-bit weights (supporting networks of up to 16 million weights). The CNN weight memory is SRAM-based so that AI network updates can be made on the fly. The CNN engine also has 1.3MB of data memory. The CNN architecture is highly flexible, allowing networks to be trained in conventional toolsets like PyTorch and TensorFlow, then converted for execution on the MAX78002 using tools provided by Analog Devices.

In addition to the memory in the CNN engine, the MAX78002 has large on-chip system memory for the microcontroller core, with 2.5MB flash and up to 384KB SRAM. Multiple high-speed and low-power communications interfaces are supported, including I^2S, MIPI CSI-2 serial camera, parallel camera (PCIF), and SD 3.0/SDIO 3.0/eMMC 4.51 secure digital.

Arm Cortex-M4 with FPU Processor and RISC-V RV32 Processor

The Arm Cortex-M4 with FPU processor (CM4) is ideal for AI system control. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction, multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed or unsigned data with or without saturation

The addition of a 32-bit RISC-V coprocessor (RV32) provides the system with ultra-low power consumption signal processing.

Convolutional Neural Network Accelerator (CNN)

The CNN accelerator consists of 64 parallel processors with 1.31MB of SRAM-based storage. Each processor includes a pooling unit and a convolutional engine with dedicated weight memory. Four processors share one data memory. These are further organized into groups of 16 processors that share common controls. A group of 16 processors operates as a peripheral to another group or independently. Data is read from SRAM associated with each processor and written to any data memory located within the accelerator. Any given processor has visibility of its dedicated weight memory and the data memory instance it shares with the three others.

The features of the CNN accelerator include:

- Data storage
  - 1.31MB SRAM-based data storage
  - Configured as 20Kx8-bit integers x64 channels or 80Kx8-bit integers x4 channels for input layers
  - Input data format – 8-bit signed values
  - Selectable output data format – 8-bit signed integer or 32-bit signed integer for last layer
  - Arm AMBA APB accessible
  - Hardware CNN results data unload assist
- Weight storage
  - SRAM based with selectable data retention mode
  - Configurable from 2M 8-bit integer weights to 16M 1-bit logical weights

- Optional 4x processing mode splits each weight memory into four parallel memories with a common address generating 4x the number of masks each cycle
- All processors include the following dedicated weight storage:
  - 1x processing mode
    - 4096x9x8-bit weights
    - 8192x9x4-bit weights
    - 16384x9x2-bit weights
    - 32768x9x1-bit weights
  - 4x processing mode
    - 4x1024x9x8-bit weights
    - 4x2048x9x4-bit weights
    - 4x4096x9x2-bit weights
    - 4x8192x9x1-bit weights
- The first processor in each x16 includes additional weight storage for input layer processing:
  - 1x processing mode
    - 1024x9x8-bit weights
    - 2048x9x4-bit weights
    - 4096x9x2-bit weights
    - 8196x9x1-bit weights
  - 4x processing mode
    - 4x256x9x8-bit weights
    - 4x512x9x4-bit weights
    - 4x1024x9x2-bit weights
    - 4x2048x9x1-bit weights
- Programmable per x16 processor weight RAM start address, start pointer, and mask count
- Arm AMBA APB accessible
- Optional weight load hardware assist for packed weight storage

● 128 independently configurable layers (per x16 processor)
- Programmable start layer – any of the 128 layers
- Linked layer mode allows arbitrary nonsequential layer execution
- Configurable per layer parameters
  - Processor and mask enables (16 channels)
  - Input data format – byte-wide input data or 4x8-bit wide input data (x16 processors 0, 4, 8, or 12 only)
  - Per layer data streaming
    - Up to eight simultaneous streaming layers – available for the first eight layers
    - Optional FIFO input data paths (first layer only)
    - Selectable streaming termination layer – transition to nonstream processing mode
    - Programmable per stream configuration
      - Stream start – relative to prior stream
      - Three stream processing delay counters – two column counters for noninteger ratios, 1-row delta counter
      - Data SRAM circular buffer size
  - Programmable input data size (separate row, column fields)
  - Programmable row and column padding – 0 to 3 bytes
  - Configurable number of input channels – 1 to 1024
  - Configurable number of output channels – 1 to 1024 (determined by the kernel count value)
  - Selectable kernel bit width size (1, 2, 4, or 8)
  - Selectable kernel SRAM pointer start address and count
  - Optional in-flight input image pooling
    - Pool mode – none, maximum, or average
    - Pool size – 2x2 to 16x16 with independent row and column counts
    - Pool dilation – 0 to 15
  - Programmable stride – 1 to 4 common row/column stride value
  - Data SRAM read pointer base address
    - Configurable read pointer increment value for flexible input channel access

  - Data SRAM write pointer configuration
    - Base address
    - Independent offsets for output channel storage in SRAM
    - Programmable stride increment offset
  - Bias – 8192 8-bit integers with an option for 1024 10-bit integers using multiple x16 processors
    - Optionally configurable as 4x2048x8-bit bias for 4x mode (with an option for 10-bit bias using multiple x16 processors)
  - Pre-activation output scaling – direction (up/down) and 0 to 15-bit shift magnitude
  - Output activation – none, ReLU, absolute value
  - Pass-through mode allows input data to be passed directly through to the output with programmable data relocation.
  - Element-wise operations (add, subtract, XOR, OR) with optional convolution – up to 16 elements
  - Deconvolution
  - Flattening - for MLP processing
  - Depthwise convolution
  - Simple logic modes support single mask bit +1/-1, 0/-1 modes
  - No mask mode supports convolutions with a fixed mask value of 1
- Processing
  - 64 parallel physical channel processors
    - Organized as 4 x 16 processors
    - 8-bit integer data path with an option for 32-bit integers on the output layer
    - Per channel processor enable/disable
    - Expandable to 1024 parallel logical channel processors
  - Configurable 3x3 or 1x1 2D kernel size
  - Configurable 1D kernel size to 1x9
  - Full-resolution sum-of-products arithmetic for 1024 8-bit integer (data and weight) channels
  - Two maximum operating frequency modes – up to 50MHz in nonpipelined mode or up to 200MHz in pipeline mode
  - Up to 16 output channels per clock processing rate
  - Conditional execution allows early layer termination and branching based on the programmable address and/or data and/or count match
- Input layer maximum input size
  - 20KB, 64 channels, non-streaming, APB I/F
  - 80KB, 16 channels, non-streaming, APB I/F
  - 80KB, 4 channels, non-streaming, FIFO I/F
  - 2048x2048 bytes, 4 channels, streaming, FIFO I/F
- Hidden layers maximum input size
  - Up to 20KB per channel, x64 channels, nonstreaming
  - 20KB can be split equally across 1 to 16 logical channels, nonstreaming
  - 4MB per channel, x64 channels, streaming
  - 4MB can be split equally across eight layers, streaming
- Optional interrupt on CNN completion and FIFO full and empty statuses
- User accessible BIST on all internal memories
- User accessible zeroization of all internal memories
- Single-step operation with full data SRAM access for CNN operation debug
- Power management
  - Independent x16 processor supply enables
  - Independent x16 processor mask retention enables
  - Independent x16 data path clock enables
  - Functional APB clock gating with per x16 processor override – registers clocked only during APB write access.
  - CNN clock frequency scaling (divide by 2, 4, 8, or 16)
  - Chip-level voltage control for power-performance optimization
- Input data row buffer memory (TRAM)

  - Organized as 12Kx16 or optionally as 4x3Kx16 in read-ahead mode
  - Programmable per layer TRAM read/write pointer start and rollover values
  - Automatically allocates memory based on the programmed number of input channels
- Read ahead input processing mode allows the next input data byte to be preprocessed while the current input byte output channel generation is active.

Memory

Internal Flash Memory

2.5MB of internal flash memory provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 384KB SRAM provides low-power retention of application information in all power modes except POWER DOWN. The SRAM is divided into eight banks. SRAM0 and SRAM1 are both 32KB; SRAM2, SRAM3, SRAM4, and SRAM5 are all 64KB each. SRAM6 is 48KB, and SRAM7 is 16KB. SRAM4, SRAM5, SRAM6, and SRAM7 are accessible by the RV32 in LOW POWER mode. For enhanced system reliability, SRAM0 (32KB) can be configured with error correction coded (ECC) single error correction-double error detection (SEC-DED). This data retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Dynamic Voltage Scaling (DVS) Controller

The DVS controller works using the fixed high-speed oscillator and the V_{COREA} supply voltage to optimally operate the Arm core at the lowest practical voltage. The ability to adaptively adjust the voltage provides a significant reduction in dynamic power consumption.

The DVS controller provides the following features:

- Controls DVS monitoring and adjustment functions
- Continuous monitoring with programmable monitor sample period
- Controlled transition to a programmable operating point
- Independent high and low operating limits for safe, bounded operation
- Independent high, center, and low operating range delay line delay monitors
- Programmable adjustment rate – when an adjustment is required
- Single clock operation
- Arm peripheral bus interface provides control and status access
- Interrupt capability during error

Clocking Scheme

Multiple clock sources can be selected as the system clock:

- Internal phase-locked loop (IPLL) provides 100MHz and 200MHz clock sources
- Internal primary oscillator (IPO) at a nominal frequency of 120MHz
- Internal secondary oscillator (ISO) at a nominal frequency of 60MHz
- Configurable internal nanoring oscillator (INRO) at 8kHz, 16kHz, or 30kHz
- External RTC oscillator at 32.768kHz (ERTCO) (external crystal required)
- Internal baud rate oscillator at 7.3728MHz (IBRO)
- External square-wave clock up to 80MHz

There are multiple external clock inputs:

- LPTMR0 and LPTMR1 can be clocked from unique external sources.
- I^2S can be be clocked from its own external source.
- USB can be clocked from its own external source.

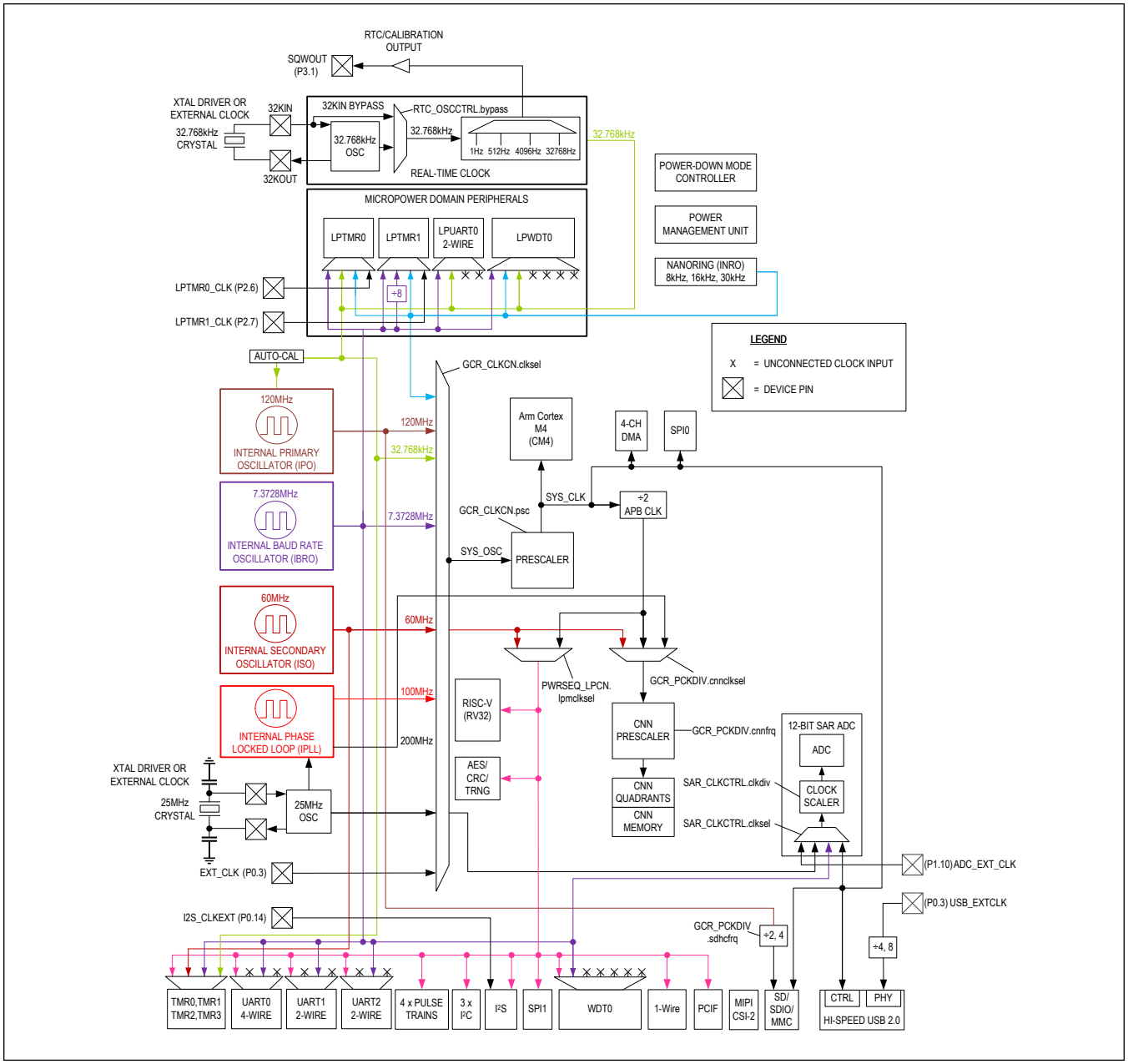

Figure 9. Clocking Scheme

General-Purpose I/O (GPIO) and Special Function Pins

Most GPIO pins share both a firmware-controlled I/O function and one or more alternate functions associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Although this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be

independently enabled, and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector.

When configured as GPIO, the following features are provided. The features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pull-up resistor or internal pull-down resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX78002 provides up to 60 GPIO pins. Caution is needed since Port 3 (P3.0 and P3.1 device pins) are configured in a different manner from the above description. Refer to the MAX78002 User Guide for details.

MIPI Camera Serial Interface 2 (MIPI CSI-2) Controller

The MIPI CSI-2 is a low voltage interface suited for CMOS image sensors with the following features:

- D-PHY 2.1
- MIPI Alliance Standard for Camera Serial Interface 2 Version 2.1 compliant
- Implements all three CSI-2 MIPI Layers (Pixel to Byte packing, Low-Level Protocol, Lane Management)
- Receiver only
- Two data lanes, one clock lane
- Supports high speed (4.5+ Gbps) D-PHY operation
- Support for all CSI-2 data types
- Error correction support

Parallel Camera Interface (PCIF)

The PCIF is a low-voltage interface suited for CMOS image sensors. It provides up to 12-bits of parallel access capability with single capture and continuous mode operation.

Analog-to-Digital Converter (ADC)

The 12-bit successive approximation register (SAR) ADC provides an external reference input and a single-ended input multiplexer. The multiplexer selects an input channel from one of the eight external analog input signals (AIN0–AIN7) or the internal power supply inputs.

The reference for the ADC can be:

- External V_{REF} input
- Internal 1.25V or 2.048V selectable

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a power mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the CPU is in SLEEP, LOW POWER, or MICRO POWER mode. The eight AIN[7:0] inputs can be configured as four pairs and deployed as four independent comparators.

The ADC measures the following voltages:

- AIN[7:0] up to 3.3V
- V_{BAT}
- V_{SS}
- V_{COREA}
- V_{COREB}
- 2.5V internal LDO
- 0.9V internal LDO
- V_{DDB}
- V_{DDA}
- Internal die temperature sensor output

Comparators

The eight AIN[7:0] inputs can be configured as four pairs and deployed as four independent comparators with the following features:

- Comparison events can trigger interrupts
- Events can wake the CM4 from SLEEP, LOW POWER, MICRO POWER, STANDBY, or BACKUP operating modes
- Can be active in all power modes

Single-Inductor Multiple-Output Switch-Mode Power Supply (SIMO SMPS)

The SIMO SMPS built into the device provides a monolithic power supply architecture for operation from a single lithium cell. The SIMO provides three buck regulator outputs that are voltage programmable. This architecture optimizes power consumption efficiency of the device and minimizes the bill of materials for the circuit design since only a single inductor/capacitor pair is required.

Power Management

Power Management Unit

The power management unit (PMU) provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPUs and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple power domains
- Fast wake-up of powered-down peripherals when activity detected
- Optional control of external switches to provide the CNN with dedicated power from an external source

ACTIVE Mode

In this mode, the CM4 and the RV32 can execute application code and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption. The CM4 has access to all system SRAM. The RV32 has access to SRAM4, SRAM5, SRAM6, and SRAM7. Both the CM4 and the RV32 can execute from internal flash simultaneously. SRAM7 can be configured as an instruction cache for the RV32.

SLEEP Mode

This mode consumes less power, but wakes faster because the clocks can optionally be enabled.

The device status is as follows:

- CM4 is asleep.
- RV32 is asleep.
- CNN quadrants and memory are configurable.
- Peripherals are on.
- Standard DMA is available for optional use.

LOW POWER Mode (LPM)

This mode is suitable for running the RV32 processor to collect and move data from enabled peripherals.

The device status is as follows:

- The CM4, SRAM0, SRAM1, SRAM2, and SRAM3 are in state retention.
- CNN quadrants and memory are configurable and active.
- The RV32 can access the SPI, all UARTS, all timers, I^2C, 1-Wire, pulse train engines, I^2S, CRC, AES, TRNG, PCIF, and comparators, as well as SRAM4, SRAM5, SRAM6, and SRAM7. SRAM7 can be configured to operate as RV32 instruction cache.
- The transition from LOW POWER mode to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.

- The DMA can access flash.
- IPO and IPLL can be optionally powered down.
- The following oscillators are enabled:
  - IBRO
  - ERTCO
  - INRO
  - ISO

MICRO POWER Mode (µPM)

This mode is used for extremely low power consumption while using a minimal set of peripherals to provide wakeup capability.

The device status is as follows:

- Both CM4 and RV32 are state retained. System state and all SRAM is retained.
- CNN quadrants are powered off.
- CNN memory provides selectable retention.
- The GPIO pins retain their state.
- All non-MICRO POWER peripherals are state retained.
- The following oscillators are powered down:
  - IPO
  - IPLL
  - ISO
- The following oscillators are enabled:
  - IBRO
  - ERTCO
  - INRO
- The following MICRO POWER mode peripherals are available to wake up the device:
  - LPUART0
  - WWDT1
  - All four low-power analog comparators

STANDBY Mode

This mode is used to maintain the system operation while keeping time with the RTC.

The device status is as follows:

- Both CM4 and RV32 are state retained. System state and all SRAM are retained.
- CNN quadrants are powered off.
- CNN memory provides selectable retention.
- GPIO pins retain their state.
- All peripherals are state retained.
- The following oscillators are powered down:
  - IPO
  - IPLL
  - ISO
  - IBRO
- The following oscillators are enabled:
  - ERTCO
  - INRO

BACKUP Mode

This mode is used to maintain the system RAM. The device status is as follows:

- CM4 and RV32 are powered off.

- SRAM0 thru SRAM7 can be configured to be state retained as per Table 1.
- CNN memory provides selectable retention.
- All peripherals are powered off.

The following oscillators are powered down:

- IPO
- IPLL
- ISO
- IBRO

The following oscillators are enabled:

- ERTCO
- INRO

Table 1. BACKUP Mode SRAM Retention Block Sizes

RAM BLOCK	RAM SIZE
SRAM0	32KB + ECC
SRAM1	32KB
SRAM2	64KB
SRAM3	64KB
SRAM4	64KB
SRAM5	64KB
SRAM6	48KB
SRAM7	16KB

POWER DOWN Mode (PDM)

This mode is used during product level distribution and storage. The device status is as follows:

- CM4 and RV32 are powered off.
- All peripherals and SRAM are powered down.
- All oscillators are powered down.
- There is no data retention in this mode, but values in flash memory are preserved.
- Voltage monitors are operational.

Wakeup Sources

The sources of wakeup from the SLEEP, LOW POWER, MICRO POWER, STANDBY, BACKUP, and POWER DOWN operating modes are summarized in Table 2.

Table 2. Wakeup Sources

OPERATING MODE	WAKEUP SOURCE
SLEEP	Any enabled peripheral with interrupt capability; RSTN
LOW POWER (LPM)	SPI0, I^2S, I^2C, UARTs, timers, watchdog timers, wakeup timer, all comparators, RTC, GPIOs, RSTN, and RV32
MICRO POWER (µPM)	All comparators, LPUART, LPTMR1, LPTIMER2, LPWDT0, RTC, wakeup timer, GPIOs, and RSTN
STANDBY	RTC, wakeup timer, GPIOs, CMP0, and RSTN
BACKUP	RTC, wakeup timer, GPIOs, CMP0, and RSTN
POWER DOWN (PDM)	P3.0, P3.1, and RSTN

Real-Time Clock

An RTC keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years

and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed with a tick resolution of 244µs. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

The RTC calibration feature provides the ability for user software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the SQWOUT alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Programmable Timers

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0–TMR3 can be configured as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX78002 provides six 32-bit timers (TMR0, TMR1, TMR2, TMR3, LPTMR0, and LPTMR1). LPTMR0 and LPTMR1 are capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes.

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all of the ports depending on the device configuration. See Table 3 for individual timer features.

Table 3. Timer Configuration Options

INSTANCE	REGISTER ACCESS NAME	SINGLE 32 BIT	DUAL 16 BIT	SINGLE 16 BIT	POWER MODE	CLOCK SOURCE						
						PCLK	ISO	IBRO	INRO	ERTCO	LPTMR0_CLK	LPTMR1_CLK
TMR0	TMR0	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
TMR1	TMR1	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No

Table 3. Timer Configuration Options (continued)

TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
LPTMR0	TMR4	No	No	Yes	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	No	Yes	Yes	Yes	Yes	No
LPTMR1	TMR5	No	No	Yes	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	No	Yes	Yes	Yes	No	Yes

Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed watchdog timer (WDT), which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific window of time. See Table 4 for individual timer features.

The MAX78002 provides two instances of the watchdog timer—WDT0 and LPWDT0.

Table 4. Watchdog Timer Configuration Options

INSTANCE NAME	REGISTER ACCESS NAME	POWER MODE	CLOCK SOURCE			
			PCLK	IBRO	INRO	ERTCO
WDT0	WDT0	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No	No
LPWDT0	WDT1	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	Yes	Yes	Yes

Pulse Train Engine (PT)

Multiple, independent pulse train generators can provide either a square-wave or a repeating pattern from 2 to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level, allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (such as divide by 2, divide by 4, and divide by 8) of the input pulse train module clock

- Input pulse train module clock can be optionally configured to be independent from the system AHB clock
- Multiple repetition options
  - Single shot (nonrepeating pattern of 2 to 32 bits)
  - Pattern repeats user-configurable number of times or indefinitely
  - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

The MAX78002 provide up to four instances of the pulse train engine peripheral (PT[3:0]).

Serial Peripherals

High-Speed USB Peripheral

The integrated USB peripheral is compliant with the High-Speed (480Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator enables smart switching between the main supply and V_{DDB} when connected to a USB host controller. The USB peripheral supports DMA for the endpoint buffers. A total of 11 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

I²C Interface (I2C)

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. These engines support Standard-mode, Fast-mode, Fast-mode Plus, and High-speed mode I²C speeds. It provides the following features:

- Controller or target mode operation
  - Supports up to four different target addresses in target mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower target devices to operate on higher speed busses
- Multiple transfer rates
  - Standard-mode: 100kbps
  - Fast-mode: 400kbps
  - Fast-mode Plus: 1000kbps
  - High-speed mode: 3.4Mbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX78002 provides three instances of the I²C peripheral—I2C0, I2C1, and I2C2.

I²S Interface (I2S)

The I²S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Controller and target mode operation
- 8, 16, 24, and 32 bit frames
- Receive and transmit DMA support
- Wakeup on FIFO status (full/empty/threshold)
- Pulse density modulation support for receive channel
- Word select polarity control
- First bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes

- Transmitter FIFO depth of 32 bytes

The MAX78002 provides one instance of the I^2S peripheral (I2S).

Serial Peripheral Interface (SPI)

SPI is a highly configurable, flexible, and efficient synchronous interface among multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more target select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either target or controller mode and provide the following features:

- SPI modes 0, 1, 2, or 3 for single-bit communication
- 3- or 4-wire mode for single-bit target device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad data modes supported
- Multiple target selects on some instances
- Multicontroller mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Target select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX78002 provides two instances of the SPI peripheral—SPI0 and SPI1. See Table 5 for configuration options.

Table 5. SPI Configuration Options

INSTANCE	DATA	TARGET SELECT LINES	MAXIMUM FREQUENCY CONTROLLER MODE (MHz)	MAXIMUM FREQUENCY TARGET MODE (MHz)
SPI0	3-wire, 4-wire, dual, or quad data support	3	60	60
SPI1	3-wire, 4-wire, dual, or quad data support	1	30	60

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- 12.5Mbps for UART maximum bit rate
- 1.85Mbps for LPUART maximum bit rate
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX78002 provides four instances of the UART peripheral—UART0, UART1, UART2, and LPUART0. LPUART0 is capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes. See Table 6 for configuration options.

Table 6. UART Configuration Options

INSTANCE NAME	REGISTER ACCESS NAME	HARDWARE FLOW CONTROL	POWER MODE	CLOCK SOURCE		
				PCLK	IBRO	ERTCO
UART0	UART0	Yes	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No
UART1	UART1	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No
UART2	UART2	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No
LPUART0	UART3	No	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	Yes	Yes

1-Wire Controller (OWM)

Analog Device's 1-Wire bus consists of one signal that carries data and also supplies power to the target devices and a ground return. The bus controller communicates serially with one or more target devices through the bidirectional, multidrop 1-Wire bus. The single-contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire controller supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The OWM supports both standard (15.6kbps) and overdrive (110kbps) speeds.

Standard DMA Controller

The standard DMA controller allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 4-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

The MAX78002 provides one instance of the standard DMA controller.

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

True Random Number Generator (TRNG) Non-Deterministic Random Bit Generator (NDRBG)

The device provides a non-deterministic entropy source that can be used to generate cryptographic seeds or strong encryption keys as part of an overall framework for a secure customer application.

Software can use random numbers to trigger asynchronous events that add complexity to program execution to thwart replay attacks or key search methodologies.

The TRNG can support the system-level validation of many security standards. Analog Devices will work directly with the customer's validation laboratory to provide the laboratory with any required information. Contact Analog Devices for details of compliance with specific standards.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. It supports a user-defined programmable polynomial up to 32-bits. Direct memory access copies data into the CRC module so that CRC calculations on large blocks of memory are performed with minimal CPU intervention. Examples of common polynomials are depicted in Table 7.

Table 7. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION
CRC-32-ETHERNET	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + x^0$
CRC-CCITT	$x^{16} + x^{12} + x^5 + x^0$
CRC-16	$x^{16} + x^{15} + x^2 + x^0$
USB DATA	$x^{16} + x^{15} + x^2 + x^0$
PARITY	$x^1 + x^0$

Bootloader

The bootloader allows loading and verification of program memory through a serial interface. It provides the following features:

- Bootloader interface through UART
- Program loading of Motorola® SREC format files
- Permanent lock state prevents altering or erasing program memory
- Access to the USN for device or customer application identification
- Disabling of the SWD interface to block debug access port functionality

The bootloader interface pins listed in Table 8 must be accessible to the host to use the bootloader.

Secure Boot

The secure boot feature available on some devices ensures software integrity by automatically comparing program memory against a stored HMAC SHA-256 hash value after every reset. Programs that fail the integrity check indicate corrupted or modified program memory and are prevented from executing any instructions. Devices with the secure boot feature provide additional security through an optional challenge/response feature that authenticates before executing bootloader commands.

Debug and Development Interface (SWD, JTAG)

The serial wire debug interface is used for code loading and ICE debug activities for the CM4. A JTAG interface is provided for the RV32. All devices in mass production have the debugging/development interface enabled.

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Applications Information

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Descriptions* table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each power pin/ball of the IC package. For example, if the *Pin Descriptions* table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. When more than one value of capacitor per pin is recommended, the capacitors should be placed in parallel starting with the lowest value capacitor closest to the pin.

Bootloader Activation

The bootloader interface options are shown in Table 8. The bootloader is activated if the activation pins are in their active state before exiting any reset and remain in that state until the bootloader sends the first command prompt through the interface. If the pins are not in their active state, the device will perform a secure boot and, if successful, begin execution of the application code. The design must ensure the activation pins and the RSTN pin are available to the host so it can activate the bootloader.

Note: *It is recommended that at least one of the bootloader activation pins are connected to a 10kΩ pull-up resistor to ensure that the pins are in their inactive state during reset.*

Table 8. Bootloader Interface

ACTIVATION PINS	INTERFACE
P0.0 UART0A_RX (Active Low) P0.29 SWDCLK (Active Low)	P0.0 UART0A_RX P0.1 UART0A_TX

Ordering Information

PART	FLASH (MB)	SYSTEM RAM (KB)	BOOTLOADER	SECURE BOOT	PIN-PACKAGE
MAX78002GXE+	2.5	384 + ECC 8	Yes	No	144 CSBGA, 12mm x 12mm x 1.3mm, 0.8mm pitch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/22	Initial release	—