# CD54HC173, CD74HC173, CD54HCT173, CD74HCT173

Data sheet acquired from Harris Semiconductor
SCHS158E

February 1998 - Revised October 2003

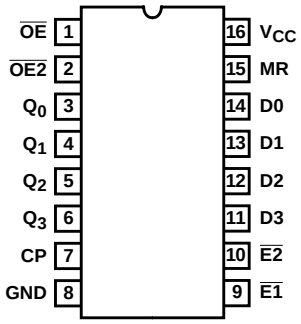
## High-Speed CMOS Logic Quad D-Type Flip-Flop, Three-State

### Features

- **Three-State Buffered Outputs**
- **Gated Input and Output Enables**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{o}$C to 125$^{o}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1 \propto A$ at $V_{OL}$, $V_{OH}$**

### Pinout

**CD54HC173, CD54HCT173**
**(CERDIP)**
**CD74HC173**
**(PDIP, SOIC, SOP, TSSOP)**
**CD74HCT173**
**(PDIP, SOIC)**
TOP VIEW




### Description

The ’HC173 and ’HCT173 high speed three-state quad D-type flip-flops are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and three-state feature make these parts ideally suited for interfacing with bus lines in bus oriented systems.

The four D-type flip-flops operate synchronously from a common clock. The outputs are in the three-state mode when either of the two output disable pins are at the logic “1” level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock If either of the 2 input ENABLES are taken to a logic “1” level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Reset is enabled by taking the MASTER RESET (MR) input to a logic “1” level. The data outputs change state on the positive going edge of the clock.

The ’HCT173 logic family is functionally, as well as pin compatible with the standard LS logic family**.**

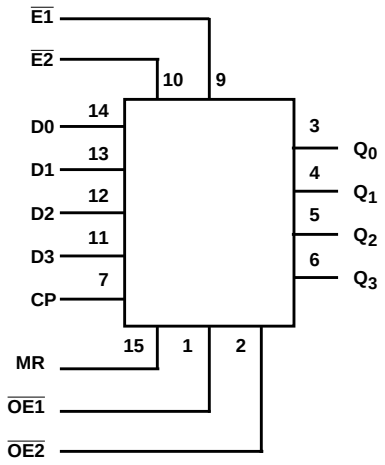
### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE |
|---|---|---|
| CD54HC173F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT173F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC173E | -55 to 125 | 16 Ld PDIP |
| CD74HC173M | -55 to 125 | 16 Ld SOIC |
| CD74HC173MT | -55 to 125 | 16 Ld SOIC |
| CD74HC173M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC173NSR | -55 to 125 | 16 Ld SOP |
| CD74HC173PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC173PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC173PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HCT173E | -55 to 125 | 16 Ld PDIP |
| CD74HCT173M | -55 to 125 | 16 Ld SOIC |
| CD74HCT173MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT173M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## Functional Diagram



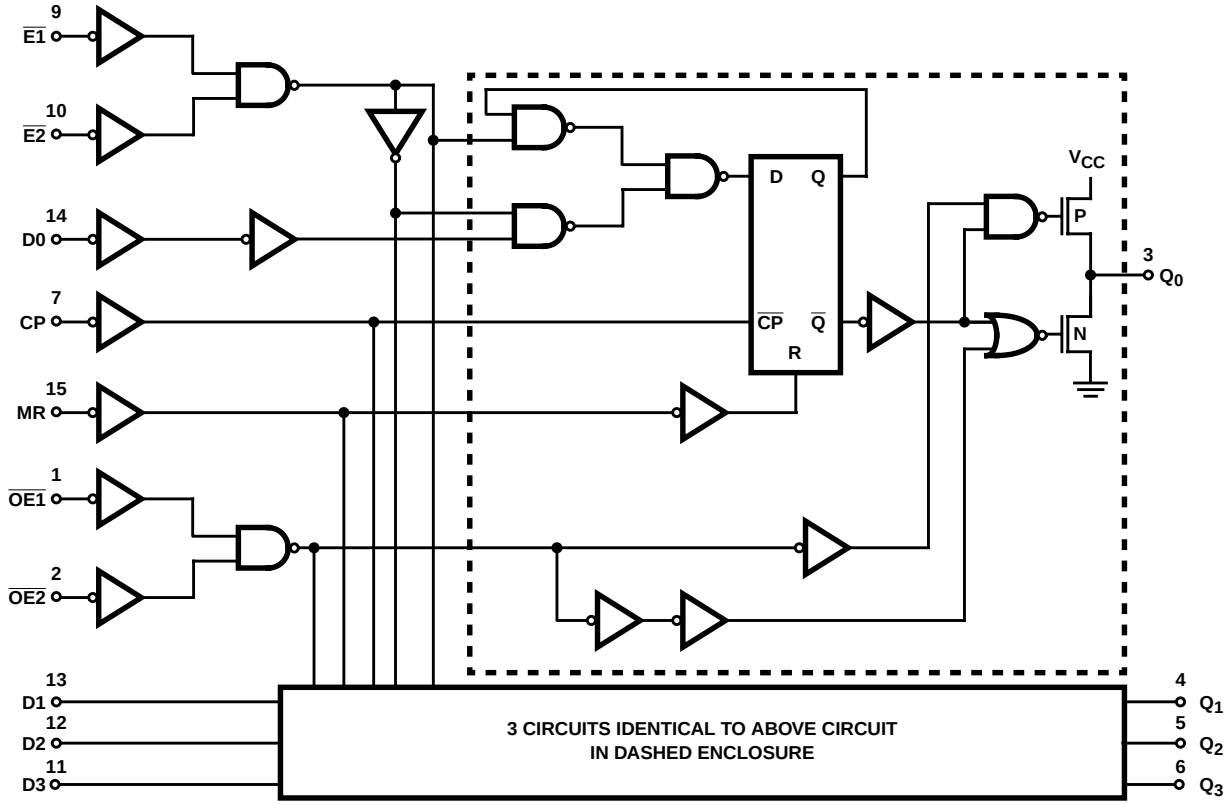

**TRUTH TABLE**

| INPUTS | | | | DATA | OUTPUT |
|---|---|---|---|---|---|
| | | DATA ENABLE | | | |
| MR | CP | $\overline{E1}$ | $\overline{E2}$ | D | $Q_n$ |
| H | X | X | X | X | L |
| L | L | X | X | X | $Q_0$ |
| L | ↑ | H | X | X | $Q_0$ |
| L | ↑ | X | H | X | $Q_0$ |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

H= High Voltage Level
L = Low Voltage Level
X= Irrelevant
↑= Transition from Low to High Level
$Q_0$= Level Before the Indicated Steady-State Input Conditions Were Established
NOTE:

1. When either OE1 or OE2 (or both) is (are) high, the output is disabled to the high-impedance state, however, sequential operation of the flip-flops is not affected.

## Logic Diagram



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±70mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 2):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package. . . . . 73°C/W
NS (SOP) Package . . . . . 64°C/W
PW (TSSOP) Package . . . . . 108°C/W
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | ∝A |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | ∝A |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IL}$ or $V_{IH}$ | - | 6 | - | - | ±0.5 | - | ±0.5 | - | ±10 | ∝A |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | ∝A |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | ∝A |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 3) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | ∝A |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IL}$ or $V_{IH}$ | - | 5.5 | - | - | ±0.5 | - | ±5.0 | - | ±10 | ∝A |

NOTE:

3. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| D0-D3 | 0.15 |
| $\overline{E1}$ and $\overline{E2}$ | 0.15 |
| CP | 0.25 |
| MR | 0.2 |
| $\overline{OE1}$ and $\overline{OE2}$ | 0.5 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g., 360∝A max at 25°C.

**Switching Specifications** Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| **HC TYPES** | | | | | | | | |
| Propagation Delay, Clock to Output | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 200 | 250 | 300 | ns |
| | | | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L$ = 15pF | 5 | 17 | - | - | - | ns |
| | | CL = 50pF | 6 | - | 34 | 43 | 51 | ns |
| Propagation Delay, MR to Output | $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| | | CL = 50pF | 6 | - | 30 | 37 | 45 | ns |
| Propagation Delay Output Enable to Q (Figure 6) | $t_{PLZ}$, $t_{PHZ}$ $t_{PZL}$, $t_{PZH}$ | CL = 50pF | 2 | | 150 | 190 | 225 | ns |
| | | $C_L$ = 50pF | 4.5 | | 30 | 38 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| | | CL = 50pF | 6 | | 26 | 33 | 38 | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | 60 | 75 | 90 | ns |
| | | | 4.5 | - | 12 | 15 | 18 | ns |
| | | | 6 | - | 10 | 13 | 15 | ns |
| Maximum Clock Frequency | $f_{MAX}$ | $C_L$ = 15pF | 5 | 60 | - | - | - | MHz |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | $C_O$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | $C_{PD}$ | - | 5 | 29 | - | - | - | pF |
| **HCT TYPES** | | | | | | | | |
| Propagation Delay, Clock to Output | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L$ = 15pF | 5 | 17 | - | - | - | ns |
| Propagation Delay, MR to Output | $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 44 | 55 | 66 | ns |
| | | $C_L$ = 15pF | 5 | 18 | - | - | - | ns |
| Propagation Delay Output Enable to Q (Figure 6) | $t_{PZL}$, $t_{PZH}$ | CL = 50pF | 2 | | 150 | 190 | 225 | ns |
| | | $C_L$ = 50pF | 4.5 | | 30 | 38 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| | | CL = 50pF | 6 | | 26 | 33 | 38 | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | 15 | 19 | 22 | ns |
| Maximum Clock Frequency | $f_{MAX}$ | $C_L$ = 15pF | 5 | 60 | - | - | - | MHz |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | $C_{PD}$ | - | 5 | 34 | - | - | - | pF |

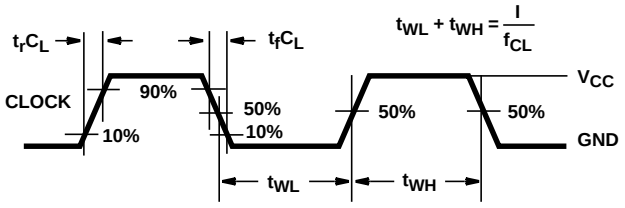
NOTES:

4. $C_{PD}$ is used to determine the dynamic power consumption, per package.
5. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where $f_i$ = Input Frequency, $f_O$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

**Prerequisite For Switching Specifications**

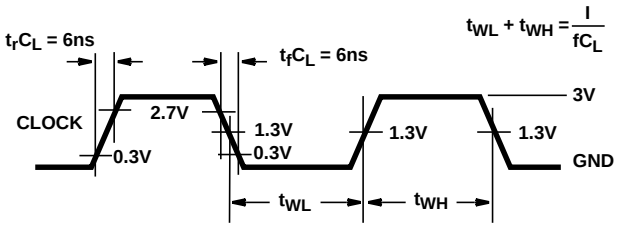
| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | |
| Maximum Clock Frequency | $f_{MAX}$ | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| MR Pulse Width | $t_w$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Clock Pulse Width | $t_w$ | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Set-up Time, Data to Clock and $\overline{E}$ to Clock | $t_{SU}$ | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | 6 | 10 | - | 13 | - | 15 | - | ns |
| Hold Time, Data to Clock | $t_H$ | 2 | 3 | - | 3 | - | 3 | - | ns |
| | | 4.5 | 3 | - | 3 | - | 3 | - | ns |
| | | 6 | 3 | - | 3 | - | 3 | - | ns |
| Hold Time, $\overline{E}$ to Clock | $t_H$ | 2 | 0 | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | 0 | - | 0 | - | ns |
| Removal Time, MR to Clock | $t_{REM}$ | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | 6 | 10 | - | 13 | - | 15 | - | ns |
| **HCT TYPES** | | | | | | | | | |
| Maximum Clock Frequency | $f_{MAX}$ | 4.5 | 20 | - | 16 | - | 13 | - | MHz |
| MR Pulse Width | $t_w$ | 4.5 | 15 | - | 19 | - | 22 | - | ns |
| Clock Pulse Width | $t_w$ | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| Set-up Time, $\overline{E}$ to Clock | $t_{SU}$ | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| Set-up Time, Data to Clock | $t_{SU}$ | 4.5 | 18 | - | 23 | - | 27 | - | ns |
| Hold Time, Data to Clock | $t_H$ | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Hold Time, $\overline{E}$ to Clock | $t_H$ | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Removal Time, MR to Clock | $t_{REM}$ | 4.5 | 12 | - | 15 | - | 18 | - | ns |

## Test Circuits and Waveforms




NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**




NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

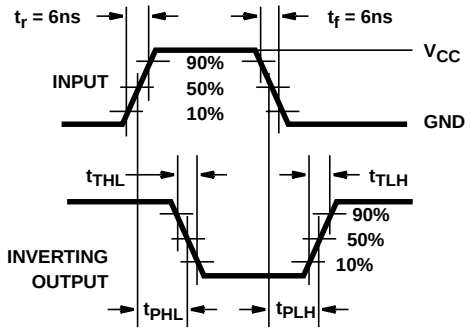



**FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

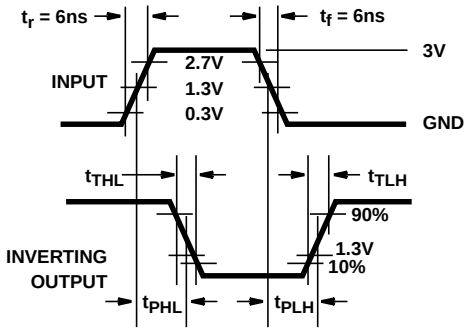



**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

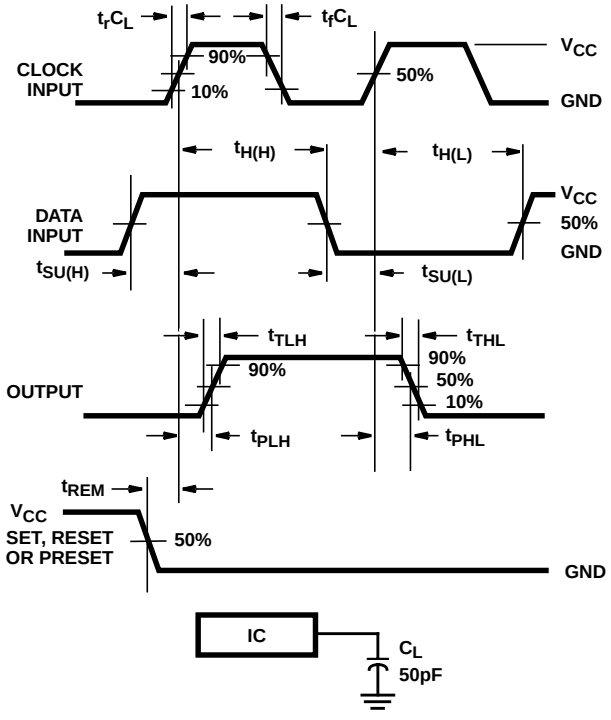



**FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

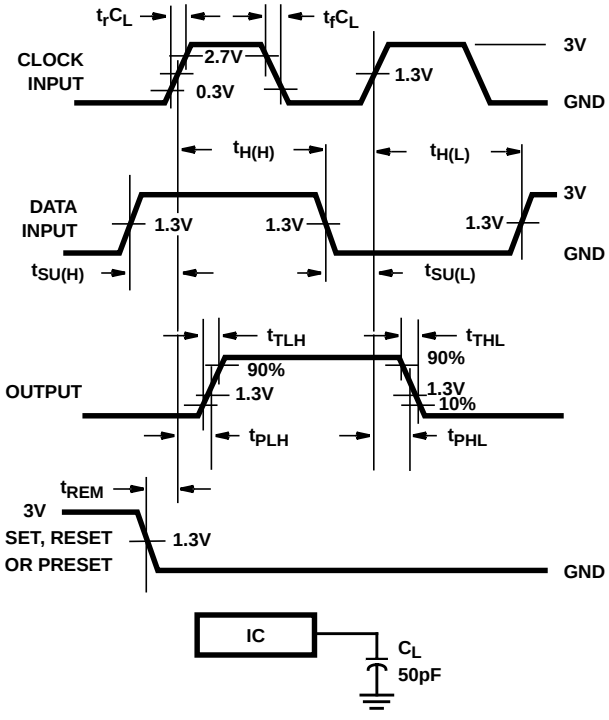



**FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

## Test Circuits and Waveforms (Continued)

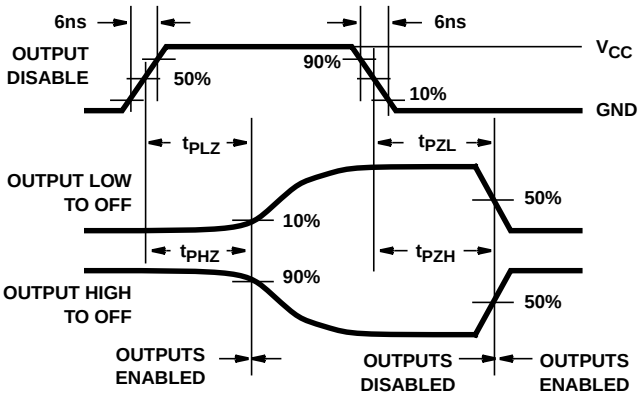



FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

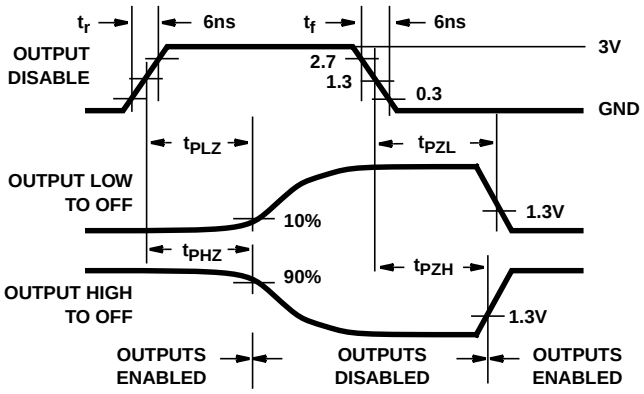
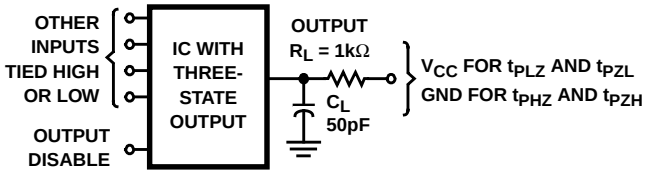



FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM




NOTE: Open drain waveforms $t_{PLZ}$ and $t_{PZL}$ are the same as those for three-state shown on the left. The test circuit is Output $R_L$ = 1kΩ to $V_{CC}$, $C_L$ = 50pF.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8682501EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8682501EA CD54HC173F3A | Samples |
| 5962-8875901EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8875901EA CD54HCT173F3A | Samples |
| CD54HC173F | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | CD54HC173F | Samples |
| CD54HC173F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8682501EA CD54HC173F3A | Samples |
| CD54HCT173F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8875901EA CD54HCT173F3A | Samples |
| CD74HC173E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC173E | Samples |
| CD74HC173M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC173M | Samples |
| CD74HC173M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC173M | Samples |
| CD74HC173M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC173M | Samples |
| CD74HC173MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC173M | Samples |
| CD74HC173PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ173 | Samples |
| CD74HC173PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ173 | Samples |
| CD74HCT173E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT173E | Samples |
| CD74HCT173M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT173M | Samples |
| CD74HCT173M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT173M | Samples |
| CD74HCT173MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT173M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF CD54HC173, CD54HCT173, CD74HC173, CD74HCT173 :**

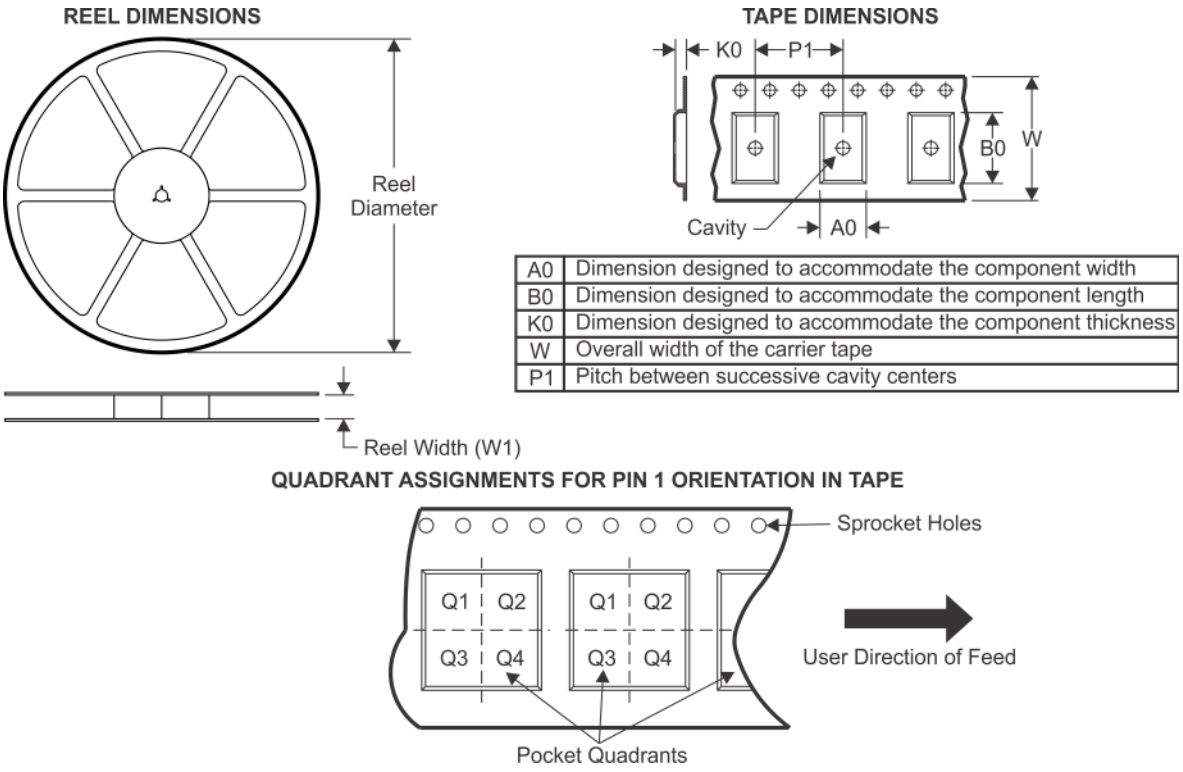
- Catalog: CD74HC173, CD74HCT173
- Military: CD54HC173, CD54HCT173

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

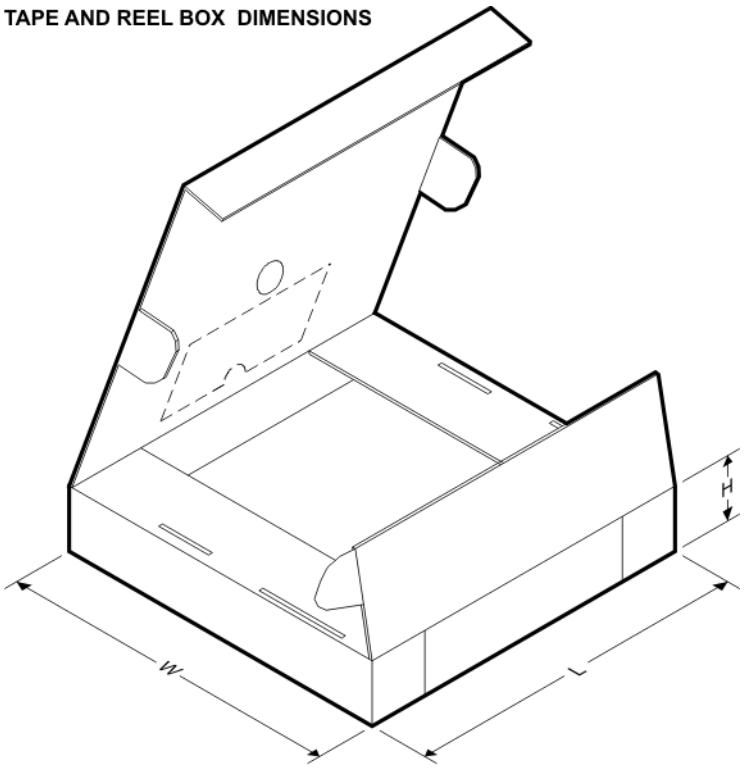



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC173M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC173PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT173M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

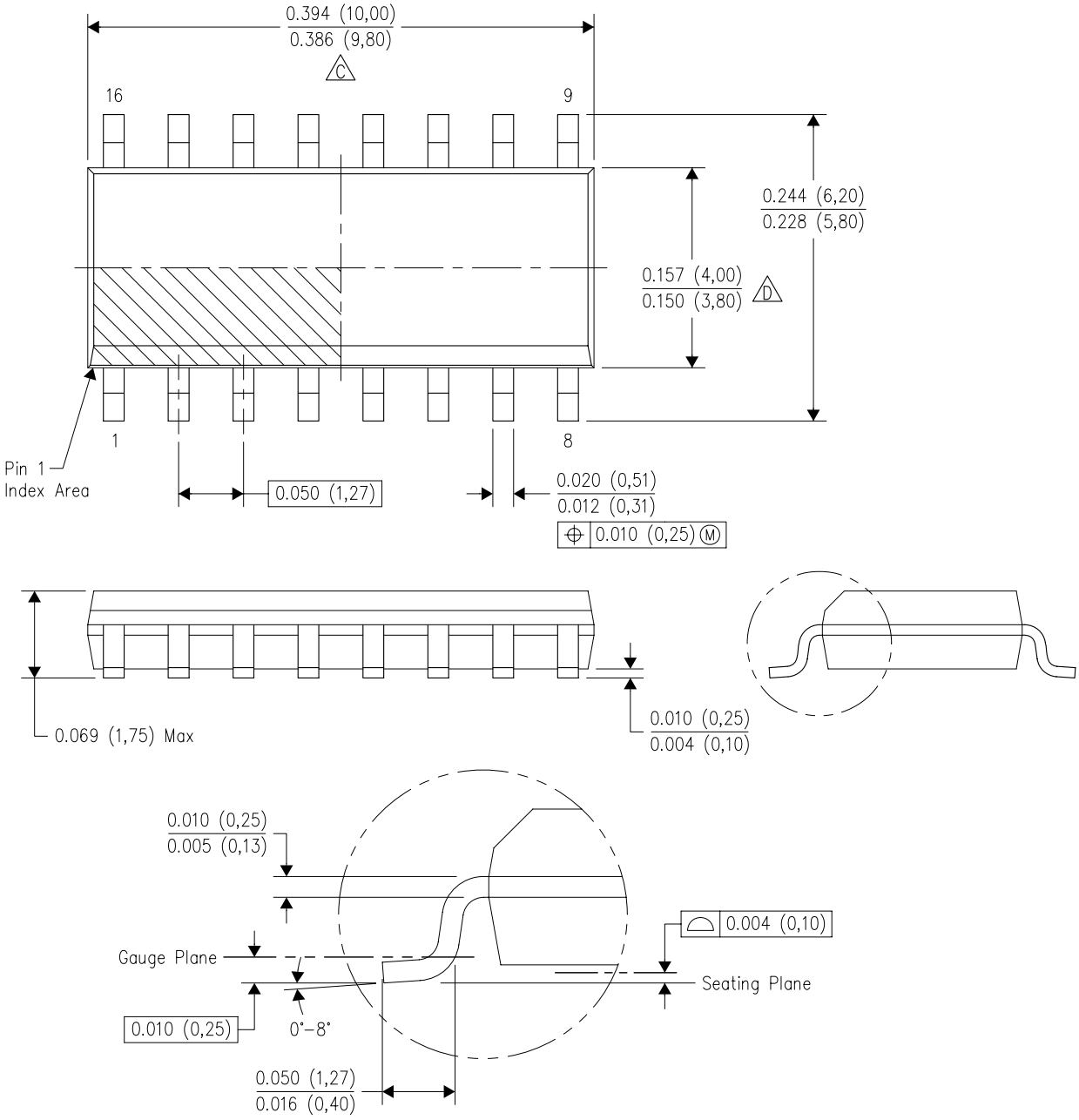
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

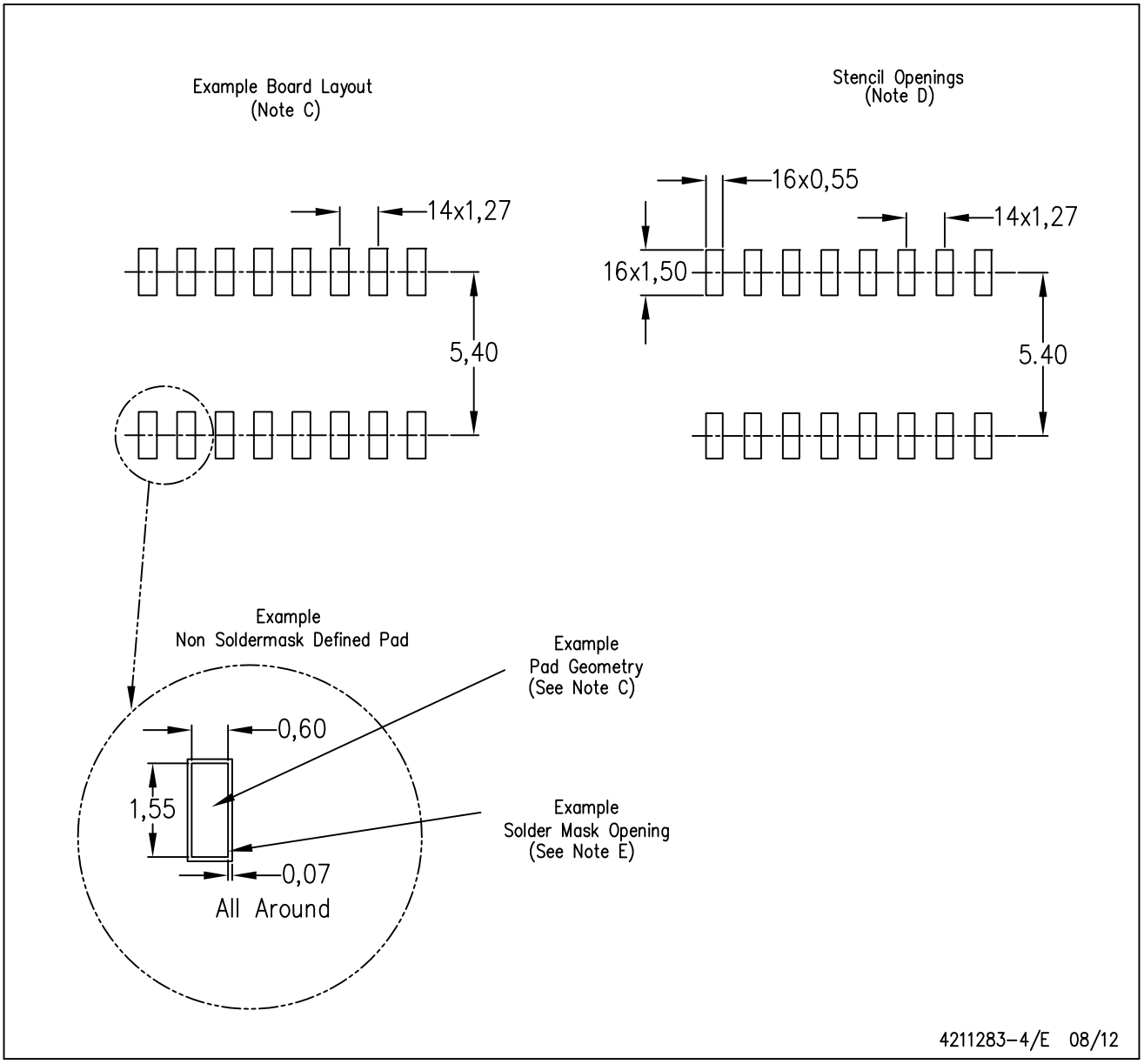
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC173M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC173PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD74HCT173M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

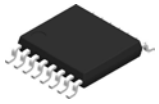
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

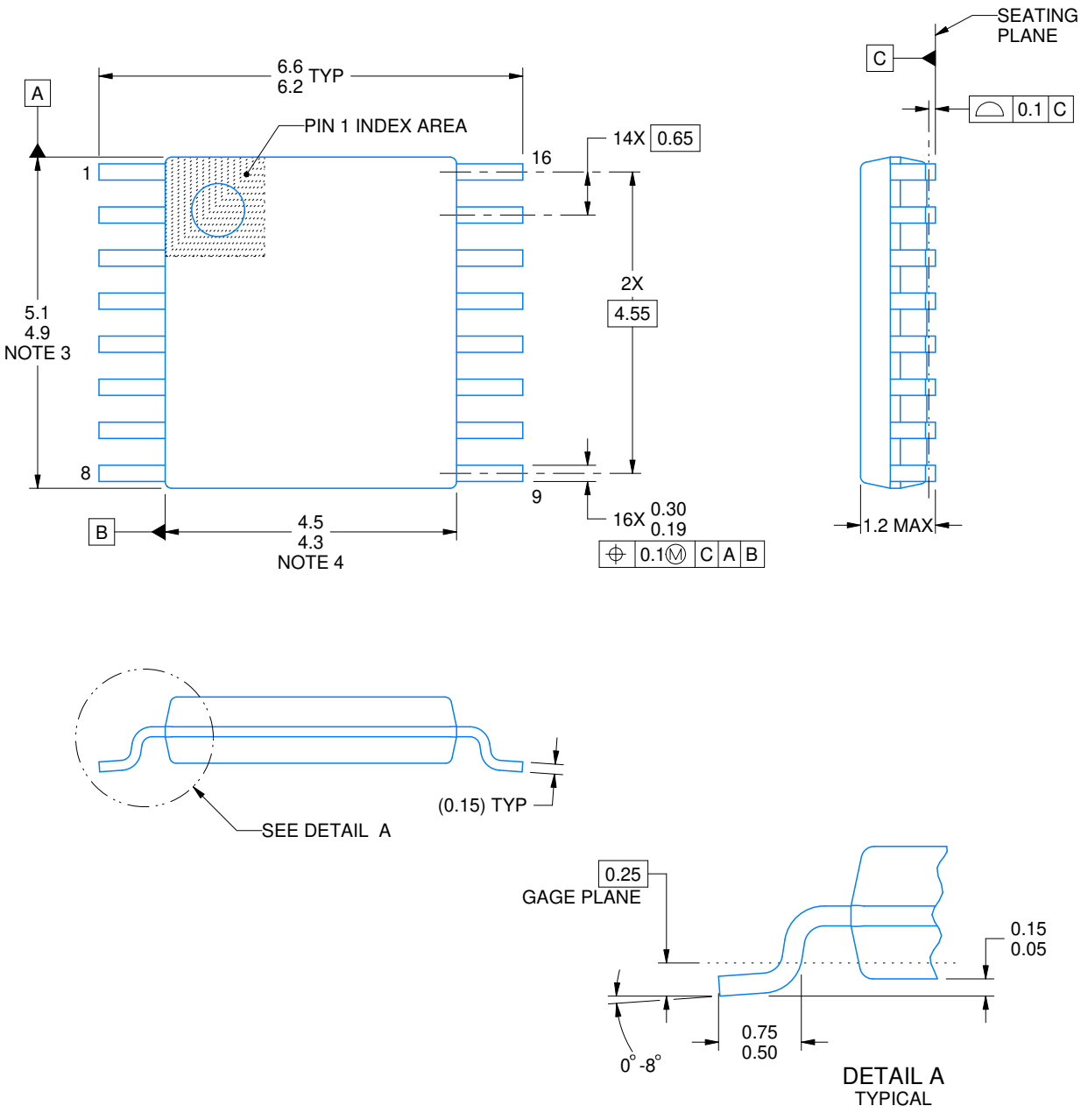
# PACKAGE OUTLINE

## PW0016A



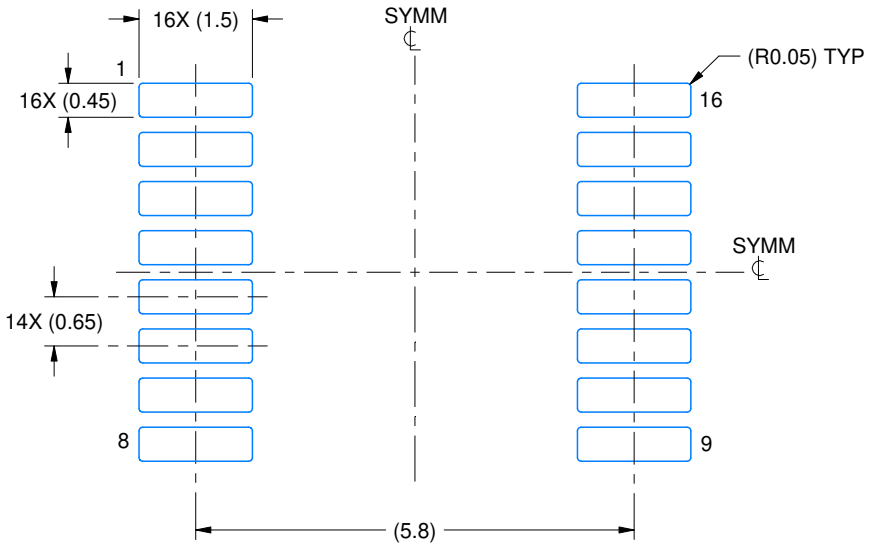
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

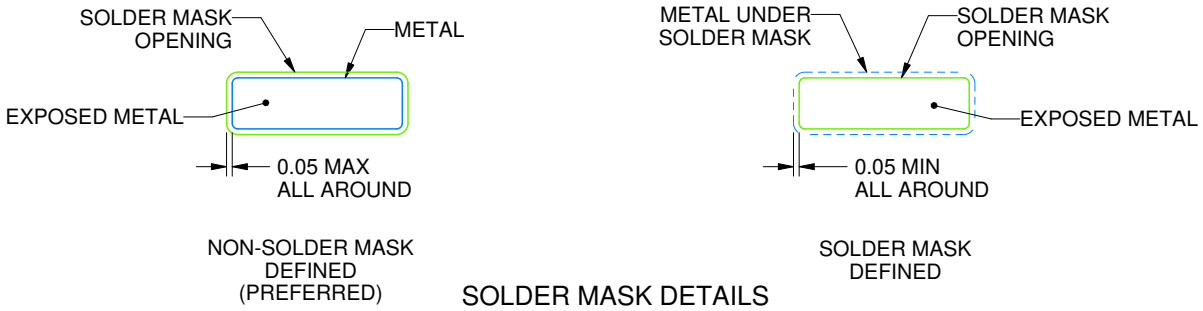



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

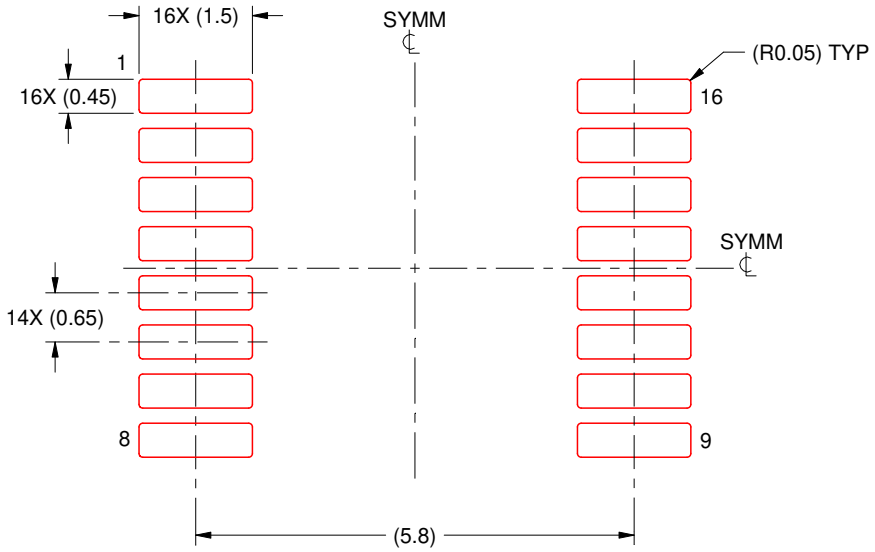



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

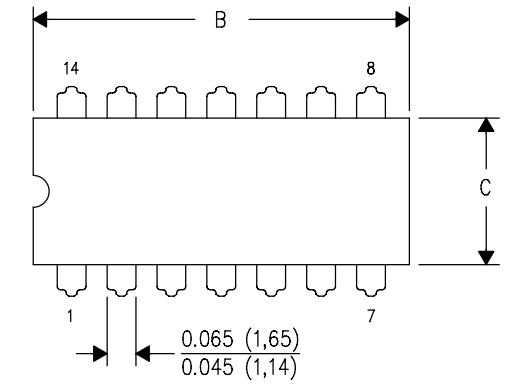
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

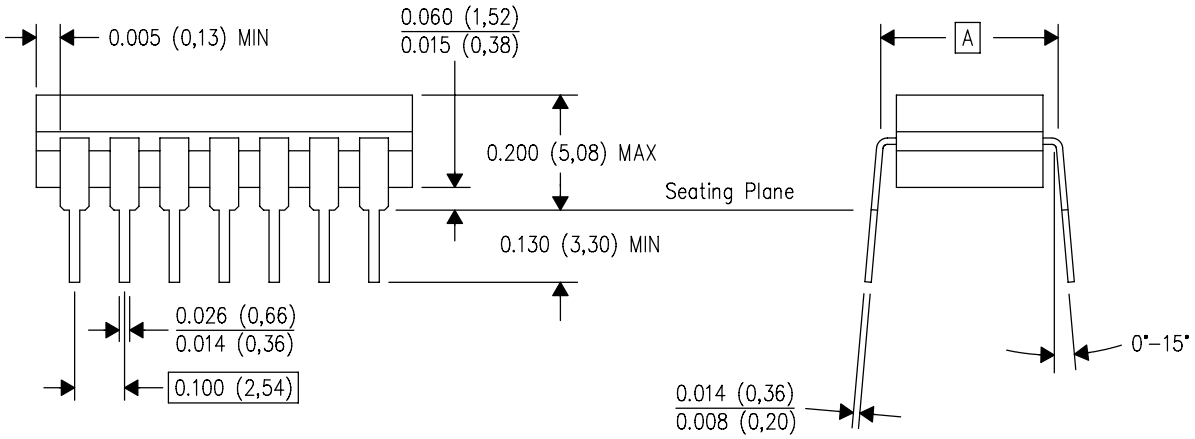
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



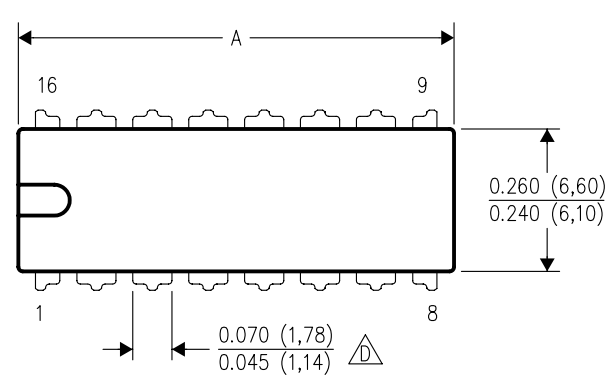

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

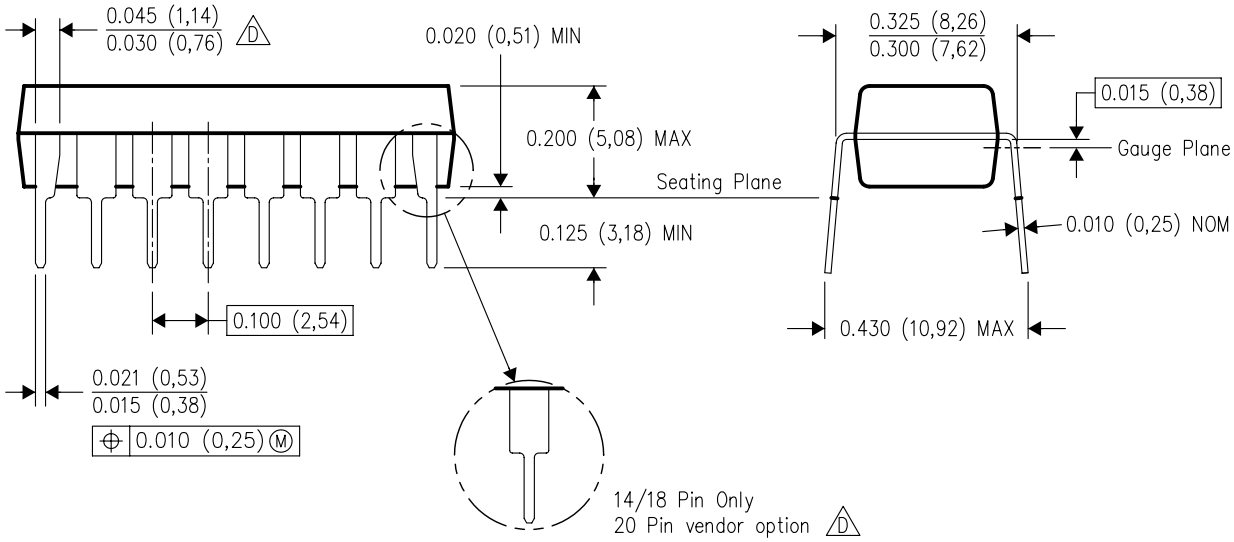
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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