

# 74LVC1G98

## Low-power configurable multiple function gate

Rev. 7 — 6 December 2022

Product data sheet

## 1. General description

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The 74LVC1G98 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to  $V_{CC}$  or GND.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

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- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power dissipation
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1000 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C.

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74LVC1G98GW</a>	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	<a href="#">SOT363-2</a>
<a href="#">74LVC1G98GV</a>	-40 °C to +125 °C	SC-74; TSOP6	plastic surface-mounted package; 6 leads	<a href="#">SOT457</a>
<a href="#">74LVC1G98GM</a>	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	<a href="#">SOT886</a>
<a href="#">74LVC1G98GN</a>	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	<a href="#">SOT1115</a>
<a href="#">74LVC1G98GS</a>	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	<a href="#">SOT1202</a>

### 4. Marking

Table 2. Marking

Type number	Marking code[1]
74LVC1G98GW	V9
74LVC1G98GV	V98
74LVC1G98GM	V9
74LVC1G98GN	V9
74LVC1G98GS	V9

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

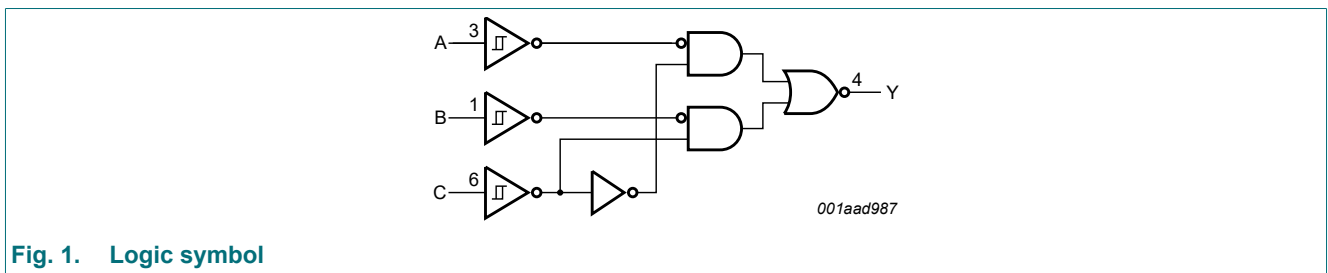
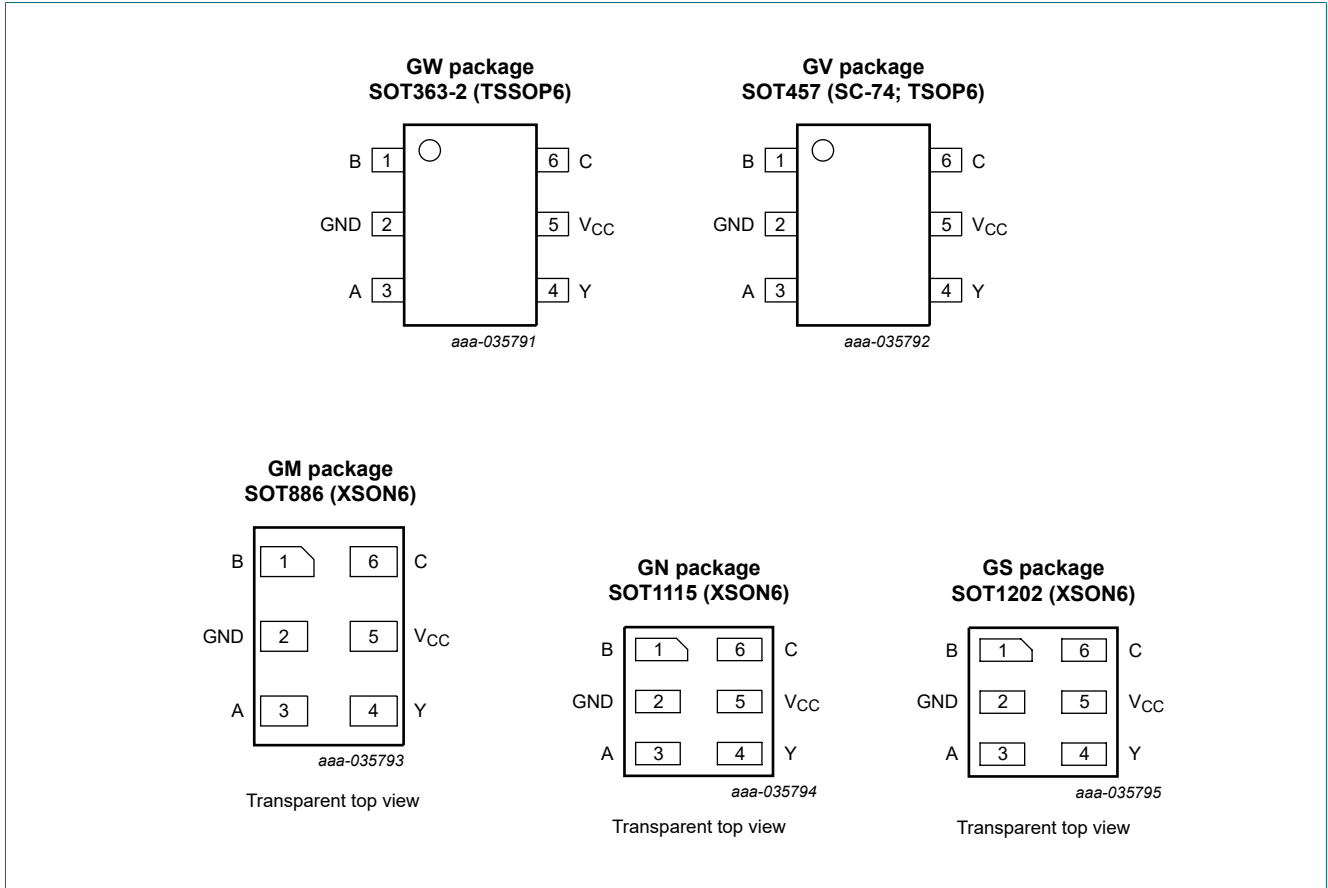


Fig. 1. Logic symbol

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V <sub>CC</sub>	5	supply voltage
C	6	data input

## 7. Functional description

**Table 4. Function table**

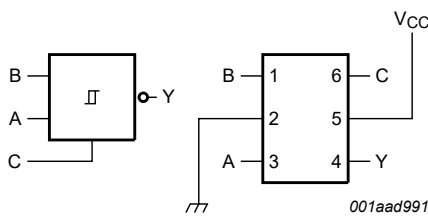
*H = HIGH voltage level; L = LOW voltage level.*

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

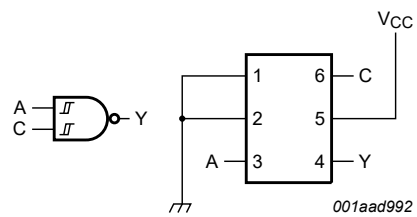
### 7.1. Logic configurations

**Table 5. Function selection table**

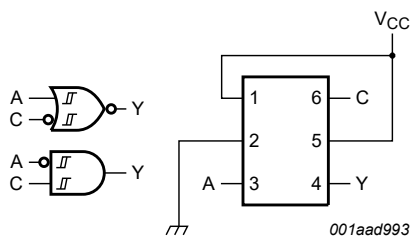
Logic function	Figure
2-input MUX with inverted output	see <a href="#">Fig. 2</a>
2-input NAND	see <a href="#">Fig. 3</a>
2-input NOR with one input inverted	see <a href="#">Fig. 4</a>
2-input AND with one input inverted	see <a href="#">Fig. 4</a>
2-input NAND with one input inverted	see <a href="#">Fig. 5</a>
2-input OR with one input inverted	see <a href="#">Fig. 5</a>
2-input NOR	see <a href="#">Fig. 6</a>
Buffer	see <a href="#">Fig. 7</a>
Inverter	see <a href="#">Fig. 8</a>



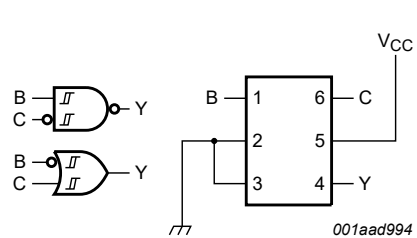
**Fig. 2. 2-input MUX with inverted output**



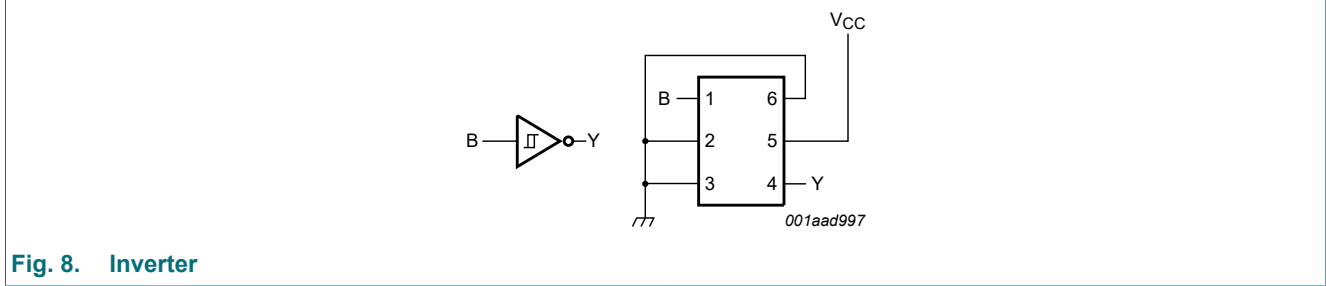
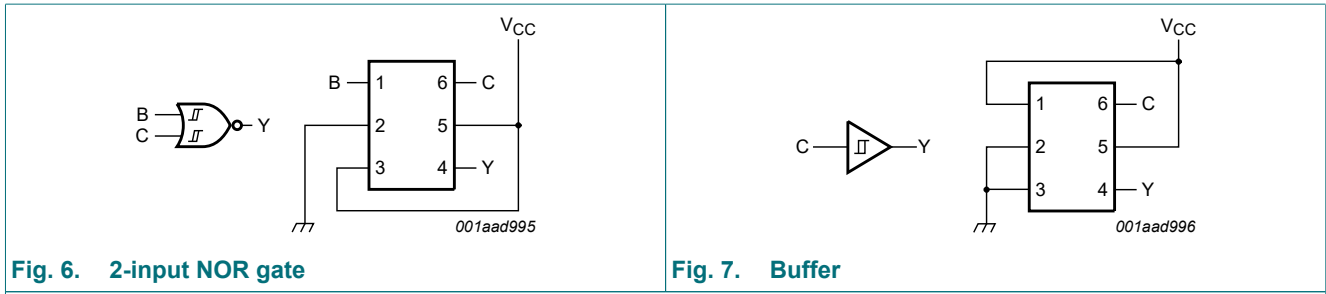
**Fig. 3. 2-input NAND gate**



**Fig. 4. 2-input AND gate with input A inverted or 2-input NOR gate with inverted C input**



**Fig. 5. 2-input OR gate with input B inverted or 2-input NAND gate with input C inverted**



## 8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	Active mode	[1] -0.5	+6.5	V
		Power-down mode; $V_{CC} = 0$ V	[1] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	+100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package:  $P_{tot}$  derates linearly with 3.7 mW/K above 83 °C.

For SOT457 (SC-74; TSOP6) package:  $P_{tot}$  derates linearly with 4.1 mW/K above 89 °C.

For SOT886 (XSON6) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package:  $P_{tot}$  derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

## 9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	Active mode	0	-	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{OL}$	LOW-level output voltage	$V_I = V_{CC}$ or GND						
		$I_O = 100 \mu\text{A}$ ; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.1	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.45	-	0.7	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.3	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.4	-	0.6	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.55	-	0.8	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	-	0.55	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{CC}$ or GND						
		$I_O = -100 \mu\text{A}$ ; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	$V_{CC} - 0.1$	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	-	-	0.95	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	-	-	1.7	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	1.9	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	-	-	2.0	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	-	-	3.4	-	V
$I_I$	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	$\pm 0.1$	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	$\pm 0.1$	$\pm 2$	-	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5$ V or GND; $I_O = 0$ A; $V_{CC} = 1.65$ V to 5.5 V	-	0.1	4	-	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	5	500	-	500	$\mu\text{A}$
$C_I$	input capacitance		-	2.5	-	-	-	pF

[1] Typical values are measured at maximum  $V_{CC}$  and  $T_{amb} = 25$  °C.

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 9 [2]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	6.0	14.4	1.0	18.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	3.5	8.3	0.5	10.4	ns
		V <sub>CC</sub> = 2.7 V	0.5	4.2	8.5	0.5	10.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	3.8	6.3	0.5	7.9	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	3.0	5.1	0.5	6.4	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = GND to V <sub>CC</sub> [3]	-	20	-	-	-	pF

[1] Typical values are measured at nominal V<sub>CC</sub> and at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

### 11.1. Waveform and test circuit

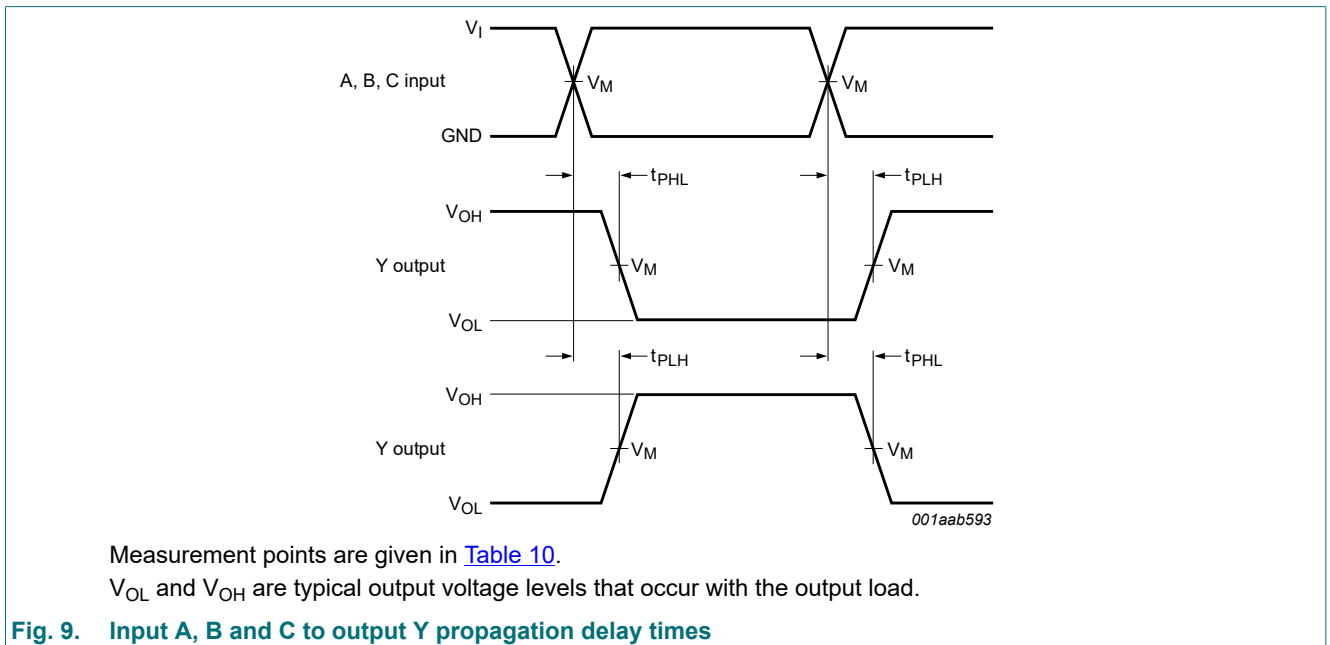
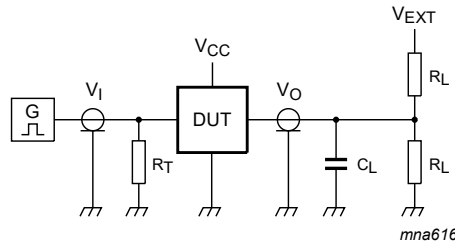


Table 10. Measurement points

Supply voltage	Input		Output
$V_{CC}$	$V_M$	$V_I$	$V_M$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$



Measurement points are given in [Table 11](#).

Definitions test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 11. Measurement points

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open



## 12. Transfer characteristics

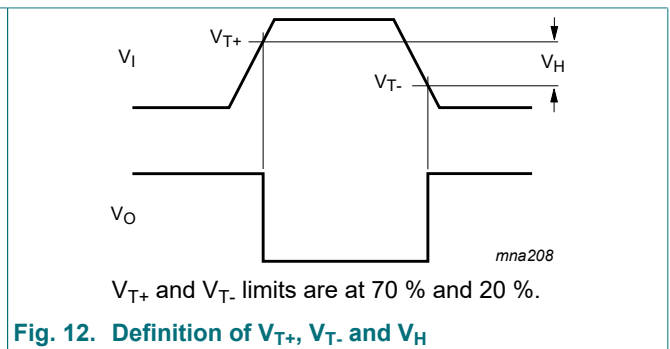
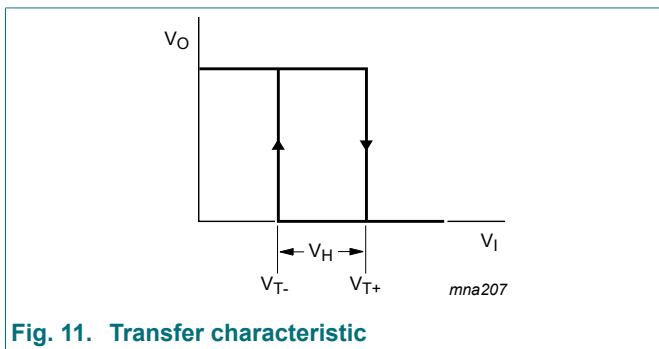
**Table 12. Transfer characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>T+</sub>	positive-going threshold voltage	see <a href="#">Fig. 11</a> , <a href="#">Fig. 12</a> , <a href="#">Fig. 13</a> and <a href="#">Fig. 14</a>						
		V <sub>CC</sub> = 1.8 V	0.70	1.02	1.20	0.67	1.20	V
		V <sub>CC</sub> = 2.3 V	1.11	1.42	1.60	1.08	1.60	V
		V <sub>CC</sub> = 3.0 V	1.50	1.79	2.00	1.47	2.00	V
		V <sub>CC</sub> = 4.5 V	2.16	2.52	2.74	2.13	2.74	V
		V <sub>CC</sub> = 5.5 V	2.61	2.99	3.33	2.58	3.33	V
V <sub>T-</sub>	negative-going threshold voltage	see <a href="#">Fig. 11</a> , <a href="#">Fig. 12</a> , <a href="#">Fig. 13</a> and <a href="#">Fig. 14</a>						
		V <sub>CC</sub> = 1.8 V	0.30	0.53	0.72	0.30	0.75	V
		V <sub>CC</sub> = 2.3 V	0.58	0.77	1.00	0.58	1.03	V
		V <sub>CC</sub> = 3.0 V	0.80	1.04	1.30	0.80	1.33	V
		V <sub>CC</sub> = 4.5 V	1.21	1.55	1.90	1.21	1.93	V
		V <sub>CC</sub> = 5.5 V	1.45	1.86	2.29	1.45	2.32	V
V <sub>H</sub>	hysteresis voltage	(V <sub>T+</sub> - V <sub>T-</sub> ); see <a href="#">Fig. 11</a> , <a href="#">Fig. 12</a> , <a href="#">Fig. 13</a> and <a href="#">Fig. 14</a>						
		V <sub>CC</sub> = 1.8 V	0.30	0.48	0.62	0.23	0.62	V
		V <sub>CC</sub> = 2.3 V	0.40	0.64	0.80	0.34	0.80	V
		V <sub>CC</sub> = 3.0 V	0.50	0.75	1.00	0.44	1.00	V
		V <sub>CC</sub> = 4.5 V	0.71	0.97	1.20	0.65	1.20	V
		V <sub>CC</sub> = 5.5 V	0.71	1.13	1.40	0.65	1.40	V

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

### 12.1. Waveforms transfer characteristics



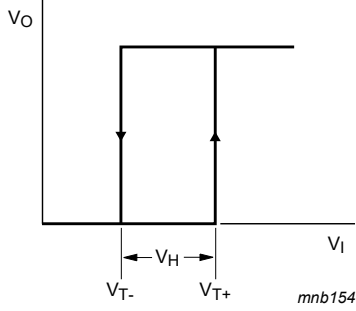
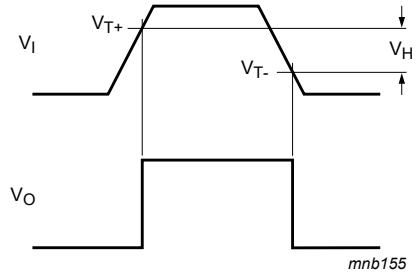


Fig. 13. Transfer characteristic



$V_{T+}$  and  $V_{T-}$  limits are at 70 % and 20 %.

Fig. 14. Definition of  $V_{T+}$ ,  $V_{T-}$  and  $V_H$

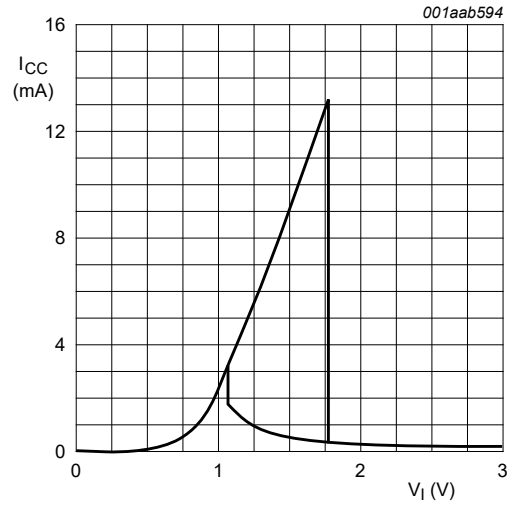


Fig. 15. Typical 74LVC1G98 transfer characteristic;  $V_{CC} = 3.0$  V

### 13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

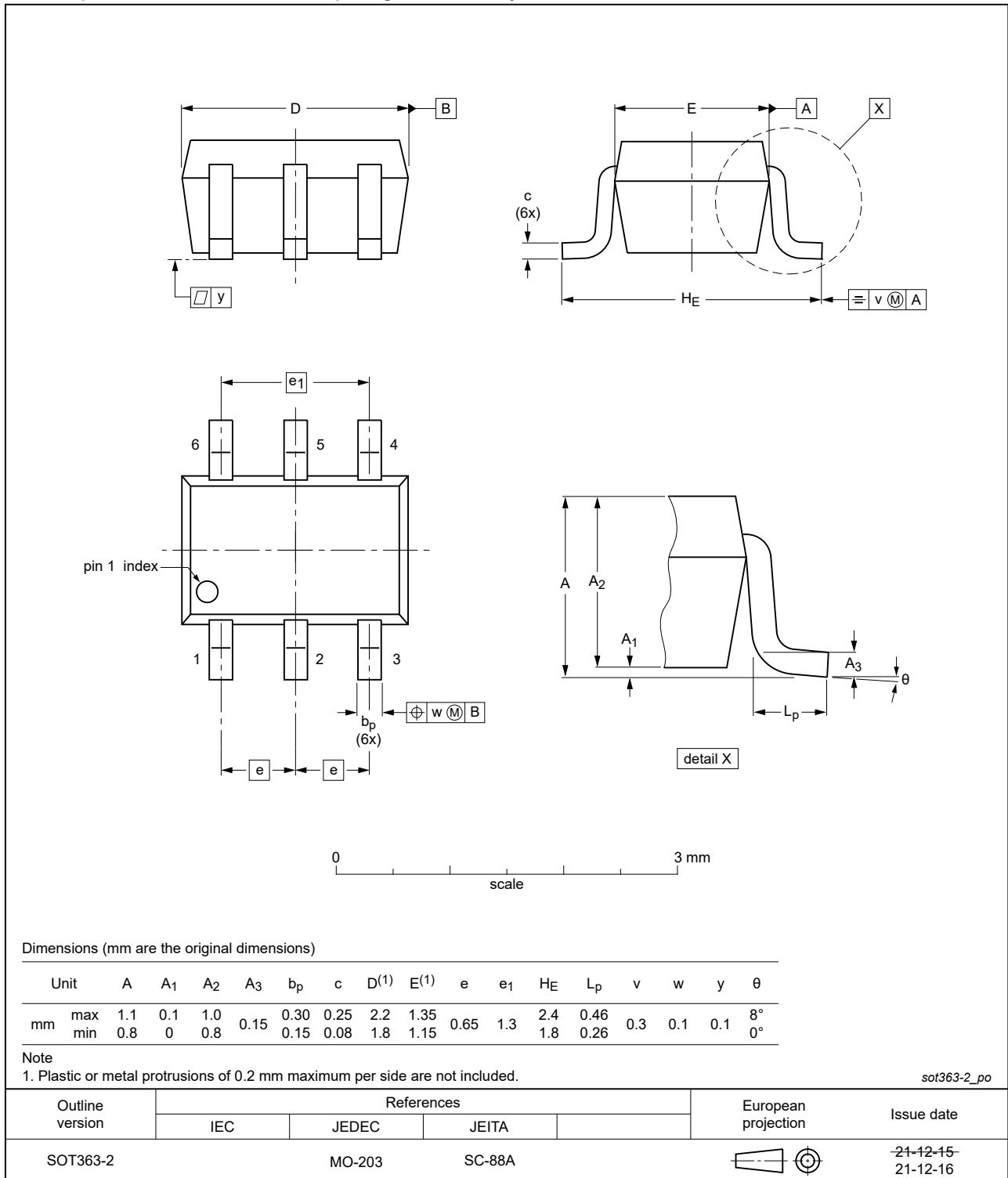


Fig. 16. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads

SOT457

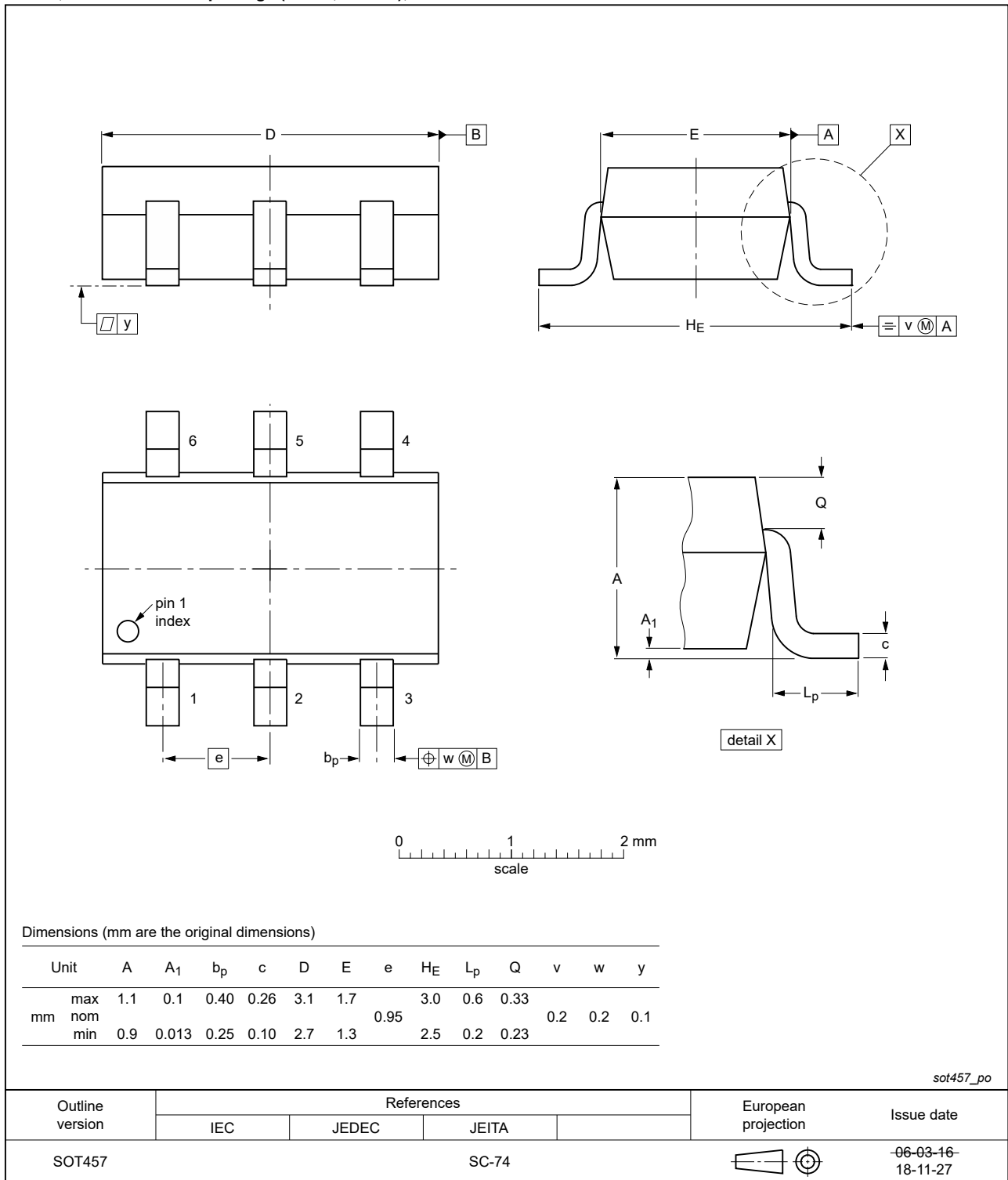


Fig. 17. Package outline SOT457 (SC-74; TSOP6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

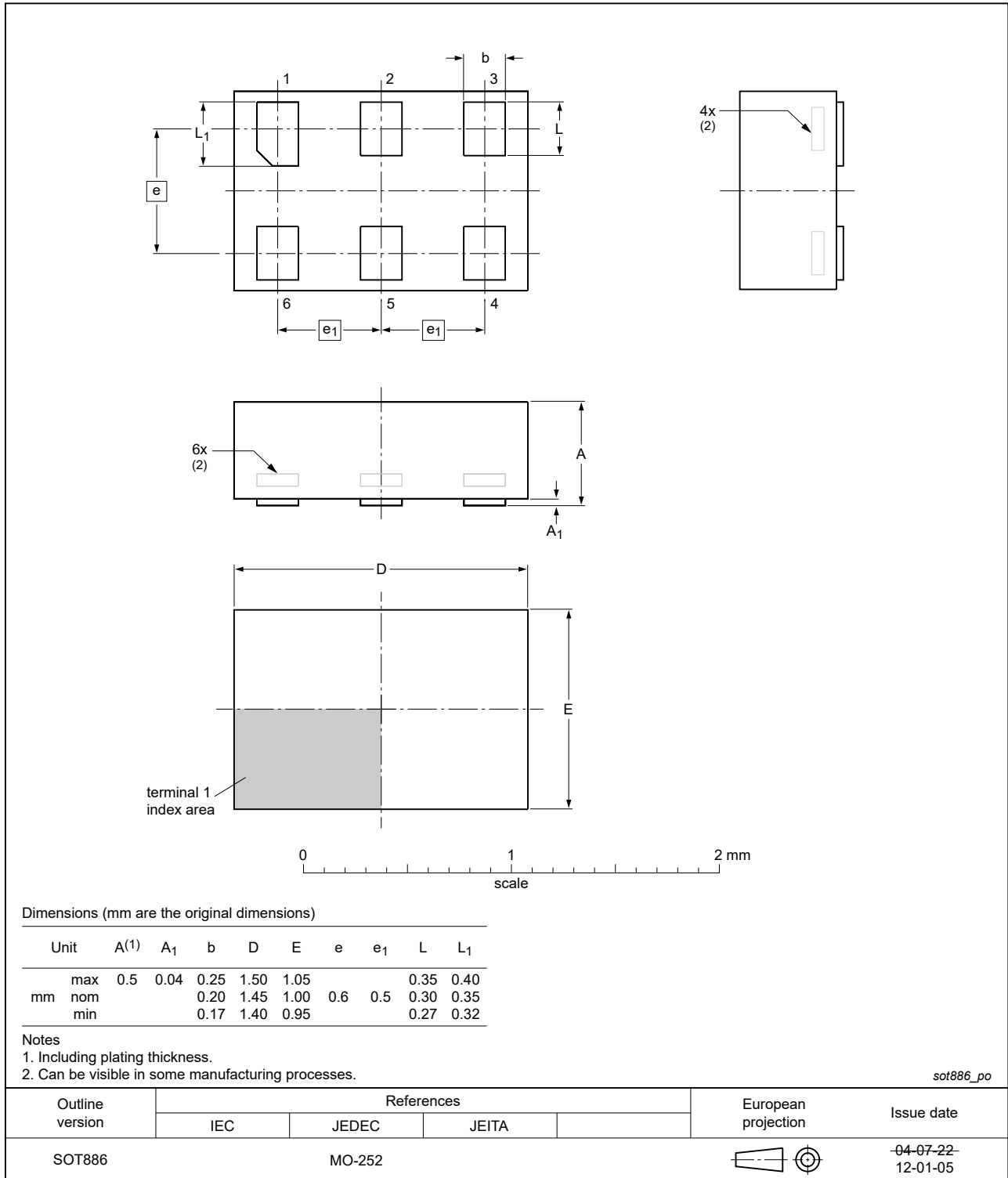
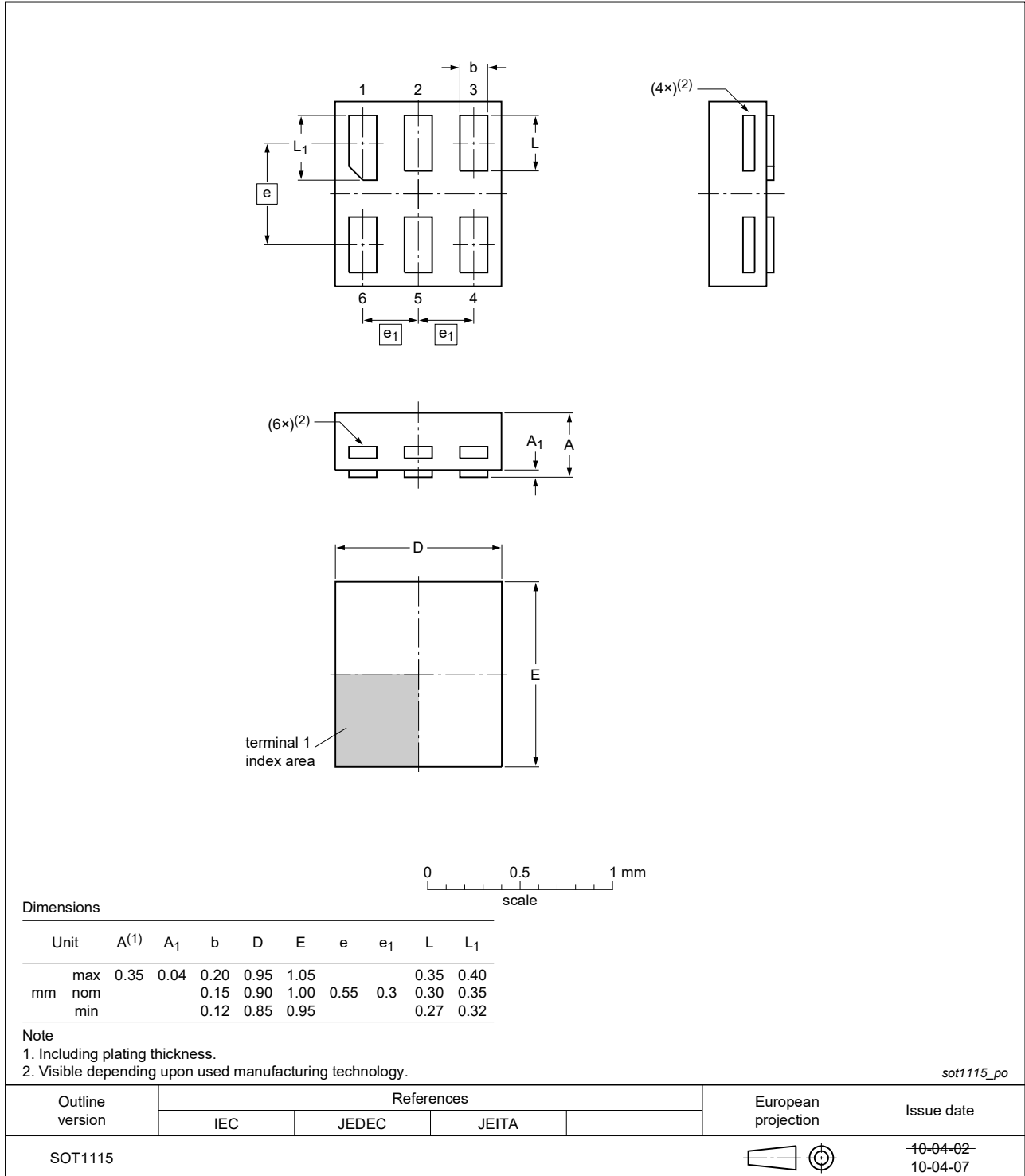


Fig. 18. Package outline SOT886 (XSON6)

**XSON6: extremely thin small outline package; no leads;**  
**6 terminals; body 0.9 x 1.0 x 0.35 mm**

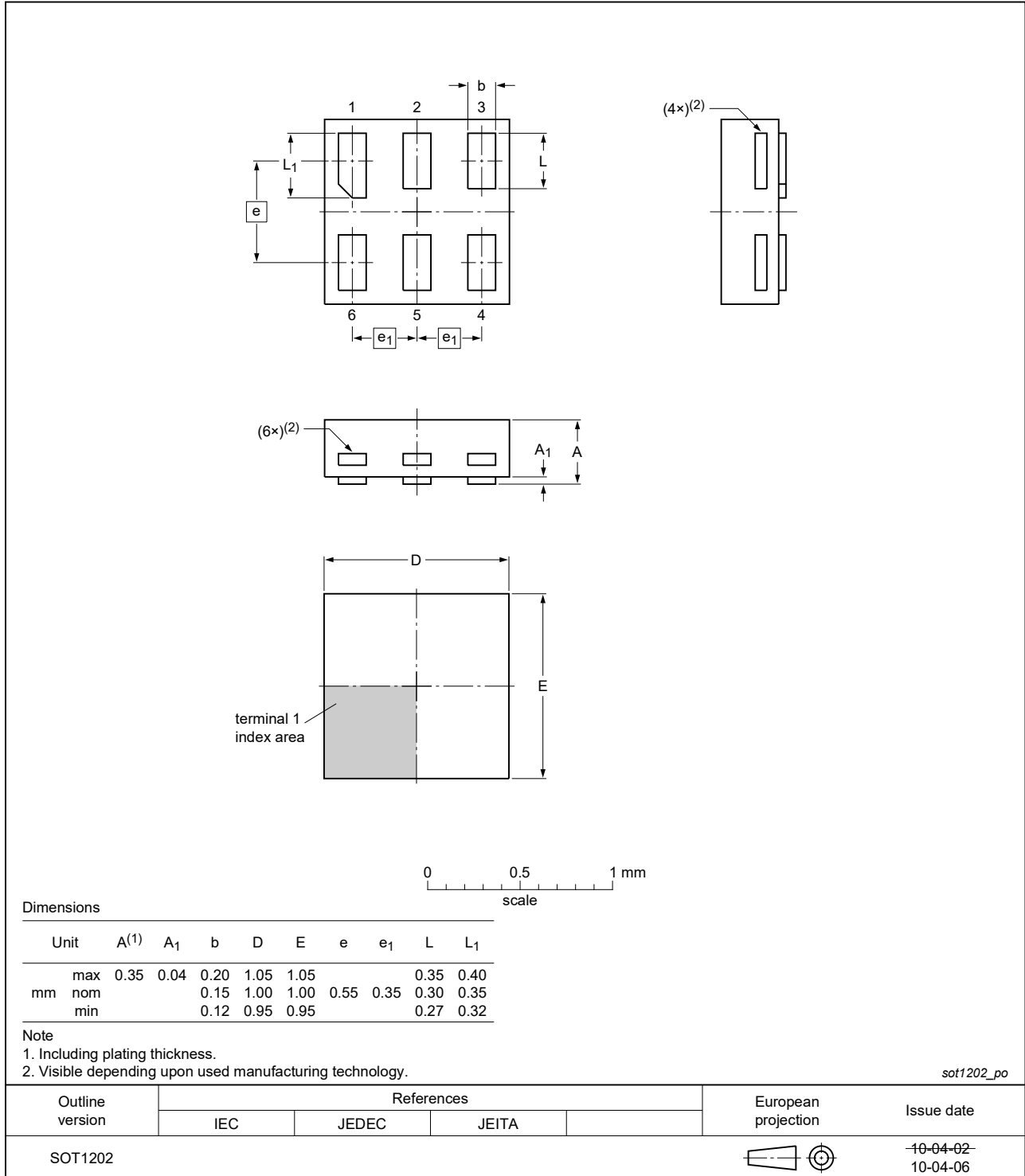
SOT1115



**Fig. 19. Package outline SOT1115 (XSON6)**

**XSON6: extremely thin small outline package; no leads;  
6 terminals; body 1.0 x 1.0 x 0.35 mm**

SOT1202



**Fig. 20. Package outline SOT1202 (XSON6)**

## 14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G98 v.7	20221206	Product data sheet	-	74LVC1G98 v.6
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a> updated.</li> </ul>			
74LVC1G98 v.6	20221121	Product data sheet	-	74LVC1G98 v.5
Modifications:	<ul style="list-style-type: none"> <li>Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6).</li> </ul>			
74LVC1G98 v.5	20210430	Product data sheet	-	74LVC1G98 v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74LVC1G98GF (SOT891/XSON6) removed.</li> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 17</a>: Package outline drawing SOT457 (SC-74; TSOP6) updated.</li> </ul>			
74LVC1G98 v.4	20161219	Product data sheet	-	74LVC1G98 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 8</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC1G98 v.3	20111201	Product data sheet	-	74LVC1G98 v.2
74LVC1G98 v.2	20111201	Product data sheet	-	74LVC1G98 v.1
74LVC1G98 v.1	20101221	Product data sheet	-	-



## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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