

Bi-directional ESD / Transient Voltage Suppressor

DESCRIPTIONS

The TESDL5V0B45P1M3 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

TESDL5V0B45P1M3 is a unique design which includes proprietary clamping cells in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

The TESDL5V0B45P1M3 may be used to provide ESD protection up to $\pm 30\text{kV}$ (contact and air discharge) according to IEC 61000-4-2, and withstand peak pulse current up to 12A (8/20 μs) according to IEC 61000-4-5.


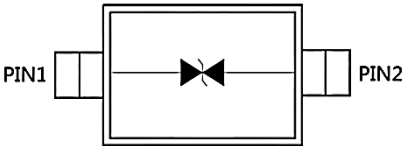

FEATURES

- ESD protect for 1 line with bidirectional
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air), $\pm 30\text{kV}$ (contact) IEC 61000-4-5 (Lightning) 12A (8/20 μs)
- Suitable for 5V and below, operating voltage applications
- Small package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

APPLICATION

- Computers and peripherals
- Power supply protection
- Portable devices
- Audio and video equipment
- Notebooks, desktops, and servers



PACKAGE: SOD-323	PIN CONFIGURATION		CIRCUIT DIAGRAM
			
	PIN 1	Anode 1	
	PIN 2	Anode 2	

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power ($t_p = 8/20\mu\text{s}$)	P_{PK}	130	W
Peak pulse current ($t_p = 8/20\mu\text{s}$)	I_{PP}	12	A
ESD according to IEC 61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC 61000-4-2 contact discharge		± 30	kV
Operating junction temperature range	T_J	-55 to +150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^\circ\text{C}$

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	$I_R = 1\text{mA}$, $T_J = 25^\circ\text{C}$	V_{BR}	5.5	-	9.5	V
Reverse leakage current	$V_{RWM} = 5\text{V}$, $T_J = 25^\circ\text{C}$	I_R	-	-	100	nA
Clamping voltage ⁽¹⁾	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$	V_C	-	-	10	V
	$I_{PP} = 12\text{A}$, $t_p = 8/20\mu\text{s}$		-	-	14	V
Junction capacitance	1MHz, $V_R = 0\text{V}$	C_J	-	36	45	pF

Notes:

1. Non-repetitive current pulse, according to IEC 61000-4-5.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TESDL5V0B45P1M3 RWG	SOD-323	3,000 / 7" Reel

CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

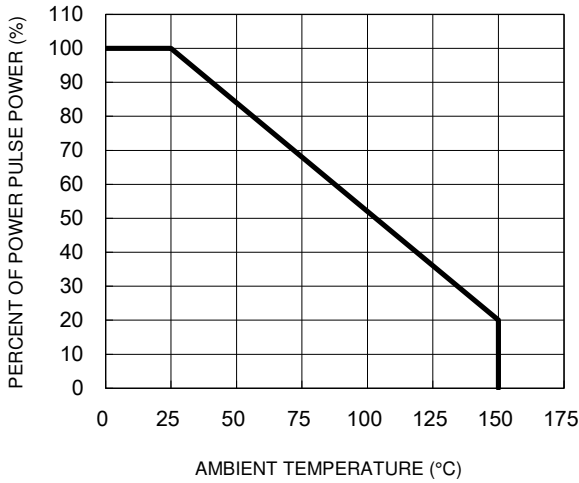


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

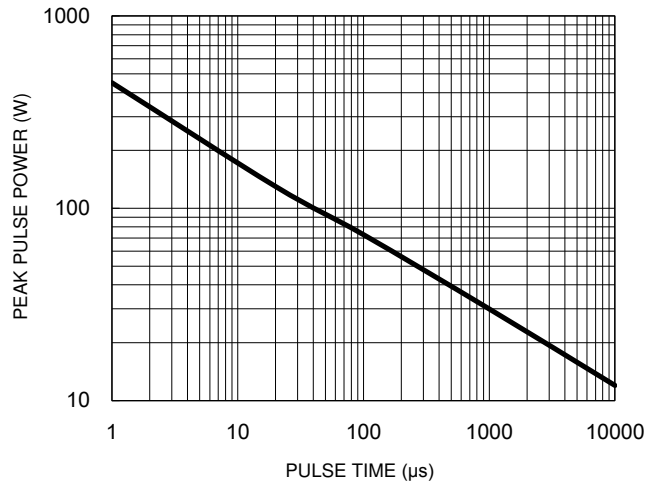


Fig.3 Clamping Voltage vs. Peak Pulse Current

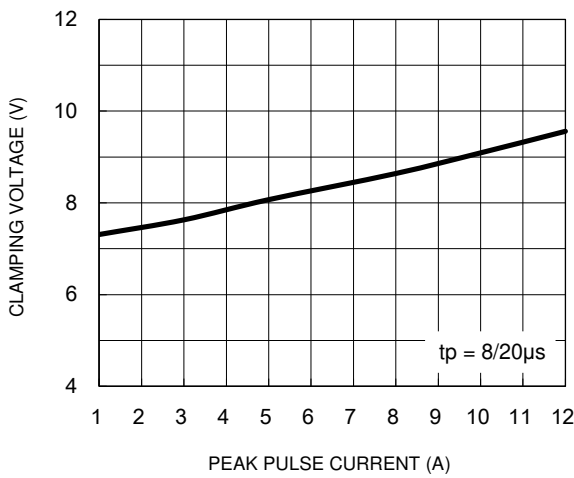


Fig.4 Capacitance vs. Reverse Voltage

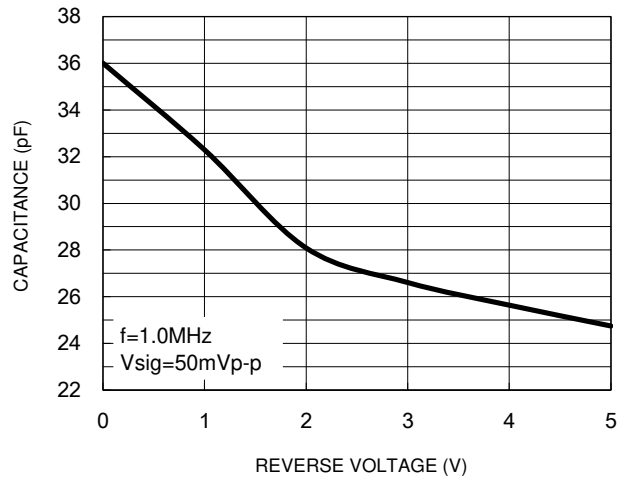
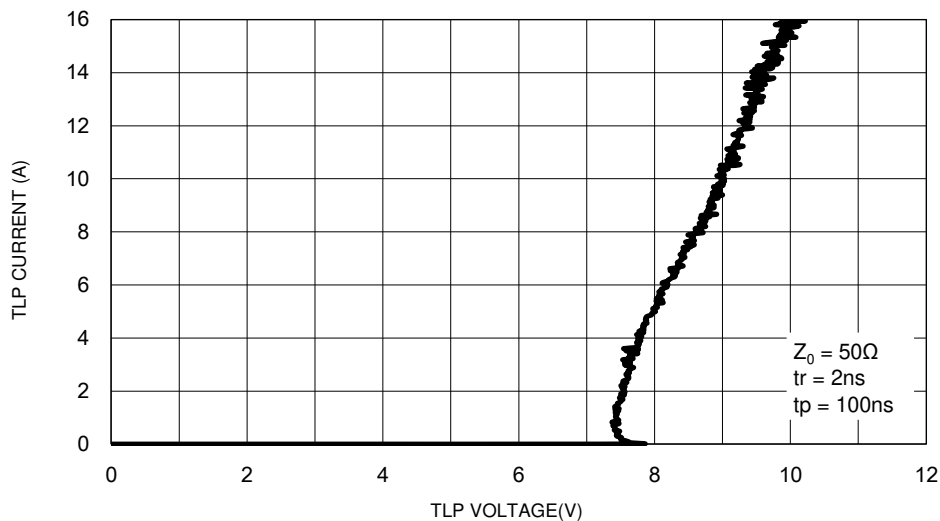


Fig.5 TLP Curve



CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.6 8/20 μs pulse waveform

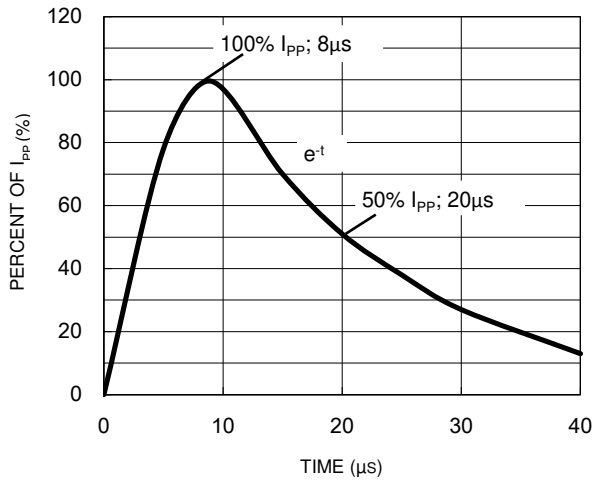
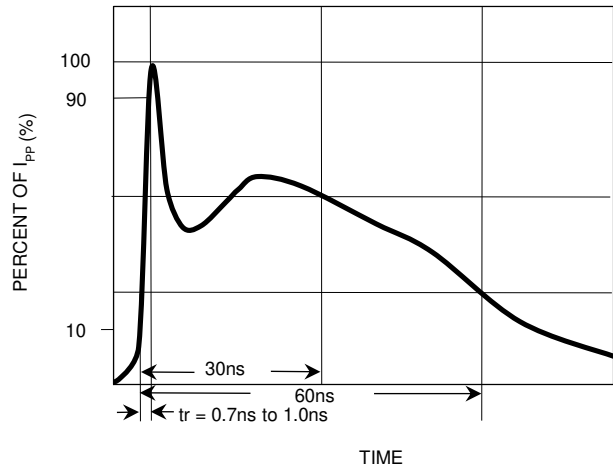


Fig.7 ESD pulse waveform



APPLICATION INFORMATION

Device Connection

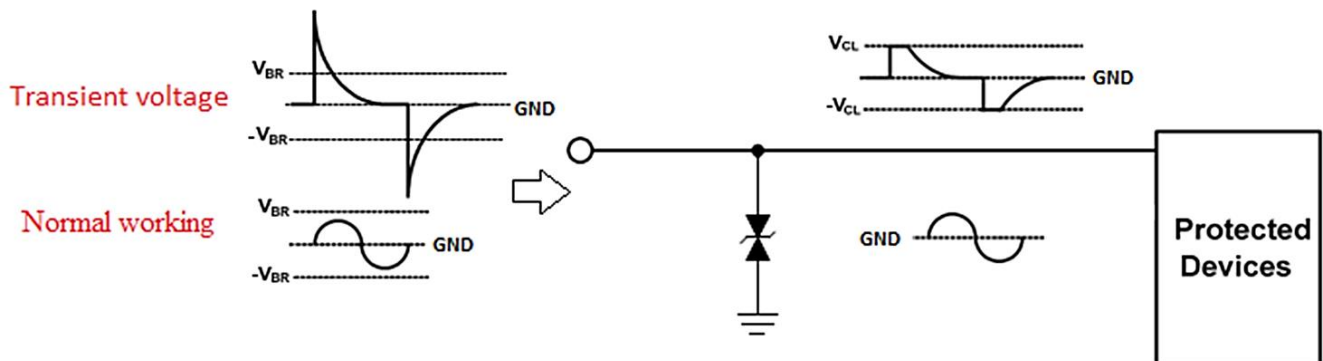
The TESDL5V0B45P1M3 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.

The usage of the TESDL5V0B45P1M3 is shown in Fig1. Protected line, such as data line, control line, or power line. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDL5V0B45P1M3 should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

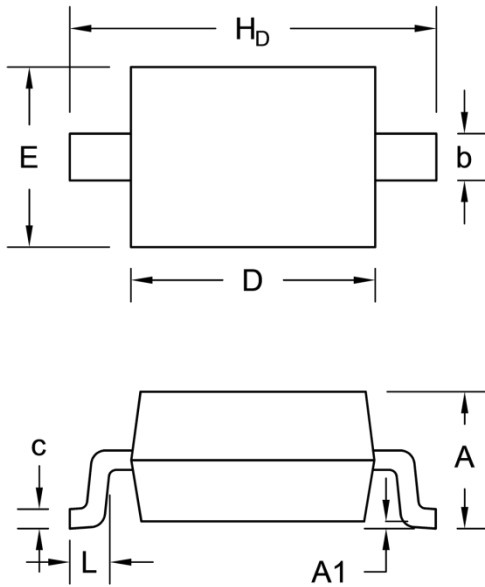
- Let the path length between the protected lines and the TESDL5V0B45P1M3 minimize.
- Place the TESDL5V0B45P1M3 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

Fig.1 ESD protection by TESDL5V0B45P1M3



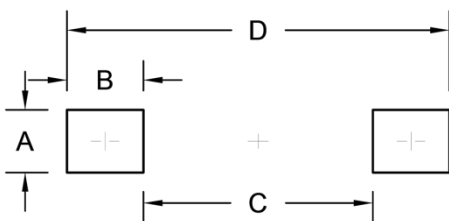
PACKAGE OUTLINE DIMENSIONS

SOD-323



DIM.	Unit (mm)		Unit (inch)	
	Min.	Max.	Min.	Max.
A	0.800	1.100	0.031	0.043
A1	0.000	0.100	0.000	0.004
b	0.250	0.400	0.010	0.016
c	0.090	0.180	0.004	0.007
D	1.600	1.800	0.063	0.071
H_D	2.300	2.800	0.091	0.110
E	1.150	1.350	0.045	0.053
L	0.100	0.300	0.004	0.012

SUGGESTED PAD LAYOUT

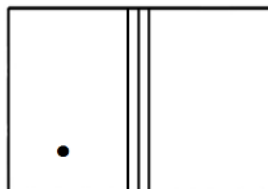


Symbol	Unit (mm)	Unit (inch)
A	0.49	0.019
B	0.60	0.024
C	1.80	0.071
D	3.00	0.118

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

MARKING DIAGRAM



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