DRV8340-Q1 12-V / 24-V Automotive Gate Driver Unit (GDU) with Independent Half Bridge Control

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C ≤ T_A ≤ 125°C
- Three independent half-bridge gate driver
  - Dedicated source (SHx) and drain (DLx) pins to support independent MOSFET control
  - Drives 3 high-side and 3 low-side N-channel MOSFETs (NMOS)
- Smart gate drive architecture
  - Adjustable slew rate control
  - 1.5-mA to 1-A peak source current
  - 3-mA to 2-A peak sink current
- Charge-pump of gate driver for 100% Duty Cycle
- SPI (S) and hardware (H) interface available
- 6x, 3x, 1x, and independent PWM modes
- Supports 3.3-V, and 5-V logic inputs
- Charge pump output can be used to drive the reverse supply protection MOSFET
- Linear voltage regulator, 3.3 V, 30 mA
- Integrated protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Short to battery (SHT_BAT)
  - Short to ground (SHT_GND)
  - MOSFET overcurrent protection (OCP)
  - Gate driver fault (GDF)
  - Thermal warning and shutdown (OTW/OTSD)
  - Fault condition indicator (nFAULT)

2 Applications

- 12-V and 24-V Automotive Motor-Control Applications
  - BLDC and BDC motor modules
  - Fans and blowers
  - Fuel and water pumps
  - Solenoid drive

3 Description

The DRV8340-Q1 device is an integrated gate driver for three-phase applications. The device provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The dedicated Source and Drain pins enable the independent MOSFET control for solenoid application. The DRV8340-Q1 generates the correct gate drive voltages using an integrated charge pump sufficient for the high-side MOSFETs and a linear regulator for the low-side MOSFETs. The Smart Gate Drive architecture supports peak gate drive currents up to 1-A source and 2-A. The DRV8340-Q1 can operate from a single power supply and supports a wide input supply range of 5.5 to 60 V for the gate driver.

The 6x, 3x, 1x, and independent input PWM modes allow for simple interfacing to controller circuits. The configuration settings for the gate driver and device are highly configurable through the SPI or hardware (H/W) interface.

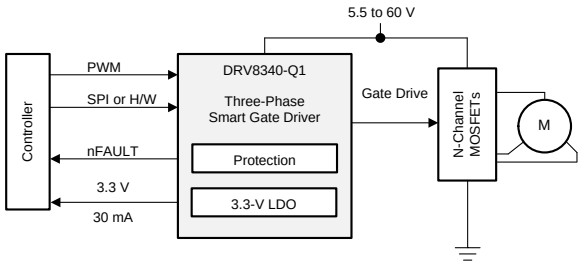
A low-power sleep mode is provided to achieve low quiescent current. Internal protection functions are provided for undervoltage lockout, charge pump fault, MOSFET overcurrent, MOSFET short circuit, phase-node short to supply and ground, gate driver fault, and overtemperature. Fault conditions are indicated on the nFAULT pin with details through the device registers for the SPI device variant.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8340-Q1	HTQFP (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2019	*	Initial Release

PP

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5 Device Comparison Table

DEVICE	VARIANT(1)	INTERFACE(1)
DRV8340-Q1	DRV8340H	Hardware
	DRV8340S	SPI

(1) For more information on the device name and device options, see the *Device Nomenclature* section.

6 Pin Configuration and Functions

DRV8340H PHP PowerPAD™ Package
48-Pin HTQFP With Exposed Thermal Pad
Top View

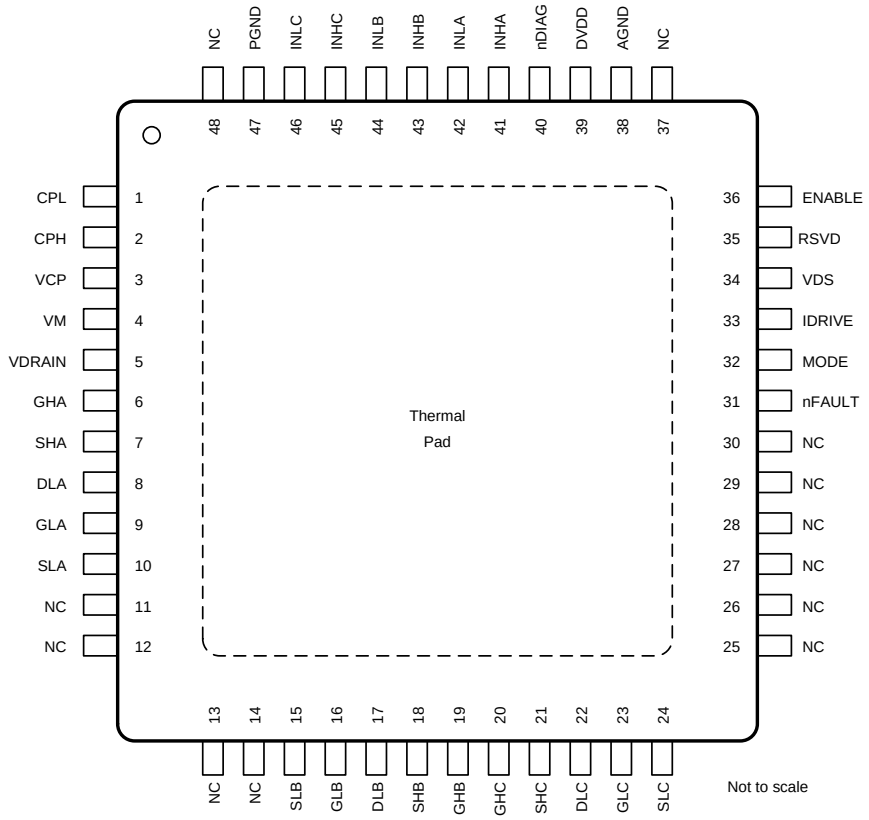

Table 1. Pin Functions—DRV8340H

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CPL	PWR	Charge pump switching node. Connect a flying capacitor between the CPH and CPL pins
2	CPH	PWR	Charge pump switching node. Connect a flying capacitor between the CPH and CPL pins
3	VCP	PWR	Charge pump output. Connect a bypass capacitor between the VCP and VM pins
4	VM	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect bypass capacitors VM and PGND pins
5	VDRAIN	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains
6	GHA	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET

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Table 1. Pin Functions—DRV8340H (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
7	SHA	I	High-side source sense input. Connect to the high-side power MOSFET source. If high-side power MOSFET is not used, connect to GND
8	DLA	I	Low-side MOSFET drain sense input. Connect to the low-side MOSFET drain
9	GLA	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
10	SLA	I	Low-side source sense input. Connect to the low-side power MOSFET source
11	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
12	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
13	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
14	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
15	SLB	I	Low-side source sense input. Connect to the low-side power MOSFET source
16	GLB	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
17	DLB	I	Low-side MOSFET drain sense input. Connect to the low-side MOSFET drain
18	SHB	I	High-side source sense input. Connect to the high-side power MOSFET source. If high-side power MOSFET is not used, connect to GND
19	GHB	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
20	GHC	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
21	SHC	I	High-side source sense input. Connect to the high-side power MOSFET source. If high-side power MOSFET is not used, connect to GND
22	DLC	I	Low-side MOSFET drain sense input. Connect to the low-side MOSFET drain
23	GLC	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
24	SLC	I	Low-side source sense input. Connect to the low-side power MOSFET source
25	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
26	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
27	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
28	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
29	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
30	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
31	nFAULT	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor
32	MODE	I	PWM input mode setting. This pin is a 7-level input pin set by an external resistor
33	IDRIVE	I	Gate drive output current setting. This pin is a 7-level input pin set by an external resistor
34	VDS	I	VDS monitor trip point setting. This pin is a 7-level input pin set by an external resistor
35	RSVD	I	Reserved. Leave open.
36	ENABLE	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 20-μs (typ) low pulse can be used to reset fault conditions
37	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
38	AGND	PWR	Device analog ground. Connect to system ground
39	DVDD	PWR	3.3-V internal regulator output. Connect a bypass capacitor between the DVDD and AGND pins. This regulator can externally source up to 30 mA.
40	nDIAG	I	Control pin for open load diagnostic and offline short-to-battery and short-to-ground diagnostic. To enable the diagnostics at device power-up, do not connect this pin (or tie it to ground). To disable the diagnostics, connect this pin to the DVDD pin.
41	INHA	I	High-side gate driver control input. This pin controls the output of the high-side gate driver
42	INLA	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver
43	INHB	I	High-side gate driver control input. This pin controls the output of the high-side gate driver
44	INLB	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver
45	INHC	I	High-side gate driver control input. This pin controls the output of the high-side gate driver
46	INLC	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver
47	PGND	PWR	Device power ground. Connect to system ground
48	NC	NC	No connect. Do not connect anything to this pin
—	Thermal Pad	PWR	Must be connected to ground

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DRV8340S PHP PowerPAD™ Package
48-Pin HTQFP With Exposed Thermal Pad
Top View

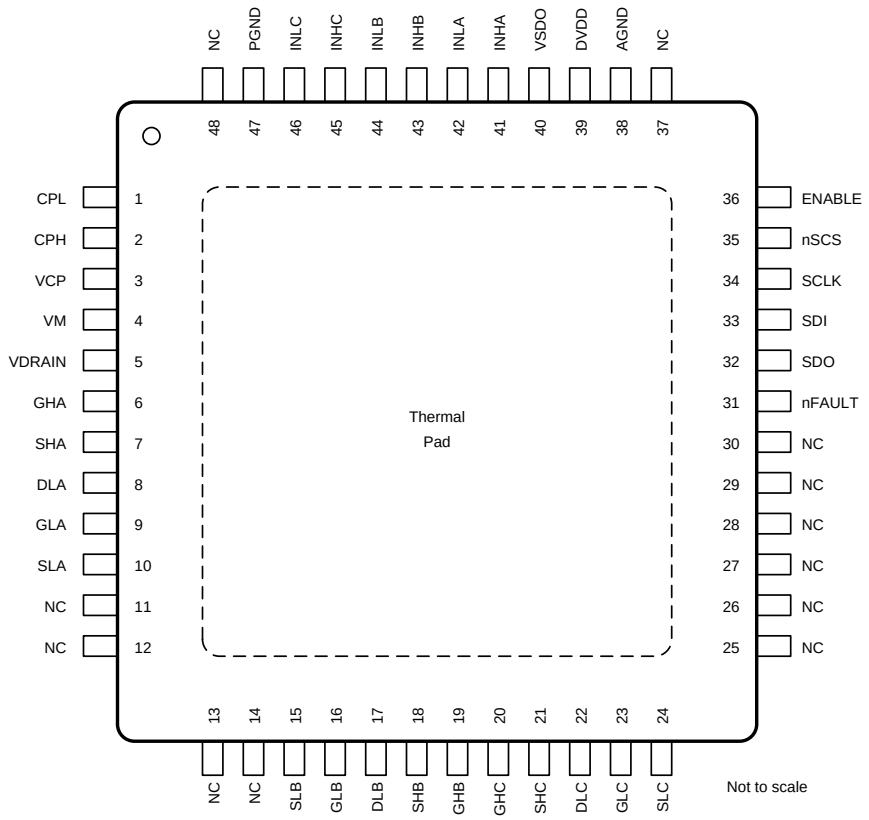

Table 2. Pin Functions—DRV8340S

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CPL	PWR	Charge pump switching node. Connect a flying capacitor between the CPH and CPL pins
2	CPH	PWR	Charge pump switching node. Connect a flying capacitor between the CPH and CPL pins
3	VCP	PWR	Charge pump output. Connect a bypass capacitor between the VCP and VM pins
4	VM	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect bypass capacitors between the VM and PGND pins
5	VDRAIN	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains
6	GHA	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
7	SHA	I	High-side source sense input. Connect to the high-side power MOSFET source. If high-side power MOSFET is not used, connect to GND
8	DLA	I	Low-side MOSFET drain sense input. Connect to the low-side MOSFET drain
9	GLA	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
10	SLA	I	Low-side source sense input. Connect to the low-side power MOSFET source
11	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
12	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
13	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
14	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
15	SLB	I	Low-side source sense input. Connect to the low-side power MOSFET source

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Table 2. Pin Functions—DRV8340S (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
16	GLB	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
17	DLB	I	Low-side MOSFET drain sense input. Connect to the low-side MOSFET drain
18	SHB	I	High-side source sense input. Connect to the high-side power MOSFET source. If high-side power MOSFET is not used, connect to GND
19	GHB	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
20	GHC	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
21	SHC	I	High-side source sense input. Connect to the high-side power MOSFET source. If high-side power MOSFET is not used, connect to GND
22	DLC	I	Low-side MOSFET drain sense input. Connect to the low-side MOSFET drain
23	GLC	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
24	SLC	I	Low-side source sense input. Connect to the low-side power MOSFET source
25	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
26	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
27	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
28	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
29	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
30	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
31	nFAULT	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor
32	SDO	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin. VSDO determines logic level on the output
33	SDI	I	Serial data input. Data is captured on the falling edge of the SCLK pin
34	SCLK	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin
35	nSCS	I	Serial chip select. A logic low on this pin enables serial interface communication
36	ENABLE	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 20-µs (typ) low pulse can be used to reset fault conditions
37	NC	NC	No internal connection. This pin can be left floating or connected to system ground.
38	AGND	PWR	Device analog ground. Connect to system ground
39	DVDD	PWR	3.3-V internal regulator output. Connect a bypass capacitor between the DVDD and AGND pins. This regulator can externally source up to 30 mA.
40	VSDO	PWR	Supply pin for SDO output. Connect to 5-V or 3.3-V depending on the desired logic level. Connect a bypass capacitors between VSDO and AGND
41	INHA	I	High-side gate driver control input. This pin controls the output of the high-side gate driver
42	INLA	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver
43	INHB	I	High-side gate driver control input. This pin controls the output of the high-side gate driver
44	INLB	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver
45	INHC	I	High-side gate driver control input. This pin controls the output of the high-side gate driver
46	INLC	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver
47	PGND	PWR	Device power ground. Connect to system ground
48	NC	NC	No connect. Do not connect anything to this pin
—	Thermal Pad	PWR	Must be connected to ground

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
GATE DRIVER			
Power supply pin voltage (VM)	–0.3	65	V
Voltage differential between ground pins (AGND, BGND, DGND, PGND)	–0.3	0.3	V
MOSFET drain sense pin voltage (VDRAIN)	–0.3	65	V
Charge pump pin voltage (CPH, VCP)	–0.3	V_{VM} + 13.5	V
Charge-pump negative-switching pin voltage (CPL)	–0.3	V_{VM}	V
Internal logic regulator pin voltage (DVDD)	–0.3	3.8	V
Voltage difference between VM and VDRAIN	–10	10	V
Digital pin voltage (ENABLE, IDRIVE, INHx, INLx, MODE, nFAULT, nSCS, SCLK, SDI, SDO, VDS, nDIAG)	–0.3	5.75	V
Continuous high-side gate drive pin voltage (GHx)	–5(2)	V_{VCP} + 0.5	V
Transient 200-ns high-side gate drive pin voltage (GHx)	–7	V_{VCP} + 0.5	V
High-side gate drive pin voltage with respect to SHx (GHx)	–0.3	13.5	V
Continuous high-side source sense pin voltage (SHx, DLx)	–5(2)	V_{VM} + 5	V
Transient 200-ns high-side source sense pin voltage (SHx, DLx)	–7	V_{VM} + 7	V
Continuous high-side source sense pin voltage (SHx, DLx)	–5(2)	V_{DRAIN} + 5	V
Transient 200-ns high-side source sense pin voltage (SHx, DLx)	–7	V_{DRAIN} + 7	V
Continuous low-side gate drive pin voltage (GLx)	–0.5	15	V
Gate drive pin source current (GHx, GLx)	Internally limited		A
Gate drive pin sink current (GHx, GLx)	Internally limited		A
Continuous low-side source sense pin voltage (SLx)	–1	1	V
Transient 200-ns low-side source sense pin voltage (SLx)	–3	3	V
Push-pull output buffer reference voltage (VSDO)	–0.3	5.75	V
Push-pull output current (SDO)	0	10	mA
Open drain pullup voltage (nFAULT)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Continuous high-side gate pin (GHx) and phase node pin voltage (SHx) should be limited to –2 V minimum for an absolute maximum of 65 V on VM. At 60 V and below, the full specification of –5 V continuous on GHx and SHx is allowable.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 10, 11, 20, 21, 30, 31, and 40)	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
GATE DRIVER				
V_{VM}	Power supply voltage (VM) Continuous (1)	5.5	50	V
	Power supply voltage (VM) Transient over voltage (2)	5.5	60	V
V_I	Input voltage (ENABLE, IDRIVE, INHx, INLx, MODE, nSCS, SCLK, SDI, VDS, VSDO, nDIAG)	0	5.5	V
f_{PWM}	Applied PWM signal (INHx, INLx)	0	200 (3)	kHz
I_{GATE_HS}	High-side average gate-drive current (GHx)	0	25 (3)	mA
I_{GATE_LS}	Low-side average gate-drive current (GLx)	0	25 (3)	mA
I_{DVDD}	External load current (DVDD)	0	30 (3)	mA
V_{SDO}	Push-pull voltage (SDO)	3	5.5	V
V_{OD}	Open drain pullup voltage (nFAULT)	0	5.5	V
T_A	Operating ambient temperature	–40	125	°C

(1) Operation at VM = 5.5V only when coming from higher VM. The minimum VM voltage for startup is greater than V_{UVLO} (rising) voltage.
(2) VM recommended operating condition for electrical characteristic table. Product life time depends on VM voltage. The device is intended for 12–V and 24–V battery automotive system with life-time nominal voltage of 5.5 V - 50 V. The device can be operated during additional overvoltage events as specified in ISO16750-2:2012
(3) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC (1)		DRV8340-Q1 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

Over recommended operating conditions 5.5 ≤ V_{VM} ≤ 60 V (unless otherwise noted). Typical limits apply for V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VCP, VM)						
I_{VM}	VM operating supply current	V_{VM} = 24 V, ENABLE = 3.3 V, INHx/INLx = 0 V, SHx = 0 V		12	16	mA
I_{VMQ}	VM sleep mode supply current	ENABLE = 0 V, V_{VM} = 24 V, T_A = 25°C		12	20	µA
		ENABLE = 0 V, V_{VM} = 24 V, T_A = 125°C			50	
t_{RST}	Reset pulse time	ENABLE = 0 V period to reset faults	4.4		43	µs
t_{WAKE} (1)	Turnon time	ENABLE = 3.3 V to outputs ready, V_{VM} > V_{UVLO}			1	ms
t_{SLEEP}	Turnoff time	ENABLE = 0 V to device sleep mode			1	ms
V_{DVDD}	DVDD regulator voltage	V_{VM} > 6 V, I_{DVDD} = 0 to 30 mA	3	3.3	3.6	V
		V_{VM} = 5.5 to 6 V, I_{DVDD} = 0 to 20 mA	3	3.3	3.6	V
V_{VCP}	VCP operating voltage with respect to VM	V_{VM} = 13 V, I_{VCP} = 0 to 25 mA	8.4	11	12.5	V
		V_{VM} = 10 V, I_{VCP} = 0 to 20 mA	6.3	9	10	
		V_{VM} = 8 V, I_{VCP} = 0 to 15 mA	5.4	7	8	
		V_{VM} = 5.5 V, I_{VCP} = 0 to 5 mA	4	5	6	
LOGIC-LEVEL INPUTS (CAL, ENABLE, INHx, INLx, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.7	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis			182		mV
I_{IL}	Input logic low current	V_{VIN} = 0 V; INHx, INLx, SDI(IDRIVE), SCLK(VDS), ENABLE	–5		5	µA
I_{IH}	Input logic high current	V_{VIN} = 5 V; INHx, INLx, SDI(IDRIVE), SCLK(VDS)		50	90	µA
I_{IH}	Input logic high current	V_{VIN} = 5 V; ENABLE		80	110	µA
R_{PD}	Pulldown resistance	To AGND; INHx, INLx, SDI(IDRIVE), SCLK(VDS)	50	100	200	kΩ
R_{PD}	Pulldown resistance	To AGND; ENABLE	30	60	110	kΩ
t_{PD}	Propagation delay	INHx/INLx input buffer and digital core propagation delay. Dead time is excluded.		105		ns
LOGIC LEVEL INPUT (nSCS)						
$V_{IL,nSCS}$	Input logic low voltage		0		0.7	V
$V_{IH,nSCS}$	Input logic high voltage		1.6		5.5	V
$R_{PU,nSCS}$	Pullup resistance	To DVDD	25	50	90	kΩ
SEVEN-LEVEL H/W INPUTS (MODE, IDRIVE, VDS)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	18 kΩ ± 5% tied to AGND		0.5		V
V_{I3}	Input mode 3 voltage	75 kΩ ± 5% tied to AGND		1.1		V
V_{I4}	Input mode 4 voltage	Hi-Z (> 1.5 MΩ)		1.65		V
V_{I5}	Input mode 5 voltage	75 kΩ ± 5% tied to DVDD		2.2		V
V_{I6}	Input mode 6 voltage	18 kΩ ± 5% tied to DVDD		2.8		V
V_{I7}	Input mode 7 voltage	MODE : 0.47 kΩ ± 5% tied to DVDD VDS, IDRIVE : Tied to DVDD		3.3		V
R_{PU}	Pullup resistance	Internal pullup to DVDD	35	73	125	kΩ
R_{PD}	Pulldown resistance	Internal pulldown to AGND	35	73	125	kΩ
PUSH-PULL OUTPUT (SDO)						
$R_{PU,SDO}$	Internal pullup	To VSDO = 5 V		40	90	Ω
		To VSDO = 3.3 V		60	120	
$R_{PD,SDO}$	Internal pulldown	To GND		30	50	Ω
OPEN DRAIN OUTPUT (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.15	V
I_{OZ}	Output high impedance leakage	V_O = 5 V	–1		9	µA
GATE DRIVERS (GHx, GLx)						

(1) Does not include OLP/Shorts diagnostic delay time in the H/W device

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Electrical Characteristics (continued)

Over recommended operating conditions 5.5 ≤ V_{VM} ≤ 60 V (unless otherwise noted). Typical limits apply for V_{VM} = 24 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GSH}	High-side gate drive voltage with respect to SHx		V_{VM} = 13 V, I_{VCP} = 0 to 25 mA, GHx no output load	8.4	11	12.5	V
			V_{VM} = 10 , I_{VCP} = 0 to 20 mA, GHx no output load	6.3	9	10	
			V_{VM} = 8 V, I_{VCP} = 0 to 15 mA, GHx no output load	5.4	7	8	
			V_{VM} = 5.5 V, I_{VCP} = 0 to 5 mA, GHx no output load	4	5	6	
V_{GSL}	Low-side gate drive voltage with respect to PGND		V_{VM} = 12 V, I_{VCP} = 0 to 25 mA, GLx no output load	9	11	12	V
			V_{VM} = 10 V, I_{VCP} = 0 to 20 mA, GLx no output load	9.9	10.0	10.1	
			V_{VM} = 8 V, I_{VCP} = 0 to 15 mA, GLx no output load	7.9	8.0	8.1	
			V_{VM} = 5.5 V, I_{VCP} = 0 to 5 mA, GLx no output load	5.4	5.5	5.6	
t_{DEAD}	Gate drive dead time	SPI Device	DEAD_TIME = 00b		500		ns
			DEAD_TIME = 01b		1000		
			DEAD_TIME = 10b		2000		
			DEAD_TIME = 11b		4000		
		H/W Device			1000		
t_{DRIVE}	Peak current gate drive time	SPI Device	TDRIVE = 00b		500		ns
			TDRIVE = 01b		1000		
			TDRIVE = 10b		2000		
			TDRIVE = 11b		3000		
		H/W Device			3000		
t_{DRIVE_MAX}	Peak current gate drive max time		IDRIVEP_Hx = 0000b, 0001b, 0010b, 0011b		20		µs

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Electrical Characteristics (continued)

Over recommended operating conditions 5.5 ≤ V_{VM} ≤ 60 V (unless otherwise noted). Typical limits apply for V_{VM} = 24 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEP}	Peak source gate current	SPI Device	IDRIVEP_Hx = 0000b (GHx), V_{VM} = 24 V	0.45	1.5	3.0	mA
			IDRIVEP_Lx = 0000b (GLx), V_{VM} = 24 V	0.81	2.7	5.4	
			IDRIVEP_Hx = 0001b (GHx), V_{VM} = 24 V	1.05	3.5	7	
			IDRIVEP_Lx = 0001b (GLx), V_{VM} = 24 V	1.17	3.9	7.8	
			IDRIVEP_Hx = 0010b (GHx), V_{VM} = 24 V	1.5	5	10	
			IDRIVEP_Lx = 0010b (GLx), V_{VM} = 24 V	1.95	6.5	13	
			IDRIVEP_Hx or IDRIVEP_Lx = 0011b (GHx/GLx), V_{VM} = 24 V	3	10	20	
			IDRIVEP_Hx or IDRIVEP_Lx = 0100b (GHx/GLx), V_{VM} = 24 V	4.5	15	30	
			IDRIVEP_Hx or IDRIVEP_Lx = 0101b (GHx/GLx), V_{VM} = 24 V	15	50	100	
			IDRIVEP_Hx or IDRIVEP_Lx = 0110b (GHx/GLx), V_{VM} = 24 V	18	60	120	
			IDRIVEP_Hx or IDRIVEP_Lx = 0111b (GHx/GLx), V_{VM} = 24 V	19.5	65	130	
			IDRIVEP_Hx or IDRIVEP_Lx = 1000b (GHx/GLx), V_{VM} = 24 V	76	200	400	
			IDRIVEP_Hx or IDRIVEP_Lx = 1001b (GHx/GLx), V_{VM} = 24 V	79.8	210	420	
			IDRIVEP_Hx or IDRIVEP_Lx = 1010b (GHx/GLx), V_{VM} = 24 V	98.8	260	520	
			IDRIVEP_Hx or IDRIVEP_Lx = 1011b (GHx/GLx), V_{VM} = 24 V	100.7	265	530	
			IDRIVEP_Hx or IDRIVEP_Lx = 1100b (GHx/GLx), V_{VM} = 24 V	279.3	735	1470	
			IDRIVEP_Hx or IDRIVEP_Lx = 1101b (GHx/GLx), V_{VM} = 24 V	304	800	1600	
			IDRIVEP_Hx or IDRIVEP_Lx = 1110b (GHx/GLx), V_{VM} = 24 V	355.3	935	1870	
			IDRIVEP_Hx or IDRIVEP_Lx = 1111b (GHx/GLx), V_{VM} = 24 V	380	1000	2000	
		H/W Device	IDRIVE = Tied to AGND (GHx), V_{VM} = 24 V	0.45	1.5	3.0	
			IDRIVE = Tied to AGND (GLx), V_{VM} = 24 V	0.81	2.7	5.4	
			IDRIVE = 18 kΩ ± 5% tied to AGND (GHx), V_{VM} = 24 V	1.5	5	10	
			IDRIVE = 18 kΩ ± 5% tied to AGND (GLx), V_{VM} = 24 V	1.95	6.5	13	
			IDRIVE = 75 kΩ ± 5% tied to AGND (GHx/GLx), V_{VM} = 24 V	3	10	20	
			IDRIVE = Hi-Z (GHx/GLx), V_{VM} = 24 V	18	60	120	
			IDRIVE = 75 kΩ ± 5% tied to DVDD (GHx/GLx), V_{VM} = 24 V	76	200	400	
			IDRIVE = 18 kΩ ± 5% tied to DVDD (GHx/GLx), V_{VM} = 24 V	98.8	260	520	
			IDRIVE = Tied to DVDD (GHx/GLx), V_{VM} = 24 V	380	1000	2000	

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Electrical Characteristics (continued)

Over recommended operating conditions 5.5 ≤ V_{VM} ≤ 60 V (unless otherwise noted). Typical limits apply for V_{VM} = 24 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEN}	Peak sink gate current	SPI Device	IDRIVEN_Hx or IDRIVEN_Lx = 0000b, V_{VM} = 24 V	0.9	3	5.4	mA
			IDRIVEN_Hx or IDRIVEN_Lx = 0001b, V_{VM} = 24 V	2.09	7	12.6	
			IDRIVEN_Hx or IDRIVEN_Lx = 0010b, V_{VM} = 24 V	3	10	18	
			IDRIVEN_Hx or IDRIVEN_Lx = 0011b, V_{VM} = 24 V	6	20	36	
			IDRIVEN_Hx or IDRIVEN_Lx= 0100b, V_{VM} = 24 V	9	30	54	
			IDRIVEN_Hx or IDRIVEN_Lx = 0101b, V_{VM} = 24 V	30	100	180	
			IDRIVEN_Hx or IDRIVEN_Lx = 0110b, V_{VM} = 24 V	36	120	216	
			IDRIVEN_Hx or IDRIVEN_Lx = 0111b, V_{VM} = 24 V	39	130	234	
			IDRIVEN_Hx or IDRIVEN_Lx = 1000b, V_{VM} = 24 V	120	400	720	
			IDRIVEN_Hx or IDRIVEN_Lx = 1001b, V_{VM} = 24 V	126	420	756	
			IDRIVEN_Hx or IDRIVEN_Lx = 1010b, V_{VM} = 24 V	156	520	936	
			IDRIVEN_Hx or IDRIVEN_Lx = 1011b, V_{VM} = 24 V	159	530	954	
			IDRIVEN_Hx or IDRIVEN_Lx = 1100b, V_{VM} = 24 V	441	1470	2646	
			IDRIVEN_Hx or IDRIVEN_Lx = 1101b, V_{VM} = 24 V	480	1600	2880	
			IDRIVEN_Hx or IDRIVEN_Lx = 1110b, V_{VM} = 24 V	561	1870	3366	
			IDRIVEN_Hx or IDRIVEN_Lx = 1111b, V_{VM} = 24 V	600	2000	3600	
		H/W Device	IDRIVE = Tied to AGND, V_{VM} = 24 V	0.9	3	5.4	
			IDRIVE = 18 kΩ ± 5% tied to AGND, V_{VM} = 24 V	3	10	18	
			IDRIVE = 75 kΩ ± 5% tied to AGND, V_{VM} = 24 V	6	20	36	
			IDRIVE = Hi-Z, V_{VM} = 24 V	36	120	216	
			IDRIVE = 75 kΩ ± 5% tied to DVDD, V_{VM} = 24 V	120	400	720	
			IDRIVE = 18 kΩ ± 5% tied to DVDD, V_{VM} = 24 V	156	520	936	
			IDRIVE = Tied to DVDD, V_{VM} = 24 V	600	2000	3600	
I_{HOLDP}	Gate holding source current after t_{DRIVE}	SPI Device	IDRIVEP_Hx = 0000b, V_{VM} = 24 V	0.45	1.5	3.8	mA
			IDRIVEP_Hx = 0001b, V_{VM} = 24 V	1.05	3.5	7	
			IDRIVEP_Hx = 0010b, V_{VM} = 24 V	1.5	5	10	
			IDRIVEP_Hx = 0011b, V_{VM} = 24 V	3	10	20	
			All other IDRIVE settings, V_{VM} = 24 V	4.5	15	30	
		H/W Device	IDRIVE tied to AGND, V_{VM} = 24 V	0.45	1.5	3.8	
			IDRIVE = 18 kΩ ± 5% tied to AGND, V_{VM} = 24 V	1.5	5	10	
			IDRIVE = 75 kΩ ± 5% tied to AGND, V_{VM} = 24 V	3	10	20	
			All other IDRIVE settings, V_{VM} = 24 V	4.5	15	30	
I_{HOLDN}	Gate holding sink current after t_{DRIVE}	SPI Device	IDRIVEP_Hx = 0000b, V_{VM} = 24 V	0.9	3	5.4	mA
			IDRIVEP_Hx = 0001b, V_{VM} = 24 V	2	7	12.6	
			IDRIVEP_Hx = 0010b, V_{VM} = 24 V	3	10	18	
			IDRIVEP_Hx = 0011b, V_{VM} = 24 V	6	20	36	
			All other IDRIVE settings, V_{VM} = 24 V	9	30	54	
		H/W Device	IDRIVE tied to AGND, V_{VM} = 24 V	0.9	3	5.4	
			IDRIVE = 18 kΩ ± 5% tied to AGND, V_{VM} = 24 V	3	10	18	
			IDRIVE = 75 kΩ ± 5% tied to AGND, V_{VM} = 24 V	6	20	36	
			All other IDRIVE settings, V_{VM} = 24 V	9	30	54	
I_{STRONG}	Gate strong pulldown current (GHx to SHx and GLx to PGND)		IDRIVEP_Hx = 0000b, 0001b, 0010b, 0011b, V_{VM} = 24 V	9	30	54	mA
			All other IDRIVE settings, V_{VM} = 24 V	0.6	2	3.6	A
R_{OFF}	Gate hold off resistor		GHx to SHx		150	280	kΩ
R_{OFF}	Gate hold off resistor		GLx to PGND		150	280	kΩ
PROTECTION CIRCUITS							
V_{UVLO}	VM undervoltage lockout		VM falling, UVLO report		5.2	5.4	V
			VM rising, UVLO recovery		5.4	5.9	
$V_{UVLO,DVDD}$	DVDD undervoltage lockout					2.9	V
V_{UVLO_HYS}	VM undervoltage hysteresis		Rising to falling threshold		200		mV

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Electrical Characteristics (continued)

Over recommended operating conditions 5.5 ≤ V_{VM} ≤ 60 V (unless otherwise noted). Typical limits apply for V_{VM} = 24 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{UVLO_DEG}	VM undervoltage deglitch time		VM falling, UVLO report		11.5		µs
V_{CPUV}	Charge pump undervoltage lockout		VCP falling, CPUV report	V_{VM} + 1.4	V_{VM} + 2.5	V_{VM} + 3.1	V
V_{GS_CLAMP}	High-side gate clamp		Positive clamping voltage	15	16.5	19	V
			Negative clamping voltage		–0.7		
V_{OLA}	Open load active mode detection threshold		DLx – VDRAIN	150	300	430	mV
			SLx – SHx, –1 < SLx < 0	150	300	500	
I_{OL}	Open load current				2.5		mA
t_{OLP}	Open load passive diagnostic delay	SPI Device	OLP_SHRT_DLY = 00b		0.25		ms
			OLP_SHRT_DLY = 01b		1.25		
			OLP_SHRT_DLY = 10b		5		
			OLP_SHRT_DLY = 11b		11.5		
		H/W Device	After t_{WAKE} and t_{SHORTS} elapse		5		
t_{SHORTS}	Offline short-to-battery and short-to-GND diagnostic delay	SPI Device	OLP_SHRT_DLY = 00b		0.1		ms
			OLP_SHRT_DLY = 01b		0.5		
			OLP_SHRT_DLY = 10b		2		
			OLP_SHRT_DLY = 11b		4.4		
		H/W Device	After t_{WAKE} elapses		2		
V_{VDS_OCP}	V_{DS} overcurrent trip voltage	SPI Device	VDS_LVL = 0000b	0.01	0.06	0.11	V
			VDS_LVL = 0001b	0.08	0.13	0.18	
			VDS_LVL = 0010b	0.15	0.2	0.25	
			VDS_LVL = 0011b	0.2	0.26	0.32	
			VDS_LVL = 0100b	0.24	0.31	0.38	
			VDS_LVL = 0101b	0.38	0.45	0.52	
			VDS_LVL = 0110b	0.45	0.53	0.61	
			VDS_LVL = 0111b	0.51	0.6	0.69	
			VDS_LVL = 1000b	0.59	0.68	0.77	
			VDS_LVL = 1001b	0.64	0.75	0.86	
			VDS_LVL = 1010b	0.81	0.94	1.07	
			VDS_LVL = 1011b	0.97	1.13	1.29	
			VDS_LVL = 1100b	1.14	1.3	1.46	
			VDS_LVL = 1101b	1.34	1.5	1.66	
			VDS_LVL = 1110b	1.52	1.7	1.88	
			VDS_LVL = 1111b	1.69	1.88	2.07	
		H/W Device	VDS = Tied to AGND	0.01	0.06	0.11	
			VDS = 18 kΩ ± 5% tied to AGND	0.08	0.13	0.18	
			VDS = 75 kΩ ± 5% tied to AGND	0.2	0.26	0.32	
			VDS = Hi-Z	0.51	0.6	0.69	
			VDS = 75 kΩ ± 5% tied to DVDD	0.97	1.13	1.29	
			VDS = 18 kΩ ± 5% tied to DVDD	1.69	1.88	2.07	
			VDS = Tied to DVDD		Disabled		
t_{OCP_DEG}	V_{DS} and V_{SENSE} overcurrent deglitch time	SPI Device	OCP_DEG=000b		2.5		µs
			OCP_DEG = 001b		4.75		
			OCP_DEG = 010b		6.75		
			OCP_DEG = 011b		8.75		
			OCP_DEG = 100b		10.25		
			OCP_DEG = 101b		11.5		
			OCP_DEG = 110b		16.5		
			OCP_DEG = 111b		20.5		
		H/W Device			4.75		

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Electrical Characteristics (continued)

Over recommended operating conditions 5.5 ≤ V_{VM} ≤ 60 V (unless otherwise noted). Typical limits apply for V_{VM} = 24 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RETRY}	Overcurrent fault retry time	SPI Device	TRETRY = 00b		2		ms
			TRERTY = 01b		4		
			TRETRY = 10b		6		
			TRETRY = 11b		8		
T_{HYS}	Thermal hysteresis		Die temperature, T_J		20		°C
T_{OTSD}	Thermal shutdown temperature		Die temperature, T_J	150	170	188	°C
T_{OTW}	Thermal warning temperature		Die temperature, T_J	130	150	169	°C

7.6 SPI Timing Requirements

Over recommended operating conditions unless otherwise noted. Typical limits apply for V_{VM} = 24 V

			MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after enable	VM > UVLO, ENABLE = 3.3 V			1	ms
t_{CLK}	SCLK minimum period		100			ns
t_{CLKH}	SCLK minimum high time		50			ns
t_{CLKL}	SCLK minimum low time		50			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{H_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time	SCLK high to SDO valid, C_L = 20 pF			30	ns
t_{SU_nSCS}	nSCS input setup time		50			ns
t_{H_nSCS}	nSCS input hold time		50			ns
t_{HI_nSCS}	nSCS minimum high time before active low		500			ns
t_{DIS_nSCS}	nSCS disable time	nSCS high to SDO high impedance		10		ns

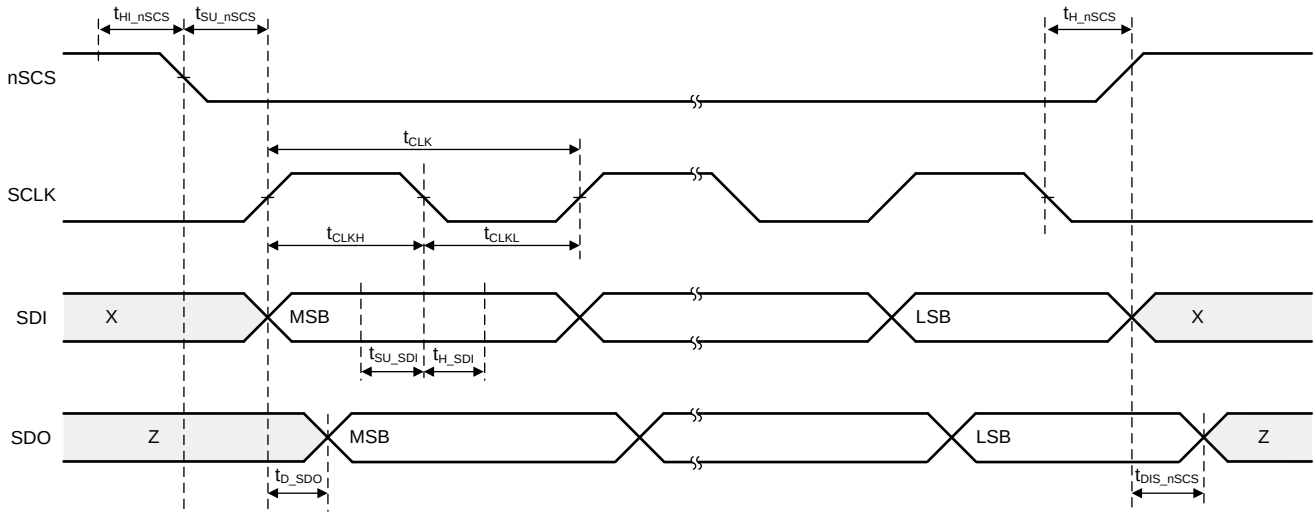

Figure 1. SPI Slave Mode Timing Diagram

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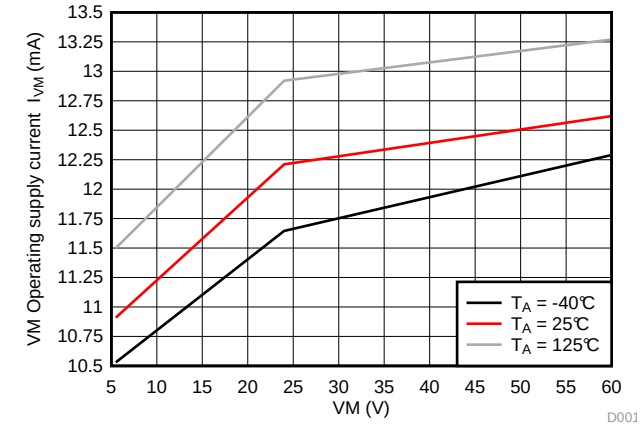
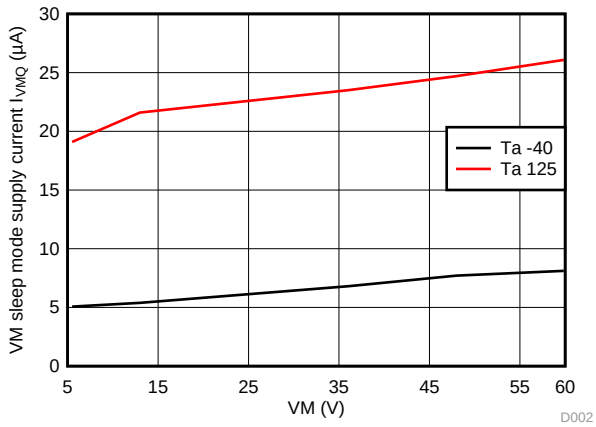
7.7 Typical Characteristics



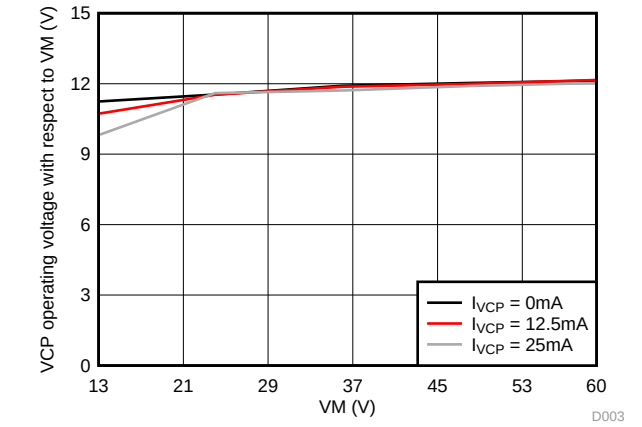
No PWM Switching

Figure 2. VM Operating Supply Current



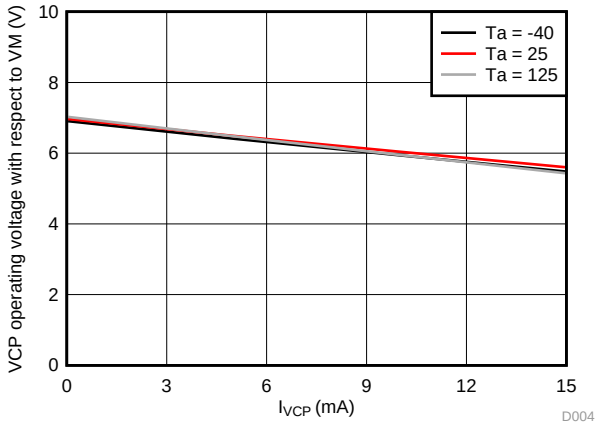
ENABLE = 0 V

Figure 3. VM Sleep Mode Supply Current



T_A = 25°C

Figure 4. VCP w.r.t VM over VM voltage > 13 V



VM = 8 V

Figure 5. VCP w.r.t VM over output load I_{VCP}

8 Detailed Description

8.1 Overview

The DRV8340-Q1 device is an integrated gate driver for three-phase motor driver automotive applications. These devices decrease system complexity by integrating three independent half-bridge gate drivers, charge pump, and linear regulator for the supply voltages of the high-side and low-side gate drivers.. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most common settings through fixed external resistors.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1-A source, 2-A sink peak currents. A doubler charge pump generates the supply voltage of the high-side gate drive. This charge pump architecture regulates the VCP output voltage for driving high-side power MOSFET. The supply voltage of the low-side gate driver is generated using a linear regulator from the VM power supply that regulates for driving low-side power MOSFET. A Smart Gate Drive architecture provides the ability to dynamically adjust the strength of the gate drive output current which lets the gate driver control the V_{DS} switching speed of the power MOSFET. This feature lets the user remove the external gate drive resistors and diodes, reducing the component count in the bill of materials (BOM), cost, and area of the printed circuit board (PCB). The architecture also uses an internal state machine to protect against short-circuit events in the gate driver, control the half-bridge dead time, and protect against dV/dt parasitic turnon of the external power MOSFET.

In addition to the high level of device integration, the DRV8340-Q1 device provides a wide range of integrated protection features. These features include power supply undervoltage lockout (UVLO), charge pump undervoltage lockout (CPUV), V_{DS} overcurrent monitoring (OCP), gate driver short-circuit detection (GDF), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

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8.2 Functional Block Diagram

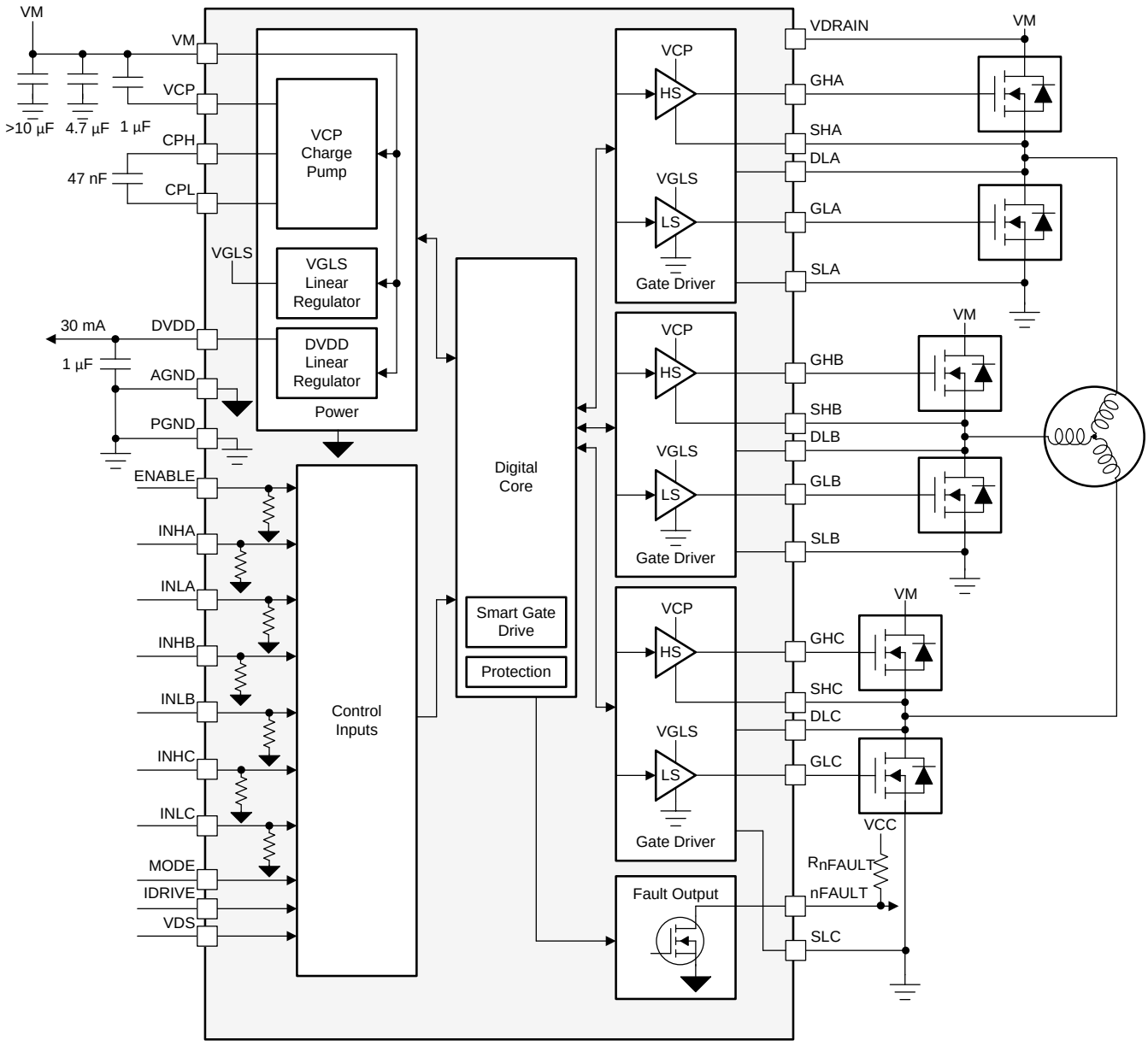

Figure 6. Block Diagram for DRV8340H

Functional Block Diagram (continued)

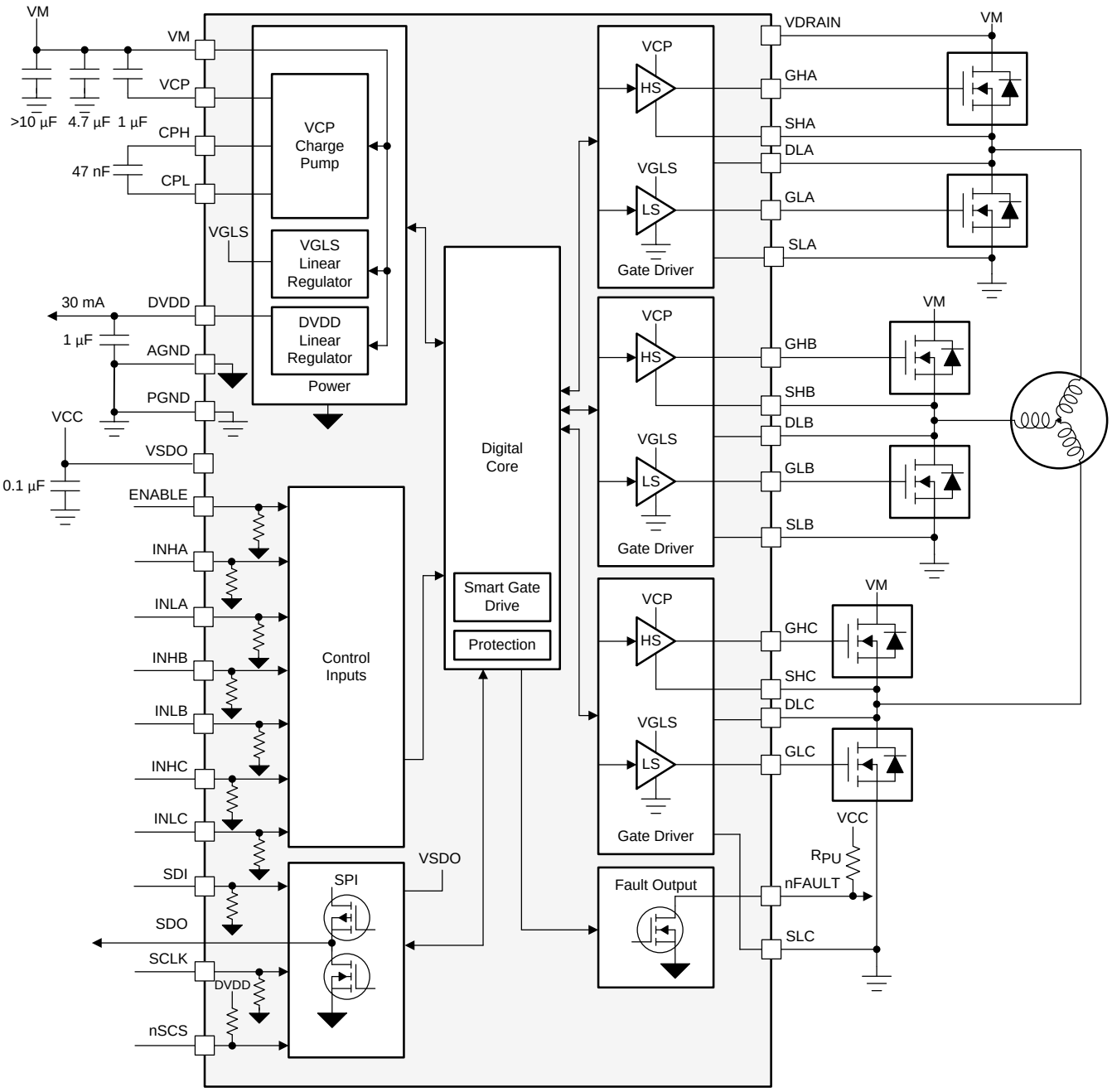

Figure 7. Block Diagram for DRV8340S

8.3 Feature Description

8.3.1 Three Phase Smart Gate Drivers

The DRV8340-Q1 device integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A doubler charge pump provides the correct gate bias voltage to the high-side MOSFET across a wide operating voltage range in addition to providing 100% support of the duty cycle. An internal linear regulator provides the gate bias voltage for the low-side MOSFETs. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

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Feature Description (continued)

The DRV8340-Q1 device implements a Smart Gate Drive architecture which allows the user to dynamically adjust the gate drive current without requiring external resistors to limit the gate current. Additionally, this architecture provides a variety of protection features for the external MOSFETs including automatic dead time insertion, prevent of parasitic dV/dt gate turnon, and gate fault detection.

8.3.1.1 PWM Control Modes

The DRV8340-Q1 device provides eight different PWM control modes in the SPI device and seven different modes in the H/W device to support various commutation and control methods. Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set all INHx and INLx pins to logic low before making a MODE pin or PWM_MODE register change. Table 3 shows the different mode settings for the SPI device. The MODE bit setting of 100b is not available in the H/W device.

Table 3. 6x PWM Mode Truth Table

H/W DEVICE	SPI DEVICE	MODE SETTINGS
Tied to AGND	000b	6x PWM
18 kΩ to AGND	001b	3x PWM
75 kΩ to AGND	010b	1x PWM
Hi-Z	011b	Independent half-bridge (for all three half-bridges)
Not Available	100b	Phases A and B are independent half-bridges, Phase C is independent FET
75 kΩ to DVDD	101b	Phases B and C are independent half-bridges, Phase A is independent FET
18 kΩ to DVDD	110b	Phases A is independent half-bridge, Phase B and C are independent FET
0.47 kΩ to DVDD	111b	Independent MOSFET (for all three half-bridges)

8.3.1.1.1 6x PWM Mode (PWM_MODE = 000b or MODE Pin Tied to AGND)

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in Table 4.

Table 4. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx + DLx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

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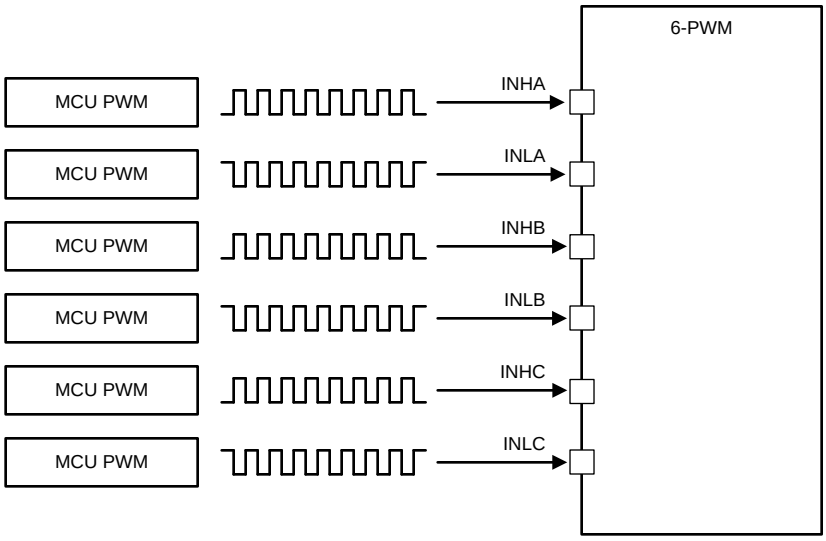

Figure 8. 6-PWM Mode

8.3.1.1.2 3x PWM Mode (PWM_MODE = 001b or MODE Pin = 18 kΩ to AGND)

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 5.

Table 5. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx + DLx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

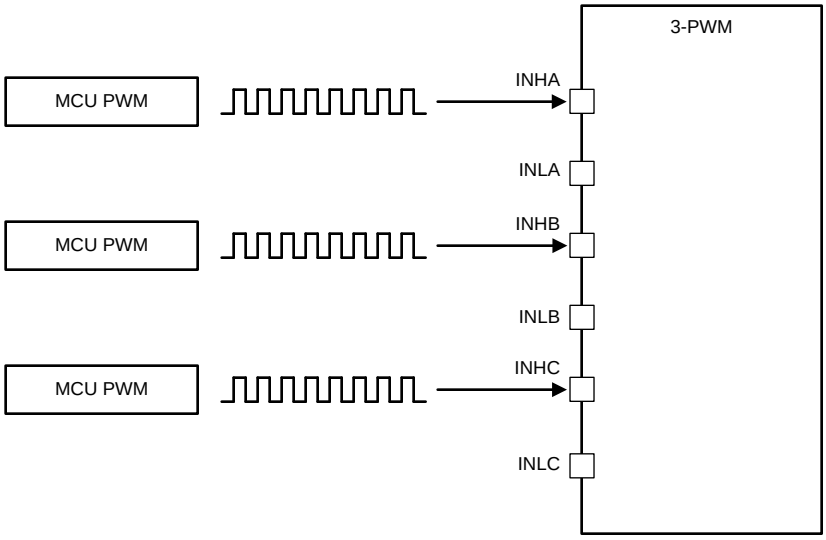

Figure 9. 3-PWM Mode

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8.3.1.1.3 1x PWM Mode (PWM_MODE = 010b or MODE Pin = 75 kΩ to AGND)

In 1x PWM mode, the DRV8340-Q1 device uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using one PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to the digital outputs of the Hall effect sensor from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) on SPI devices. This configuration is set using the 1PWM_COM bit in the SPI registers.

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when Hall effect sensors are directly controlling the state of the INLA, INHB, and INLB inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when the INLC pin is pulled low. This brake is independent of the state of the other input pins. Tie the INLC pin high if this feature is not required. In the SPI device, the brake and coast mode can also be selected by the 1PWM_BRAKE register (see Table 22).

Table 6. Synchronous 1x PWM Mode

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS(1)						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

(1) *!PWM* is the inverse of the PWM signal.

Table 7. Asynchronous 1x PWM Mode 1PWM_COM = 1 (SPI Only)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

Figure 10 and Figure 11 show the different possible configurations in 1x PWM mode.

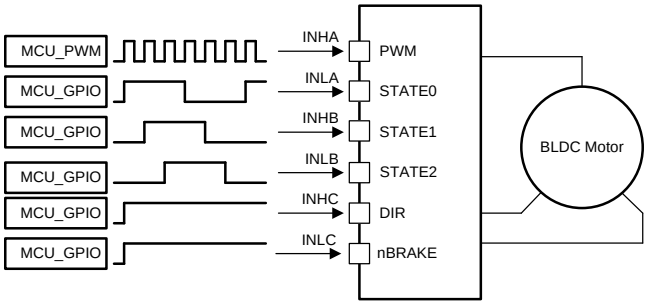

Figure 10. 1x PWM—Simple Controller

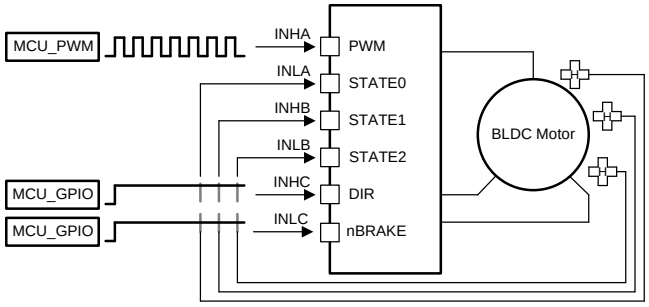

Figure 11. 1x PWM—Hall Effect Sensor

8.3.1.1.4 Independent Half-Bridge PWM Mode (PWM_MODE = 011b or MODE Pin is > 1.5 MΩ to AGND or Hi-Z)

In independent half-bridge PWM mode, the INHx pin controls each half-bridge independently and supports two output states: low or high. The corresponding INHx and INLx signals control the output state as listed in Table 8. The INLx pin is used to change the half-bridge to high impedance. If the high-impedance (Hi-Z) state is not required, tie all INLx pins logic high.

Table 8. Independent Half-Bridge Mode Truth Table

INLx	INHx	GLx	GHx
0	X	L	L
1	0	H	L
1	1	L	H

8.3.1.1.5 Phases A and B are Independent Half-Bridges, Phase C is Independent FET (MODE = 100b)

In this mode, phases A and B are independent half-bridge control, with independent fault handling and dead time enforcement by the device. Phase C is independent FET mode where the dead time inserted by the device is bypassed and both MOSFETs can be turned-on at the same time. This mode is not available in the H/W version.

8.3.1.1.6 Phases B and C are Independent Half-Bridges, Phase A is Independent FET (MODE = 101b or MODE Pin is 75 kΩ to DVDD)

In this mode, phases B and C are independent half-bridge control, with independent fault handling and dead time enforcement by the device. Phase A is independent FET mode where the dead time inserted by the device is bypassed and both MOSFETs can be turned-on at the same time.

8.3.1.1.7 Phases A is Independent Half-Bridge, Phases B and C are Independent FET (MODE = 110b or MODE Pin is 18 kΩ to DVDD)

In this mode, phase A is independent half-bridge control, with dead time enforcement by the device. Phases B and C are independent FET mode where the dead time is bypassed and both MOSFETs in a given phase can be turned-on at the same time. Fault handling is also done independently for each FET in phases B and C.

8.3.1.1.8 Independent MOSFET Drive Mode (PWM_MODE = 111b or MODE Pin = 0.47 kΩ to DVDD)

In independent MOSFET drive mode, the INHx and INLx pins control the outputs, GHx and GLx, respectively. This control mode lets the DRV8340-Q1 device drive separate high-side and low-side loads with each half-bridge. These types of loads include unidirectional brushed DC motors, solenoids, and low-side and high-side switches. In this mode, turning on both the high-side and low-side MOSFETs at the same time in a given half-bridge gate driver is possible to use the device as a high-side or low-side driver. The dead time (t_{DEAD}) is bypassed in the mode and must be inserted by the external MCU.

Table 9. Independent PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

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Figure 12 shows how the DRV8340-Q1 device can be used to connect a high-side load and a low-side load at the same time with one half-bridge and drive the loads independently. In this mode, the VDS monitors are active for both the MOSFETs to protect from an overcurrent condition.

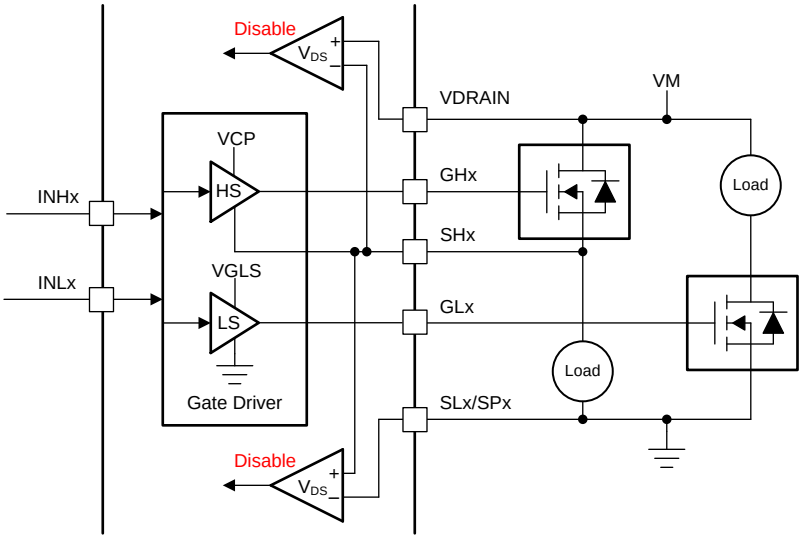

Figure 12. Independent PWM High-Side and Low-Side Drivers

If the half-bridge is used to implement only a high-side or low-side driver, using the VDS monitors to help protect from an overcurrent condition is possible as shown in Figure 13 or Figure 14. The unused gate driver can stay disconnected.

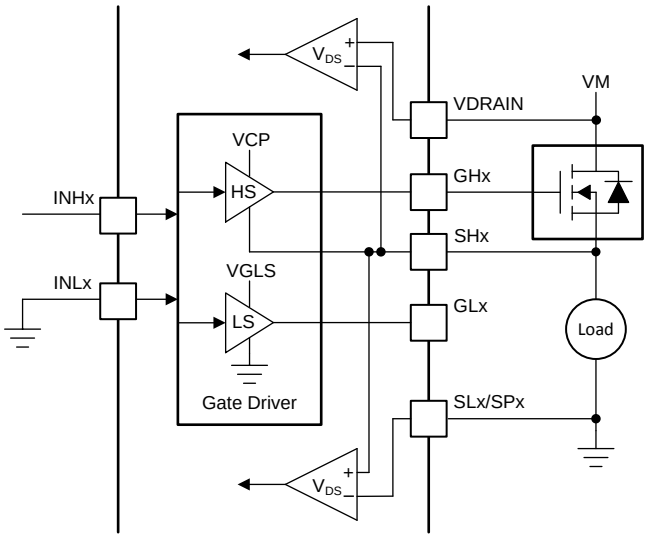

Figure 13. One High-Side Driver

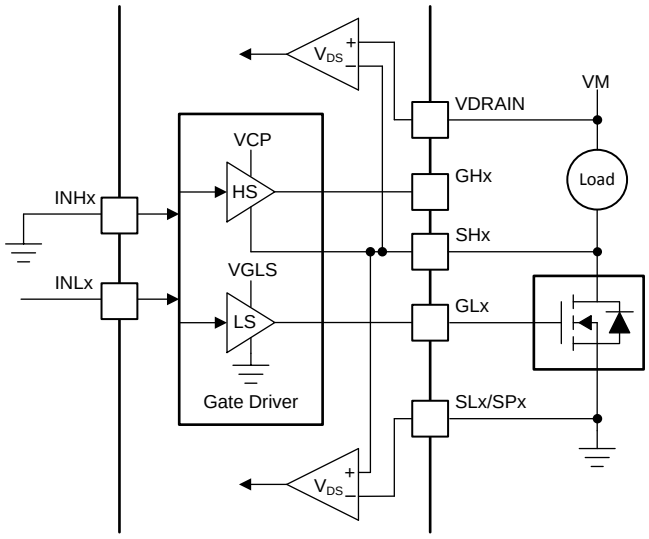

Figure 14. One Low-Side Driver

Figure 15 shows how the DRV8340-Q1 device can be used to connect a solenoid load where both the high-side and low-side MOSFETs can be turned on at the same time to drive the load without causing shoot-through. TI recommends having the external diodes for current recirculation. If a half-bridge is not used, the gate pins (GHx and GLx) can stay unconnected and the sense pins (SHx and DLx) can be tied directly or with a resistor to GND.

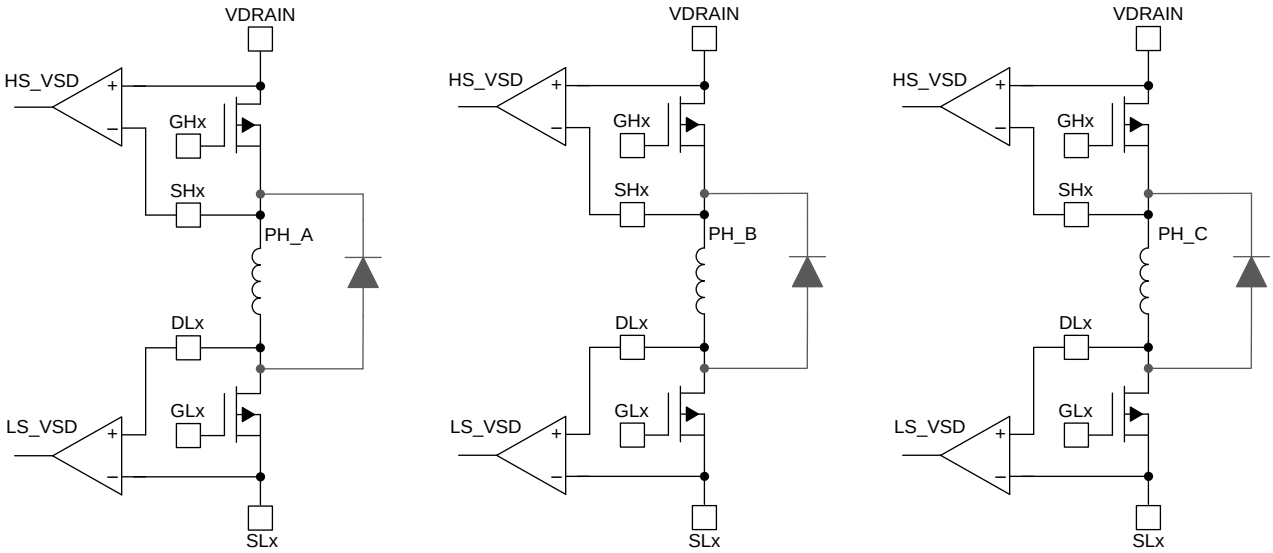

Figure 15. Solenoid Drive Configuration

8.3.1.2 Device Interface Modes

The DRV8340-Q1 device supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their circuit design and layout.

8.3.1.2.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the DRV8340-Q1 device. This support lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin has a push-pull output structure.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV8340-Q1 device.

For more information on the SPI, see the *SPI Communication* section.

8.3.1.2.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are IDRIVE, MODE, and VDS. This conversion lets the application designer configure the most common device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The IDRIVE pin configures the gate drive current strength.
- The MODE pin configures the PWM control mode.
- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.

For more information on the hardware interface, see the *Pin Diagrams* section.

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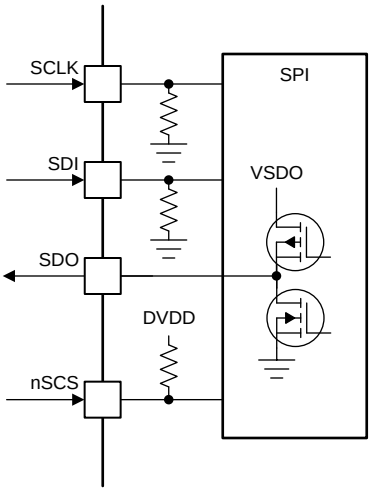

Figure 16. SPI

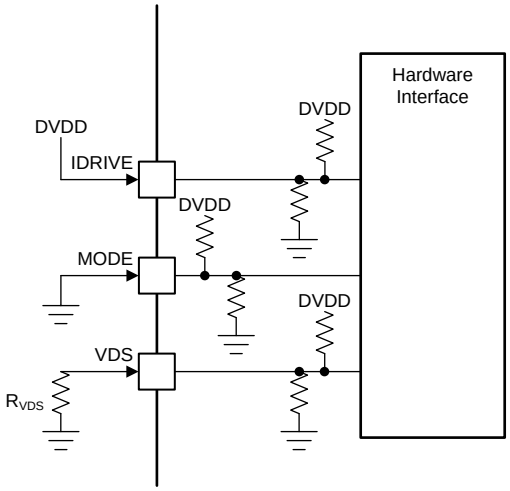

Figure 17. Hardware Interface

8.3.1.3 Gate Driver Voltage Supplies

The voltage supply for the high-side gate driver is created using a doubler charge pump that operates from the VM voltage supply input. The charge pump lets the gate driver correctly bias the high-side MOSFET gate with respect to the source across a wide input supply voltage range. The charge pump is regulated to keep a fixed output voltage V_{VCP} and supports an average output current I_{GATE_HS}. The charge pump is continuously monitored for undervoltage events to prevent under-driven MOSFET conditions. The charge pump requires a ceramic capacitor between the VM and VCP pins to act as the storage capacitor. Additionally, a flying capacitor is required between the CPH and CPL pins.

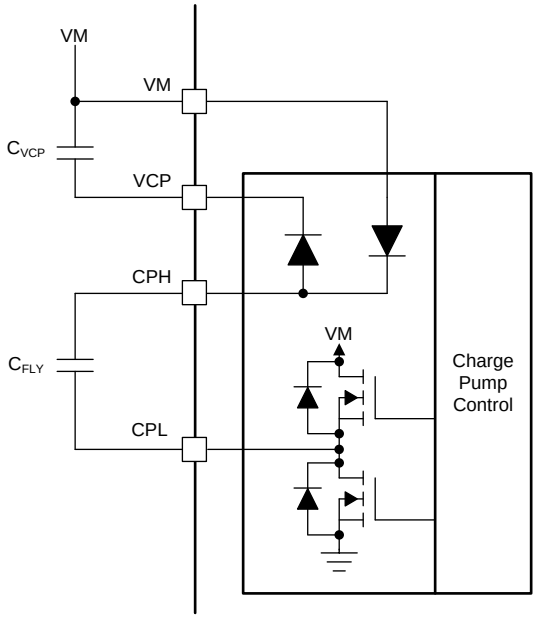

Figure 18. Charge Pump Architecture

The voltage supply of the low-side gate driver is created using a linear regulator that operates from the VM voltage supply input. The linear regulator lets the gate driver correctly bias the low-side MOSFET gate with respect to ground. The linear regulator output is V_{GSL} and supports an output current I_{GATE_LS}.

8.3.1.4 Smart Gate Drive Architecture

The DRV8340-Q1 gate drivers use an adjustable, complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates.

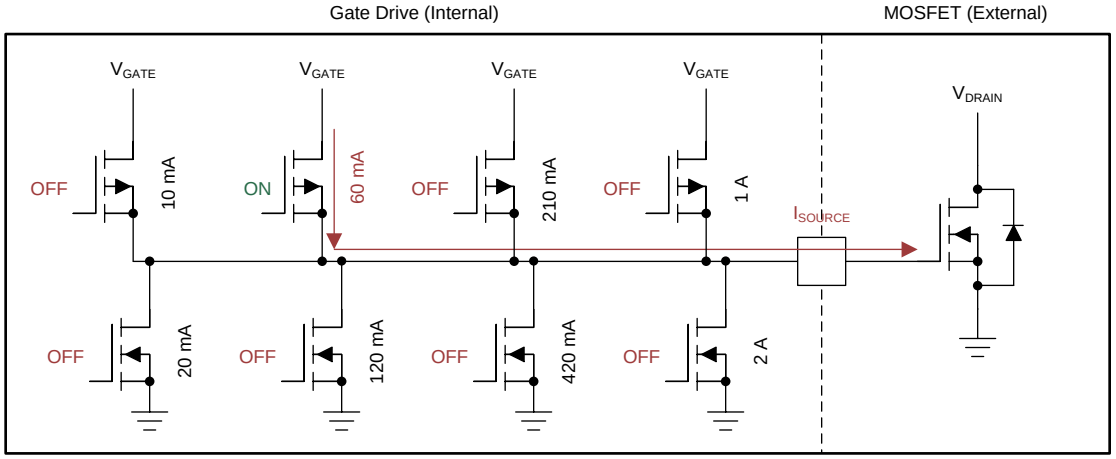

Figure 19. Charge Pump Architecture

Additionally, the gate drivers use a Smart Gate Drive architecture to provide additional control of the external power MOSFETs, additional steps to protect the MOSFETs, and optimal tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE which are described in the *IDRIVE: MOSFET Slew-Rate Control* section and *TDRIVE: MOSFET Gate Drive Control* section. Figure 20 shows the high-level functional block diagram of the gate driver.

The IDRIVE gate drive current and TDRIVE gate drive time should be initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times (see the *Application and Implementation* section).

The high-side gate driver also implements a Zener clamp diode to help protect the external MOSFET gate from overvoltage conditions in the case of external short-circuit events on the MOSFET.

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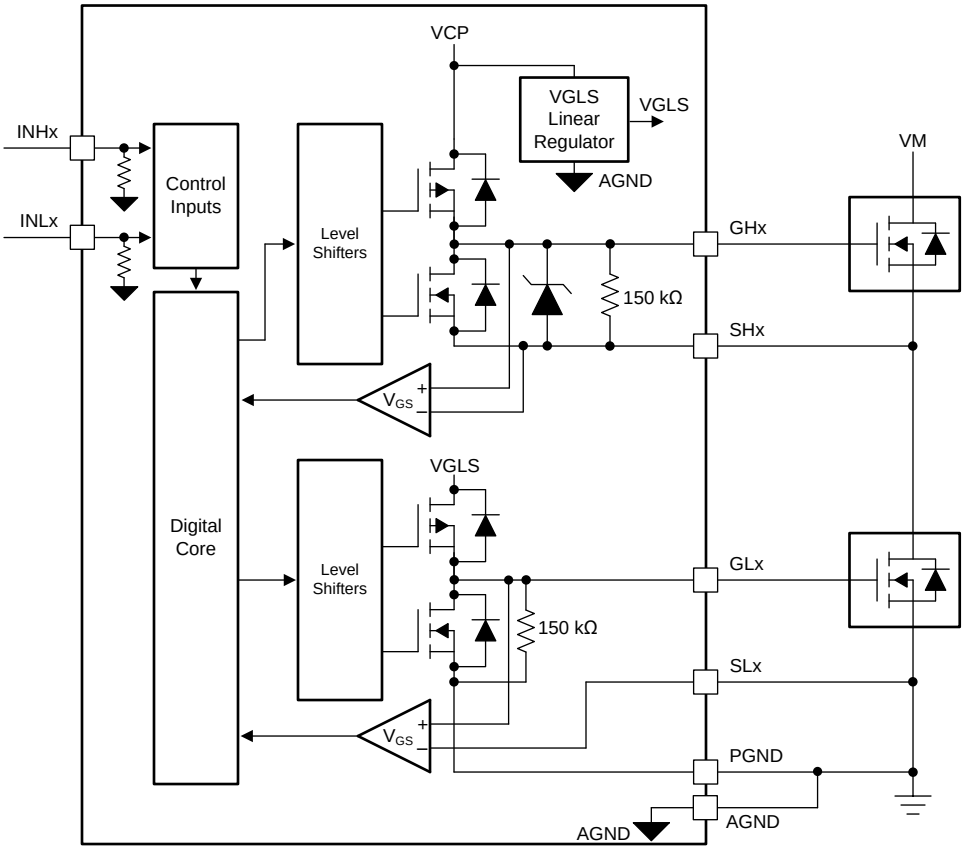

Figure 20. Gate Driver Block Diagram

8.3.1.4.1 IDRIVE: MOSFET Slew-Rate Control

The IDRIVE component implements adjustable gate drive current to control the MOSFET V_{DS} slew rates. The MOSFET V_{DS} slew rates are a critical factor for optimizing radiated emissions, energy, and duration of diode recovery spikes, dV/dt gate turnon resulting in shoot-through, and switching voltage transients related to parasitics in the external half-bridge. The IDRIVE component operates on the principal that the MOSFET V_{DS} slew rates are predominately determined by the rate of gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By letting the gate driver adjust the gate current, the gate driver can effectively control the slew rate of the external power MOSFETs.

The IDRIVE component lets the DRV8340-Q1 device dynamically switch between gate drive currents either through a register setting on SPI devices or the IDRIVE pin on hardware interface devices. The SPI devices provide 16 I_{DRIVE} settings ranging from 1.5-mA to 1-A source and 3-mA to 2-A sink. Hardware interface devices provide 7 I_{DRIVE} settings within the same ranges. The setting of the gate drive current is delivered to the gate during the turnon and turnoff of the external power MOSFET for the t_{DRIVE} duration. After the MOSFET turnon or turnoff, the gate driver switches to a smaller hold current (I_{HOLD}) to improve the gate driver efficiency. In the event of an overcurrent condition, the IDRIVE component is automatically decreased to help prevent device damage. For additional details on the IDRIVE settings, see the *Register Maps* section for the SPI devices and the *Pin Diagrams* section for the hardware interface devices.

8.3.1.4.2 TDRIVE: MOSFET Gate Drive Control

The TDRIVE component is an integrated gate drive state machine that provides automatic dead time insertion through handshaking between the high-side and low-side gate drivers, parasitic dV/dt gate turnon prevention, and MOSFET gate fault detection.

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The first component of the TDRIVE state machine is automatic dead time insertion. Dead time is period of time between the switching of the external high-side and low-side MOSFETs to make sure that they do not cross conduct and cause shoot-through. The DRV8340-Q1 device uses V_{GS} voltage monitors to measure the MOSFET gate-to-source voltage and determine the correct time to switch instead of relying on a fixed time value. This feature lets the dead time of the gate driver adjust for variation in the system such as temperature drift and variation in the MOSFET parameters. An additional digital dead time (t_{DEAD}) can be inserted and is adjustable through the registers on SPI devices.

The second component of the TDRIVE state machine is parasitic dV/dt gate turnon prevention. To implement this component, the TDRIVE state machine enables a strong pulldown current (I_{STRONG}) on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown occurs for the TDRIVE duration. This feature helps remove parasitic charge that couples into the MOSFET gate when the voltage half-bridge switch node slews rapidly.

The third component implements a gate-fault detection scheme to detect pin-to-pin solder defects, a MOSFET gate failure, or a MOSFET gate stuck-high or stuck-low voltage condition. This implementation is done with a pair of V_{GS} gate-to-source voltage monitors for each half-bridge gate driver. When the gate driver receives a command to change the state of the half-bridge it starts to monitor the gate voltage of the external MOSFET. If, at the end of the t_{DRIVE} period, the V_{GS} voltage has not increased the correct threshold, the gate driver reports a fault. To make sure that a false gate drive fault (GDF) is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not increase the PWM time and will terminate if another PWM command is received while active. In the SPI device, for IDRIVE bit settings of 0000b, 0001b, 0010b, and 0011b, a longer t_{DRIVE} time of 20-µs is automatically selected by the TDRIVE_MAX bit. If the 20-µs t_{DRVIE} time is not required, write a 0 to the TDRIVE_MAX bit to disable it and set the t_{DRIVE} time by the TDRIVE bits. For all other IDRIVE settings, writing to the TDRIVE_MAX bit is disabled. This option is not available in the H/W device.

For additional details on the TDRIVE settings, see the *Register Maps* section for SPI devices and the *Pin Diagrams* section for hardware interface devices. Figure 21 shows an example of the TDRIVE state machine in operation.

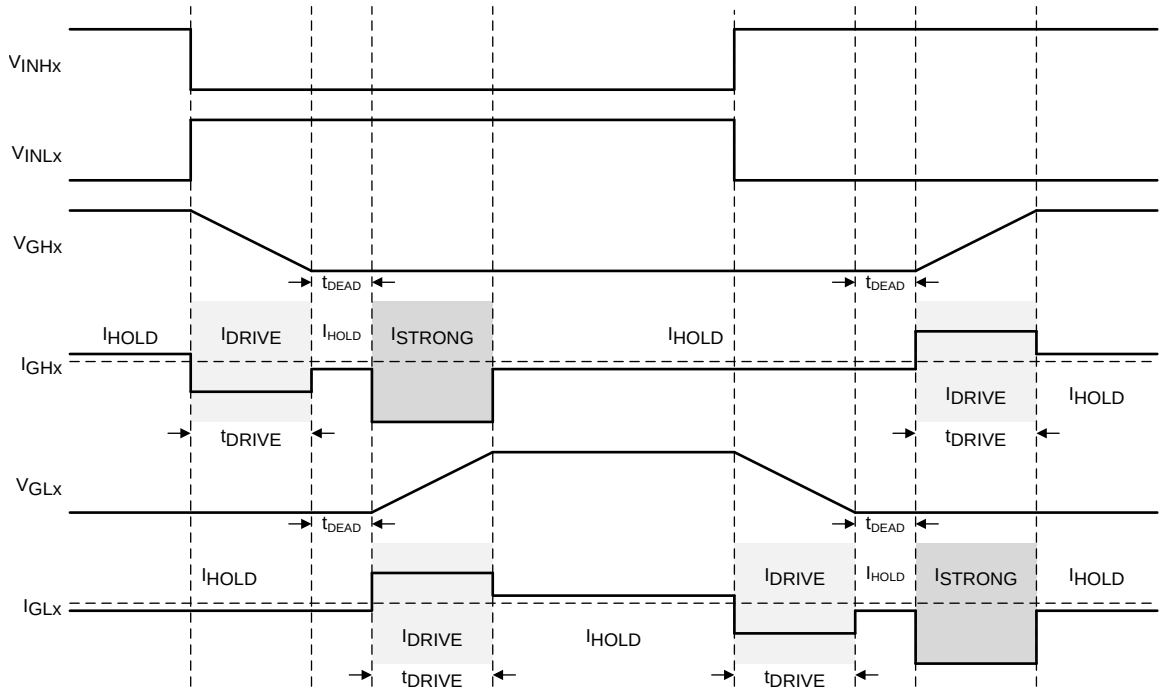

Figure 21. TDRIVE State Machine

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8.3.1.4.3 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has three parts consisting of the digital input deglitcher delay, the digital propagation delay, and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

8.3.1.4.4 MOSFET V_{DS} Monitors

The gate drivers implement adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the V_{DS} trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and action is taken according to the device V_{DS} fault mode.

The high-side V_{DS} monitors measure the voltage between the VDRAIN and SHx pins.The low-side V_{DS} monitor measures between the DLx and SLx pins.

The V_{VDS_OCP} threshold is programmable from 0.06 V to 1.88 V. For additional information on the V_{DS} monitor levels, see the *Register Maps* section for SPI devices and in the *Pin Diagrams* section hardware interface device.

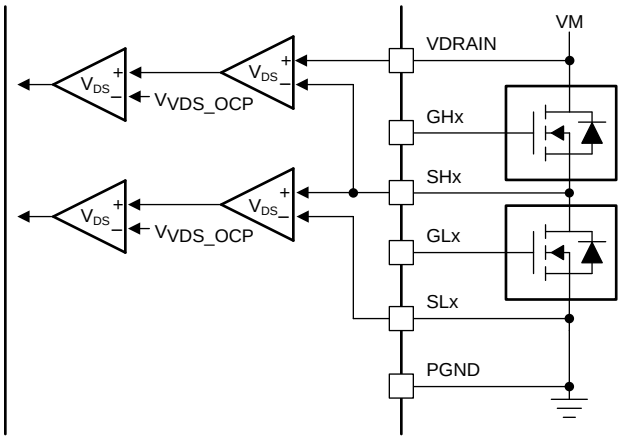

Figure 22. DRV8340-Q1 V_{DS} Monitors

8.3.1.4.5 VDRAIN Sense Pin

The DRV8340-Q1 device provides a separate sense pin for the common point of the high-side MOSFET drain. This pin is called VDRAIN. This pin lets the sense line for the overcurrent monitors (VDRAIN) and the power supply (VM) stay separate and prevent noise on the VDRAIN sense line. This separation also lets implementation of a small filter on the gate driver supply (VM) or insertion of a boost converter to support lower voltage operation if desired. Care must still be used when designing the filter or separate supply because VM is still the reference point for the VCP charge pump that supplies the high-side gate drive voltage (V_{GSH}). The VM supply must not drift too far from the VDRAIN supply to avoid violating the V_{GS} voltage specification of the external power MOSFETs.

8.3.1.4.6 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5 V or 3.3 V supply. When a fault is detected, the nFAULT line is logic low. For a 3.3-V pullup the nFAULT pin can be tied to the DVDD pin with a resistor (refer to the *Application and Implementation* section). For a 5-V pullup an external 5-V supply must be used.

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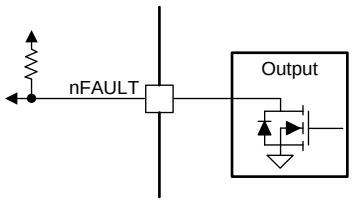

Figure 23. nFAULT Pin

During the power-up sequence, or when going from sleep mode, the digital core of the device is enabled to a VM voltage of approximately 3.3 V and the device is fully operational after VM exceeds 5.5 V. After the digital core is alive if the VM does not exceed 5.5 V within 100-µs the device will flag a UVLO fault. In the H/W device, the nFAULT pin is driven low. In the SPI device, the FAULT and ULVO bits will be latched high

8.3.2 DVDD Linear Voltage Regulator

A 3.3-V, 30-mA linear regulator is integrated into the DRV8340-Q1 device and is available for use by external circuitry. This regulator can provide the supply voltage for a low-power MCU or other circuitry supporting low current. The output of the DVDD regulator should be bypassed near the DVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The DVDD nominal, no-load output voltage is 3.3 V. When the DVDD load current exceeds 30 mA, the regulator functions like a constant-current source. The output voltage drops significantly with a current load greater than 30 mA.

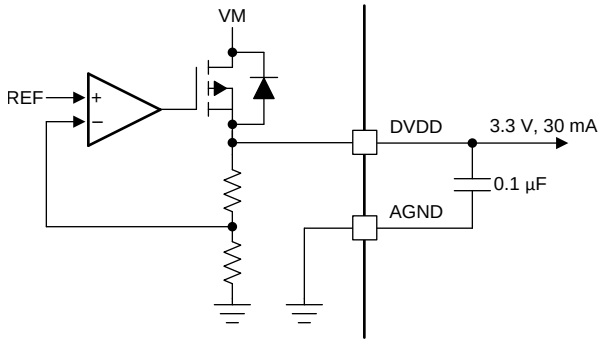

Figure 24. DVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the DVDD linear regulator.

$$P = \left(V_{VM} - V_{DVDD}\right) \times I_{DVDD} \tag{1}$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of DVDD results in a power dissipation as shown in Equation 2.

$$P = \left(24\ V - 3.3\ V\right) \times 20\ mA = 414\ mW \tag{2}$$

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8.3.3 Pin Diagrams

Figure 25 shows the input structure for the logic level pins, INHx, INLx, ENABLE, nSCS, SCLK, and SDI. The input can be driven with a voltage or external resistor.

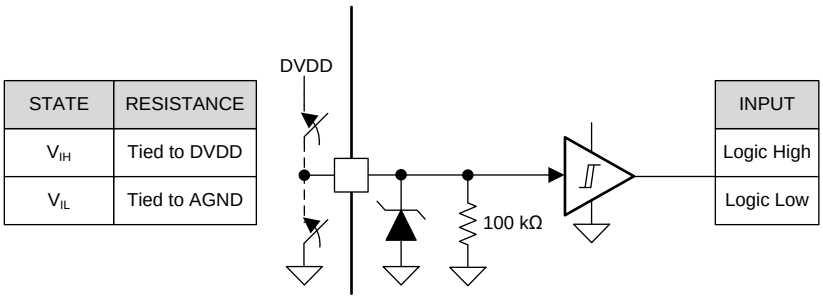

Figure 25. Logic-Level Input Pin Structure

Figure 26 shows the structure of the seven level input pins, MODE, IDRIVE and VDS, on hardware interface devices. The input can be set with an external resistor.

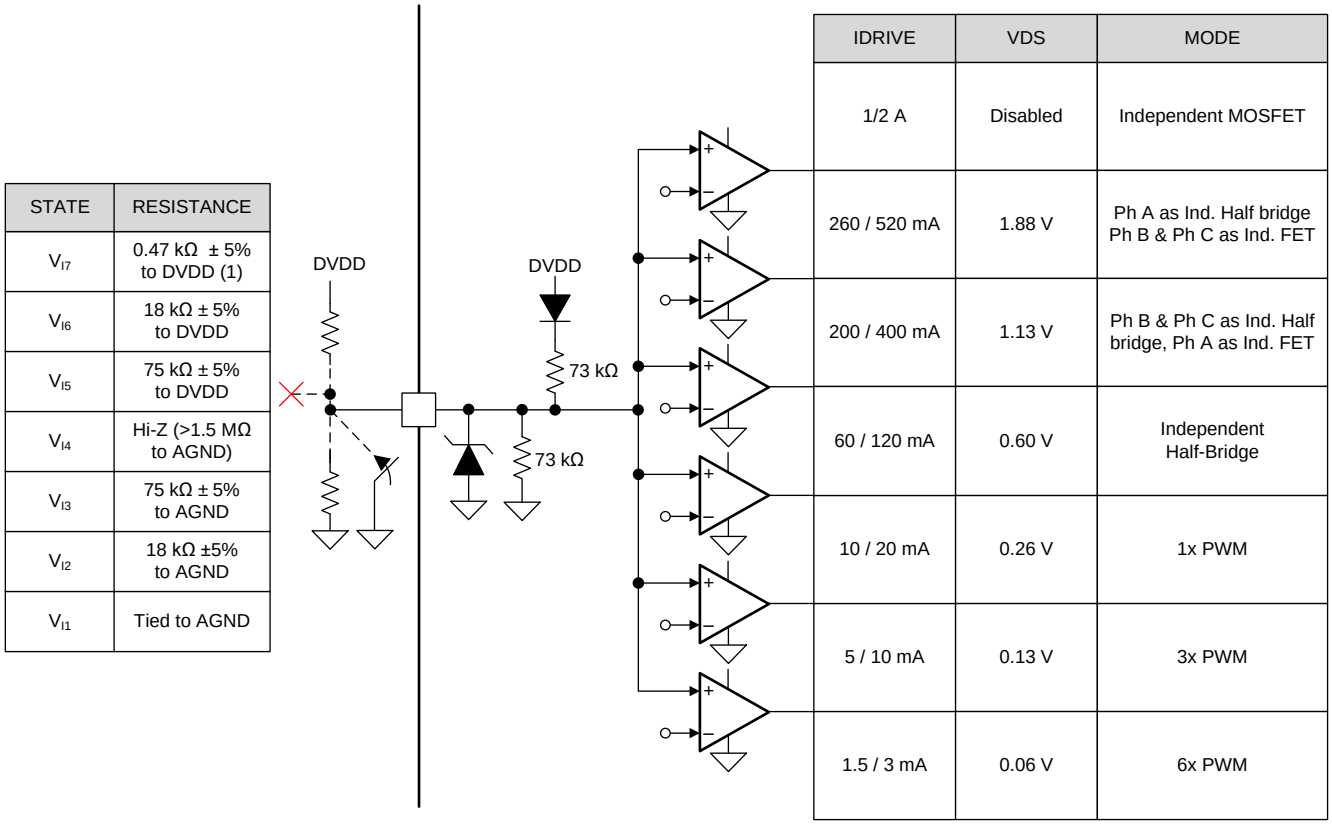

Figure 26. Seven Level Input Pin Structure (1)

Figure 27 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function correctly.

(1) V_{I7} requires a 0.47 kΩ resistor to DVDD for MODE input pin. VDS and IDRIVE pins can be directly tied to DVDD.

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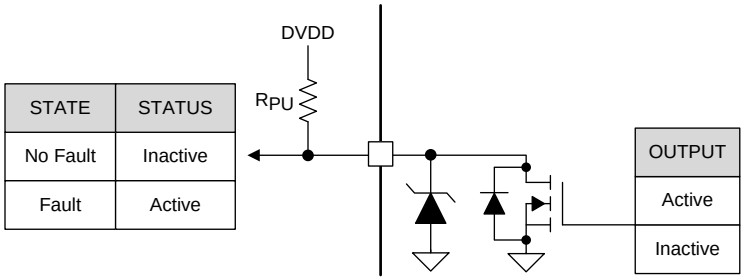

Figure 27. Open-Drain Output Pin Structure

8.3.4 Gate Driver Protective Circuits

The DRV8340-Q1 device is protected against VM undervoltage, charge pump undervoltage, MOSFET VDS overcurrent, gate driver shorts, and overtemperature events. The DRV8340-Q1 device also provides a detection mechanism for open-load, offline short-to-supply, and offline short-to-ground conditions. When a fault occurs, the individual fault bit is set high along with the global FAULT bit in the FAULT status register for the SPI device. The FAULT bit is OR'ed with all the other individual status bits. In the H/W device, only the nFAULT pin is driven low during a fault condition. Some of the protection and detection features can be disabled through SPI in the SPI device, or the nDIAG pin in the H/W device

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Table 10. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
VM undervoltage (UVLO)	$V_{VM} < V_{UVLO}$	—	nFAULT	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
Charge pump undervoltage (CPUV)	$V_{VCP} < V_{CPUV}$	DIS_CPUV = 0b	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$
		DIS_CPUV = 1b	None	Active	Active	
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{VDS\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	Report only
		OCP_MODE = 11b	None	Active	Active	No action
Gate driver fault (GDF)	Gate voltage stuck > t_{DRIVE}	DIS_GDF = 0b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		DIS_GDF = 1b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	OTSD_MODE = 0b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OTSD_MODE = 1b	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$
Open load passive (OLP)	No load detected	EN_OLP = 0b	None	Hi-Z	Active	No action
		EN_OLP = 1b	nFAULT	Hi-Z	Active	Report only
Open load active (OLA)	No load detected	EN_OLA_X = 0b	None	Active	Active	No action
		EN_OLA_X = 1b	nFAULT	Active	Active	Report only
Offline short-to-supply (SHT_BAT)	Phase node short-to-supply	EN_SHT_TST = 0b	None	Hi-Z	Active	No action
		EN_SHT_TST = 1b	nFAULT	Hi-Z	Active	Report only
Offline short-to-ground (SHT_GND)	Phase node short-to-ground	EN_SHT_TST = 0b	None	Hi-Z	Active	No action
		EN_SHT_TST = 1b	nFAULT	Hi-Z	Active	Report only
Device internal memory (1)data fault	Memory checksum fault detected	—	nFAULT	Active	Active	No action

(1) The DRV8340-Q1 has a OTP (one time program) memory which stores TI internal data used for analog functional blocks. The memory has a check-sum feature, and nFAULT is pulled low if a fault is detected at power up.

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8.3.4.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold, all of the external MOSFETs are disabled, the charge pump is disabled, and the nFAULT pin is driven low. The FAULT and VM_UVLO bits are also latched high in the registers on SPI devices. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the VM undervoltage condition clears. The VM_UVLO bit stays set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}).

8.3.4.2 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the CPUV threshold voltage of the charge pump, all of the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and CPUV bits are also latched high in the registers in the SPI device. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the VCP undervoltage condition is removed. The FAULT and CPUV bits stay set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). Setting the DIS_CPUV bit high on the SPI devices disables this protection feature. If the DIS_CPUV bit is set high and a charge pump undervoltage condition occurs, the device keeps operating but the CPUV fault bit is set high in the SPI register until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). CPUV protection cannot be disabled in the H/W device.

8.3.4.3 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

A MOSFET overcurrent event is sensed by monitoring the VDS voltage drop across the external MOSFET $R_{DS(on)}$. If the voltage across an enabled MOSFET exceeds the V_{VDS_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a VDS_OCP event is recognized and action is done according to the OCP_MODE. On hardware interface devices, the V_{VDS_OCP} threshold is set with the VDS pin, the t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE is configured for latched shutdown but can be disabled by tying the VDS pin to DVDD. In the SPI device, the V_{VDS_OCP} threshold is set through the VDS_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG bits in the SPI register, and the OCP_MODE bit can operate in four different modes: V_{DS} latched shutdown, V_{DS} automatic retry, V_{DS} report only, and V_{DS} disabled.

8.3.4.3.1 V_{DS} Latched Shutdown (OCP_MODE = 00b)

After a VDS_OCP event in this mode, all external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the VDS_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). This is the default mode in both the H/W and SPI device options.

8.3.4.3.2 V_{DS} Automatic Retry (OCP_MODE = 01b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation starts again automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, VDS_OCP, and MOSFET OCP bits stay latched until the t_{RETRY} period expires.

8.3.4.3.3 V_{DS} Report Only (OCP_MODE = 10b)

No protective action occurs after a VDS_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, VDS_OCP, and corresponding MOSFET OCP bits high in the SPI registers. The gate drivers continue to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the VDS_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.4.3.4 V_{DS} Disabled (OCP_MODE = 11b)

No action occurs after a VDS_OCP event in this mode. The VDS overcurrent monitor is disabled for all three half-bridges at the same time and the DIS_VDS_x bits are locked. In the H/W device, VDS_OCP is disabled for all three half-bridges at the same time through the VDS pin.

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8.3.4.4 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, SLx, or VM pins. Additionally, a gate driver fault may be encountered if the selected IDRIVE setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin driven low. In addition, the FAULT, GDF, and corresponding VGS bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the gate driver fault condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). In the SPI device, setting the DIS_GDF bit high disables this protection feature. If DIS_GDF bit is set high and a gate drive fault occurs, the device keeps operating but the appropriate VGS fault bit is set high in the SPI register until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). GDF cannot be disabled in the H/W device option.

Gate driver faults can indicate that the selected IDRIVE or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the IDRIVE or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on. The t_{DRIVE} time also refers to the GDF fault blanking time.

Fault handling is done as follows based on the MODE setting:

- In 6x, 3x, and 1x PWM modes a GDF fault in one of the external MOSFETs turns off all the MOSFETs.
- In independent half-bridge mode (MODE = 011b or MODE pin is Hi-Z) a GDF fault in one half-bridge only disables both the MOSFETs in that half-bridge. The MOSFETs in the other half-bridges operate as commanded.
- In independent MOSFET mode (MODE = 111b or MODE pin tied to DVDD) a GDF fault in a MOSFET only disables that particular MOSFET. All the other MOSFETs operate as commanded. The same fault handling scheme applies for MODE = 100b, 101b, and 110b.
- A GDF fault in phases set as Independent half-bridge disables both MOSFETs in that particular phase.
- A GDF fault in phases set as Independent FET mode disables the MOSFET where the fault occurred.

8.3.4.5 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. When the die temperature falls lower than the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin by setting the OTW_REP bit to 1 through the SPI registers. OTW is not available in the H/W device.

8.3.4.6 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OTSD bits are latched high. This protection feature cannot be disabled. The overtemperature protection can operate in two different modes.

8.3.4.6.1 Latched Shutdown (OTSD_MODE = 0b)

In latched shutdown mode, after a OTSD event, normal operation starts again (motor driver operation and the nFAULT line released) when the OTSD condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This is the default mode for a OTSD event in the SPI device.

When the DRV8340-Q1 device hits thermal shutdown, the OTSD and FAULT bits are latched in the SPI register. Clearing the fault through the CLR_FLT bit or an nSLEEP reset pulse will clear the OSTD and FAULT bits. When the DRV8340-Q1 device hits thermal shutdown, the device will disable the charge pump without triggering CPUV. The charge pump will be enabled again when the OTSD and FAULT bits are cleared through the CLR_FLT bit or an nSleep reset Pulse.

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8.3.4.6.2 Automatic Recovery (OTSD_MODE = 1b)

In automatic recovery mode, after a OTSD event, normal operation starts again (motor driver operation and the nFAULT line released) when the junction temperature falls to less than the overtemperature threshold limit minus the hysteresis (T_{OTSD} – T_{HYS}). The OTSD bit stays latched high indicating that a thermal event occurred until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse. This is the default mode for a OTSD event in the H/W device.

8.3.4.7 Open Load Detection (OLD)

If the load is disconnected from the device, an open load is detected and the nFAULT pin is latched low. In the DRV8340-Q1 device, The FAULT, OL_SHT, and the corresponding open load (OL_PH_x) bits in the SPI register are latched high. When the open-load condition is removed, and the MCU clears the fault through either the CLR_FLT bit or an ENABLE-pin reset pulse (t_{RST}), the device is ready to drive the motor based on the input commands.

8.3.4.7.1 Open Load Detection in Passive Mode (OLP)

In open load detection in passive mode, open load diagnosis is performed without the motor in motion. If the motor is disconnected from the device an open load is detected and the nFAULT pin will latch low until a clear faults command is issued by the MCU either through the CLR_FLT bit or an ENABLE reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode. OLP is designed for applications having capacitance less than the values listed in Table 11 between motor phase pins to ground.

Table 11. Open Load Passive Diagnostic Run-Time

Capacitance (nF)	OLP_SHTS_DLY (ms)
5	0.25
26	1.25
110	5
270	11.5

When the open load test is running, all external MOSFETs are disabled. For the H/W device option, at power-up or after going from sleep mode, the offline short-to-supply (SHT_BAT) and short-to-ground (SHT_GND) diagnostics run first followed by the OLP diagnostic if the nDIAG pin is left as no connect or tied to GND. If the nDIAG pin is tied to DVDD (or an external 3.3 V) the open load test is not performed. If a short condition is detected, the OLP diagnostic is not run (see Offline Shorts Diagnostics). If a short condition and open load occurs on a given phase at device power-up, for example, only the short condition is reported on the nFAULT pin and through the SPI fault register. In the SPI device option the OLP test is performed when commanded through SPI. If both short and OLP diagnostics are enabled simultaneously and a short condition is detection, only the short condition is reported on the nFAULT pin and through the SPI fault register.

The sequence to perform open load diagnostics in passive mode is as follows:

1. Device powered up (ENABLE = 1).
2. Mode is selected by SPI.
3. Hi-Z all three half-bridges by turning-off all the external MOSFETs.
4. Write a 1 to the EN_OLP bit in the SPI register and OLP is performed.
   - If an open load is detected, the nFAULT pin is driven low, and the FAULT bit, the OLD bit, and the respective OL_PH_x bit are latched high. When the open load condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an ENABLE reset pulse which resets the OL_PH_x register bit and causes the nFAULT pin to go high.
   - If open load is not detected, the EN_OLP bits return to default setting (0b) after t_{OL} expires.

The EN_OLP register keeps the written command until the diagnostic is complete. The half bridges must stay in Hi-Z state for the entire duration of the test. While open load diagnostic is running, if an input change occurs or the EN_OLP bit is set low, the open load test is aborted to start normal operation again, and no fault is reported. OLP should not be performed if the motor is energized.

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The open load detection checks for a high impedance connection on the motor phase pins (SHx or DLx). The diagnostic has two major steps as listed in the *OLP Steps* section. The sequencing of the pullup and pulldown current varies depending on the load connections. Figure 28 a simplified H-bridge configuration as an example for open load detection.

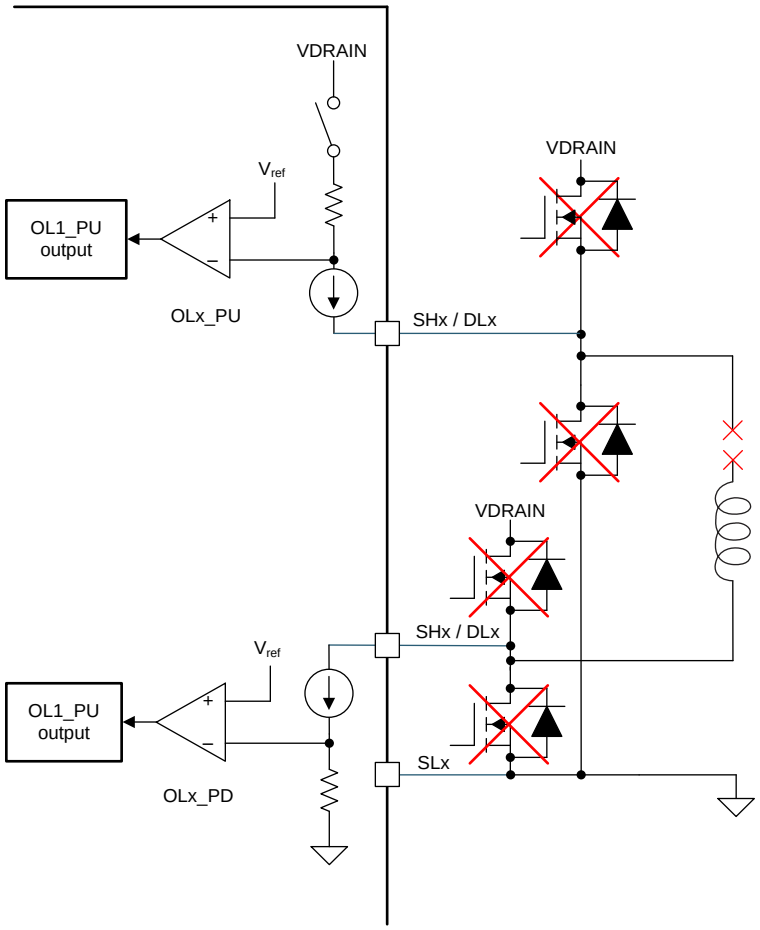

Figure 28. Circuit for Open Load Detection in Passive Mode

8.3.4.7.1.1 OLP Steps

The OLP algorithm list is as follows:

- The pullup current source is enabled. If a load is connected, current passes through the pullup resistor and the OLx_PU comparator output stays low. If an open load condition occurs, the current through the pullup resistor goes 0 and the OLx_PU comparator trips high.
- The pulldown current source is enabled. In the same way, the OLx_PD comparator output either stays low to indicate load-connected, or trips high to indicate an open load condition.
- If both the OLx_PU and OLx_PD comparators report an open load, the OL_PH_x bit in the SPI register latches high, and the nFAULT line goes low, to indicate an OL fault.

When the OL condition is removed, a clear faults command must be issued by the micro-controller either through the CLR_FLT bit or an ENABLE reset pulse which resets open load register bits. The charge pump stays active during this fault condition. The load connections shown in Figure 29 are not supported OLP.

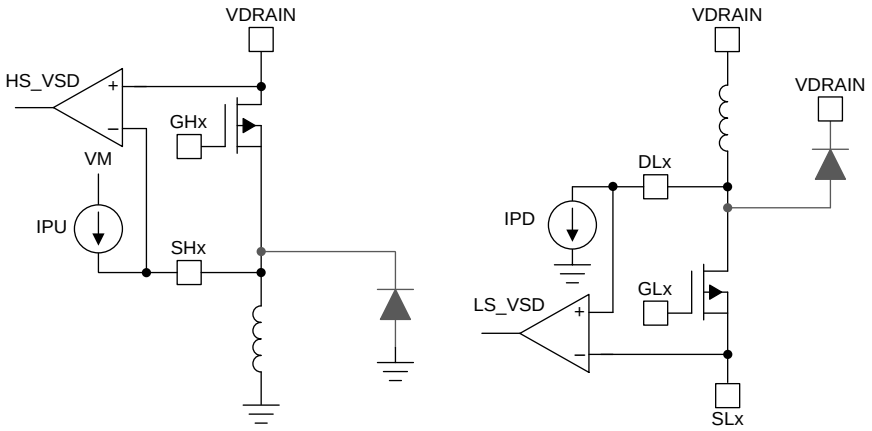

Figure 29. Load Configurations Not Supported

8.3.4.7.2 Open Load Detection in Active Mode (OLA)

An open load in active mode is disabled by default in the SPI device and can be enabled independently per half-bridge by writing a 1 to the EN_OLA_x bit. In the H/W device, OLA runs if the nDIAG pin is left as unconnected or tied to GND. OLA is detected when the motor gets disconnected from the driver when it is commutating. Figure 30 shows a simplified H-bridge configuration for OLA implementation during high-side current recirculation. When the voltage drop across the body diode of the MOSFET does not exhibit overshoot greater than the VOLA over VM between the time the low-side FET is switched off and the high side FET is switched on during an output PWM cycle. An open load is not detected if the energy stored in the inductor is high enough to cause an overshoot greater than the V_{OLA} over VM caused by the fly-back current flowing through the body diode of the high-side FET.

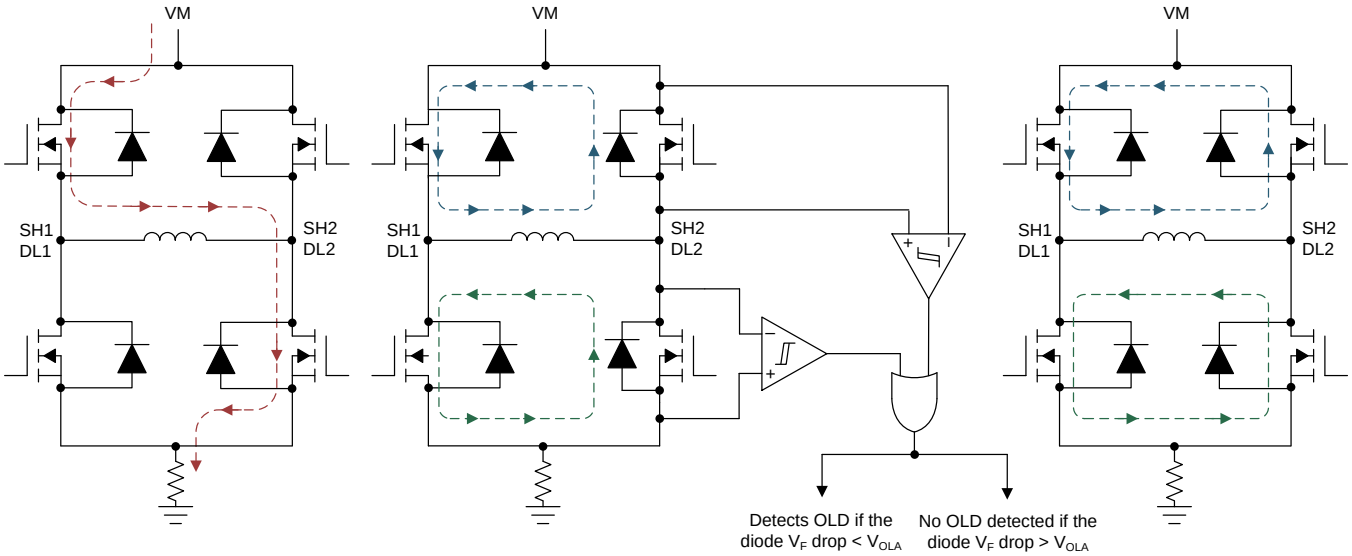

Figure 30. Circuit for Open Load Detection in Active Mode

NOTE

Depending on the operating conditions and on external circuitry, such as the output capacitors, an open load could be reported even though the load is present. This case might occur during a direction change or for small load currents respectively small PWM duty cycles. Therefore, TI recommends evaluating the open load diagnosis only in known suitable operating conditions and to ignore it otherwise.

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The device has a failure counter to avoid inadvertent triggering of the open load active diagnosis. Three consecutive occurrences of the internal open load signal must occur, essentially three consecutive PWM pulses without freewheeling detected, before an open load is reported through the nFAULT pin and in the respective SPI register.

In the SPI device, depending on the load configuration and the PWM sequence, OLA on one phase can latch all three OL_PH_x bits high. In that case, the OLP diagnostic can be initiated to determine which phase has the open load condition. The load connections shown in Figure 29 are not supported by OLA.

For OLA to function correctly, place capacitors between the motor phase node and GND. This capacitor is required for BLDC, bi-directional BDC and unidirectional BDC motors at the phase node. If a solenoid load is connected, as shown in Figure 15, the capacitor is not required. Size the capacitors according Equation 3. Make sure that the capacitor (C_{phase}) is placed on the PCB.

$$C_{phase} \geq \frac{V_{TH} \times C_{rss}}{V_{OLA(min)}} - C_{oss} \quad (3)$$

where

- V_{TH} is the threshold voltage of the MOSFET.
- $V_{OLA(min)}$ is 150 mV.

The values of C_{rss} and C_{oss} of the MOSFETs should be used for 0-V V_{DS}. Derating of C_{phase} must be considered when selecting the capacitance.

8.3.4.8 Offline Shorts Diagnostics

The device detects short-to-battery and short-to-ground conditions when the motor is not commutating. These offline diagnostics can be activated in the SPI device by setting the EN_SHT_TST bit high. Both the short-to-battery and short-to-ground diagnostics run when the EN_SHT_TST bit is set high. In the H/W device, these diagnostics run at power-up or when going from the sleep mode if the nDIAG pin is left unconnected or tied to GND. To disable the diagnostics in the H/W device, connect the nDIAG pin to the DVDD supply (or an external 3.3 V or 5 V rail). The short-to-supply diagnostic runs first (see Offline Short-to-Supply Diagnostic (SHT_BAT)) followed by the short-to-ground diagnostic (see Offline Short-to-Ground Diagnostic (SHT_GND)). In the SPI device, the duration for this diagnostics is selected through the OLP_SHTS_DLY register. In the H/W device, the duration is fixed to 2 ms.

8.3.4.8.1 Offline Short-to-Supply Diagnostic (SHT_BAT)

When the EN_SHT_TST bit is set high, all the pulldown current sources on the DLx pins are enabled. The voltage across each pulldown source is individually measured and compared to an internal threshold (V_{TH}). If the voltage across any of the current sources exceeds V_{TH}, the DRV8340-Q1 device flags that as a fault condition. The nFAULT pin is driven low, and in the SPI device the FAULT, OL_SHT, and the corresponding SHT_BAT_x bit is set. Figure 31 shows the internal circuit for the short to battery detection.

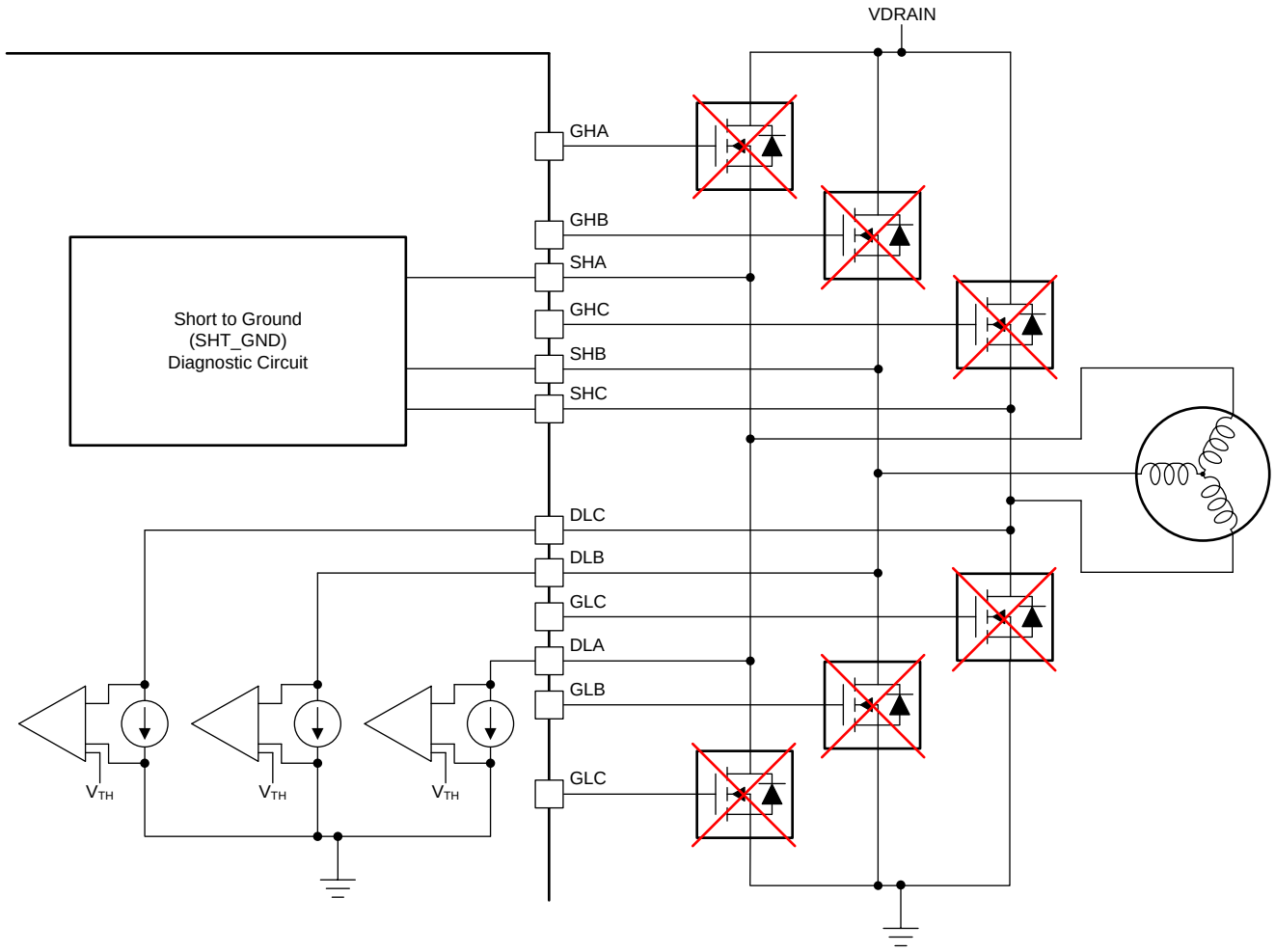

Figure 31. Offline Short-to-Supply Detection Circuit

In the SPI device, depending on the load configuration, SHT_BAT on one phase can latch all three SHT_BAT_x bits high. To determine which phase has a short-to-supply fault condition, the external MOSFETs can be enabled and the appropriate VDS_Lx fault bit is latched indicating the faulty phase node. SHT_BAT is not supported for load configurations shown in Figure 29.

8.3.4.8.2 Offline Short-to-Ground Diagnostic (SHT_GND)

When the EN_SHT_TST bit is set high, all the pullup current sources on the SHx pins are enabled. The voltage across each pullup source is individually measured and compared to an internal threshold (V_{TH}). If the voltage across any of the current sources exceeds V_{TH}, the DRV8340-Q1 device flags that as a fault condition. The nFAULT pin is driven low, and in the SPI device the FAULT, OL_SHT, and the corresponding SHT_GND_x bit is set. Figure 32 shows the internal circuit for the short-to-ground detection.

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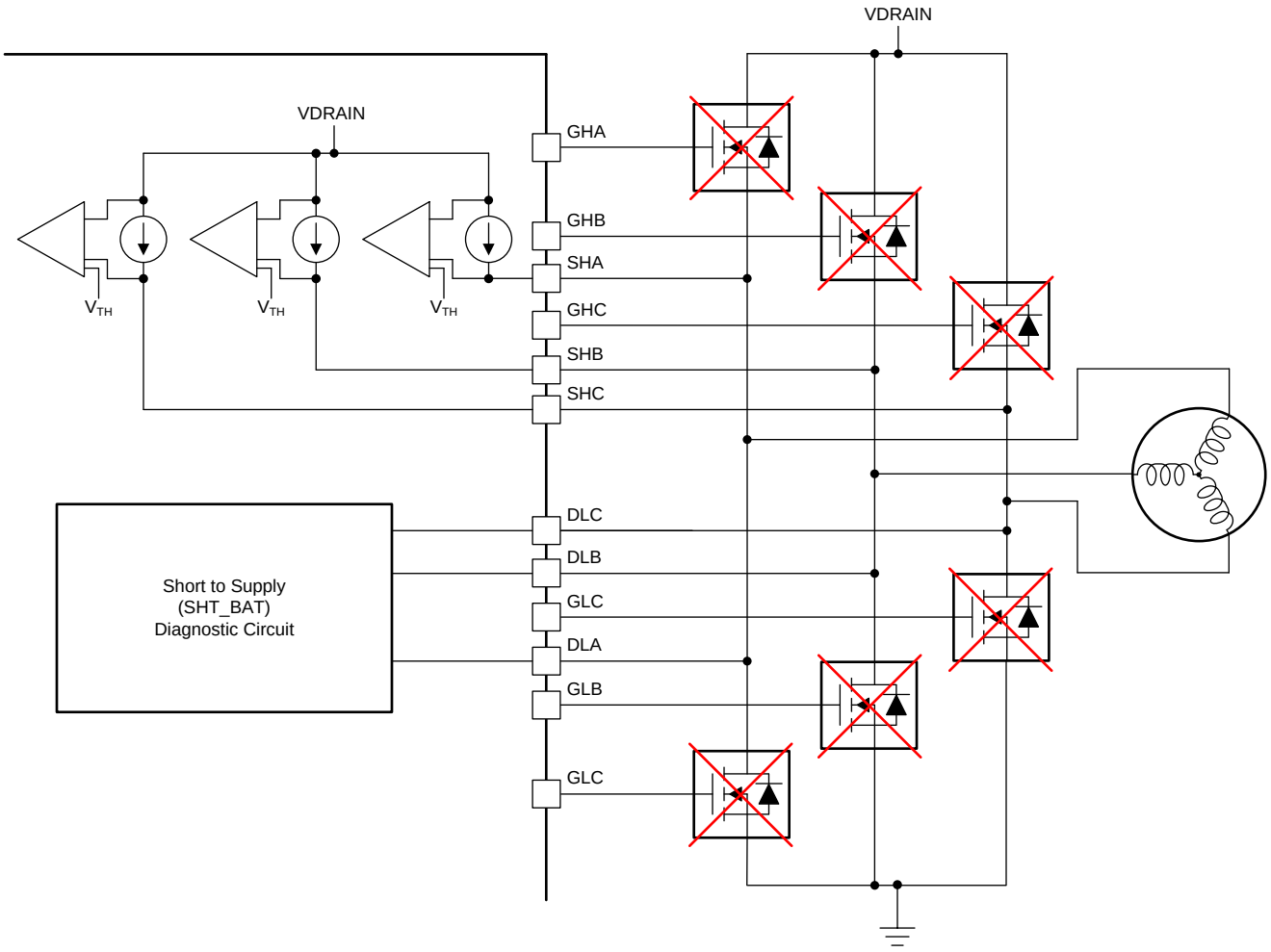

Figure 32. Offline Short-to-Ground Detection Circuit

In the SPI device, depending on the load configuration, SHT_GND on one phase can latch all three SHT_GND_x bits high. To determine which phase has a short-to-ground fault condition, the external MOSFETs can be enabled and the appropriate VDS_Hx fault bit is latched indicating the faulty phase node. SHT_GND is not supported for load configurations shown in Figure 29.

8.3.4.9 Reverse Supply Protection

The circuit in Figure 33 can be implemented to help protect the system from reverse supply conditions. This circuit requires the following additional components:

- N-channel MOSFET
- NPN BJT
- Diode
- 10-kΩ and 43-kΩ resistors

The VCP voltage with respect to VM supplies the gate-source voltage of N-channel MOSFET, and the voltage V_{VCP} depends on VM voltage. The characteristics of N-Channel MOSFET (e.g. gate threshold voltage) and the VM voltage range of the system need to be reviewed by the system integrator.

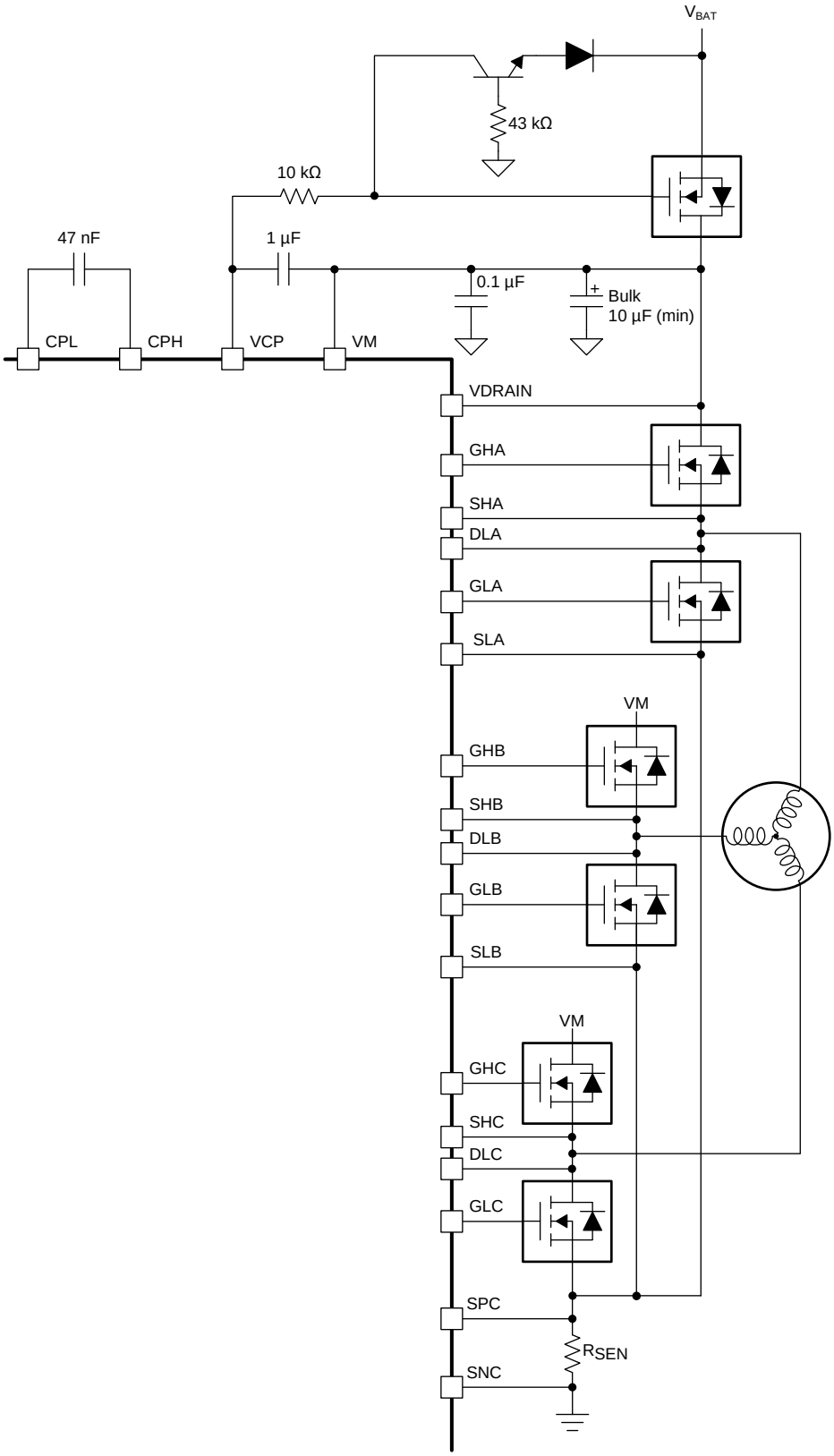

Figure 33. Reverse Supply Protection

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8.4 Device Functional Modes

8.4.1 Gate Driver Functional Modes

8.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV8340-Q1 device. When the ENABLE pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the charge pump is disabled, the DVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all external MOSFETs are disabled. The high-side gate pins, GHx, are pulled to the SHx pin by an internal resistor and the low-side gate pins, GLx, are pulled to the PGND pin by an internal resistor.

8.4.1.2 Operating Mode

When the ENABLE pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, low-side gate regulator, DVDD regulator, and SPI bus are active.

8.4.1.3 Fault Reset (CLR_FLT or ENABLE Reset Pulse)

In the case of device latched faults, the DRV8340-Q1 device goes to a partial shutdown state to help protect the external power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a result pulse to the ENABLE pin on either interface variant. The ENABLE reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the ENABLE pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks

8.5 Programming

This section applies only to the DRV8340-Q1 SPI devices.

8.5.1 SPI Communication

8.5.1.1 SPI

On DRV8340-Q1 SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16-bit word, with an 8-bit command and 8 bits of data. The SPI output data (SDO) word consists of 8-bit register data. The first 8 bits are don't care bits.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

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Programming (continued)

8.5.1.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 7 address bits, A (bits B14 through B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 5 bits are don't care bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 12. SDI Input Data Word Format

R/W	ADDRESS							DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	0	0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 13. SDO Output Data Word Format

R/W	DON'T CARE							DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

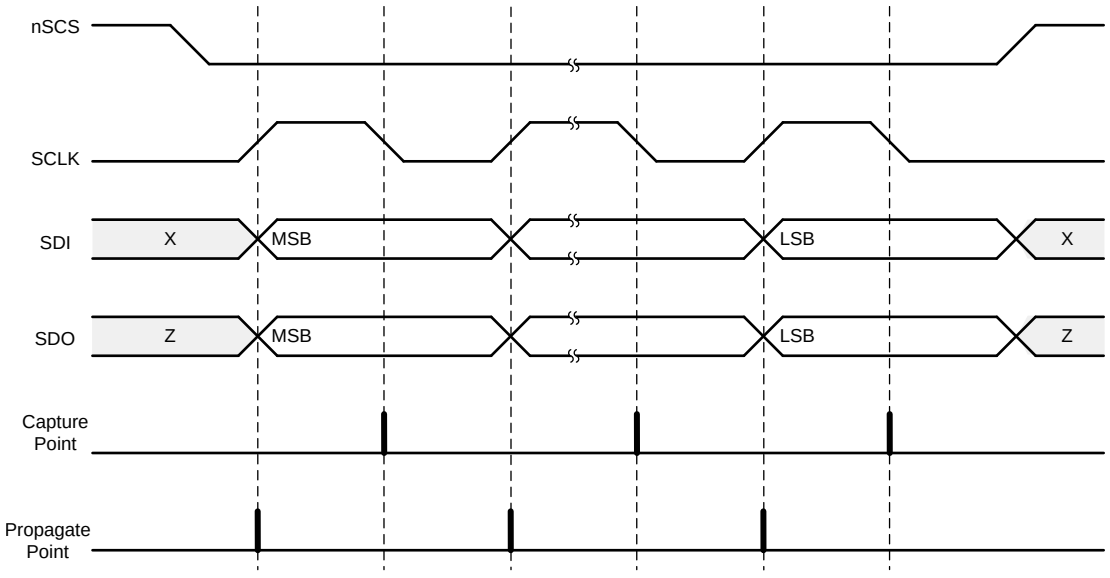

Figure 34. SPI Slave Timing Diagram

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8.6 Register Maps

This section applies only to the DRV8340-Q1 SPI devices.

NOTE

Do not modify reserved registers or addresses not listed in the register map (). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0. To help prevent erroneous SPI writes from the master controller, set the LOCK bits to lock the SPI registers.

Table 14. DRV8340-Q1 Register Map

Register Name	7	6	5	4	3	2	1	0	Access Type	Address
FAULT Status	FAULT	GDF	CPUV	UVLO	OCP	OTW	OTSD	OL_SHT	R	0x00
DIAG Status A	RSVD	SHT_GND_A	SHT_BAT_A	OL_PH_A	VGS_LA	VGS_HA	VDS_LA	VDS_HA	R	0x01
DIAG Status B	RSVD	SHT_GND_B	SHT_BAT_B	OL_PH_B	VGS_LB	VGS_HB	VDS_LB	VDS_HB	R	0x02
DIAG Status C	RSVD	SHT_GND_C	SHT_BAT_C	OL_PH_C	VGS_LC	VGS_HC	VDS_LC	VDS_HC	R	0x03
IC1 Control	CLR_FLT	PWM_MODE			1PWM_COM	1PWM_DIR	1PWM_BRAKE		RW	0x04
IC2 Control	OTSD_MODE	OLP_SHTS_DLY		EN_SHT_TST	EN_OLP	EN_OLA_C	EN_OLA_B	EN_OLA_A	RW	0x05
IC3 Control	IDRIVEP_LA				IDRIVEP_HA				RW	0x06
IC4 Control	IDRIVEP_LB				IDRIVEP_HB				RW	0x07
IC5 Control	IDRIVEP_LC				IDRIVEP_HC				RW	0x08
IC6 Control	VDS_LVL_LA				VDS_LVL_HA				RW	0x09
IC7 Control	VDS_LVL_LB				VDS_LVL_HB				RW	0x0A
IC8 Control	VDS_LVL_LC				VDS_LVL_HC				RW	0x0B
IC9 Control	COAST	TRETRY		DEAD_TIME		TDRIVE_MAX	TDRIVE		RW	0x0C
IC10 Control	LOCK			DIS_CPUV	DIS_GDF	OCP_DEG			RW	0x0D
IC11 Control	RSVD	OTW_REP	CBC	DIS_VDS_C	DIS_VDS_B	DIS_VDS_A	OCP_MODE		RW	0x0E
IC12 Control	RSVD	RSVD	RSVD		RSVD		RSVD		RW	0x0F
IC13 Control	RSVD	RSVD	RSVD		RSVD		RSVD		RW	0x10
IC14 Control	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RW	0x11

Complex bit access types are encoded to fit into small table cells. Table 15 shows the codes that are used for access types in this section.

Table 15. Status Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 Status Registers

Table 16 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 16 should be considered as reserved locations and the register contents should not be modified.

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers.

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Table 16. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT Status	Go
0x01	DIAG Status A	Go
0x02	DIAG Status B	Go
0x03	DIAG Status C	Go

8.6.1.1 FAULT Status Register (Address = 0x00) [reset = 0x00]

FAULT Status is shown in Figure 35 and described in Table 17.

Figure 35. FAULT Status Register

7	6	5	4	3	2	1	0
FAULT	GDF	CPUV	UVLO	OCP	OTW	OTSD	OL_SHT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 17. FAULT Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	Logic OR of FAULT status registers
6	GDF	R	0b	Indicates gate drive fault condition
5	CPUV	R	0b	Indicates charge pump undervoltage fault condition
4	UVLO	R	0b	Indicates undervoltage lockout fault condition
3	OCP	R	0b	Indicated overcurrent fault condition either by VDS
2	OTW	R	0b	Indicates overtemperature warning
1	OTSD	R	0b	Indicates overtemperature shutdown
0	OL_SHT	R	0b	Indicates open load detection, or offline short-to-supply or GND detection

8.6.1.2 DIAG Status A Register (Address = 0x01) [reset = 0x00]

DIAG Status A is shown in Figure 36 and described in Table 18.

Figure 36. DIAG Status A Register

7	6	5	4	3	2	1	0
RSVD	SHT_GND_A	SHT_BAT_A	OL_PH_A	VGS_LA	VGS_HA	VDS_LA	VDS_HA
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 18. DIAG Status A Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved.
6	SHT_GND_A	R	0b	Indicates offline short-to-ground fault in Phase A
5	SHT_BAT_A	R	0b	Indicates offline short to battery fault in Phase A
4	OL_PH_A	R	0b	Indicates open load fault in Phase A
3	VGS_LA	R	0b	Indicates gate drive fault on the A low-side MOSFET
2	VGS_HA	R	0b	Indicates gate drive fault on the A high-side MOSFET
1	VDS_LA	R	0b	Indicates VDS overcurrent fault on the A low-side MOSFET
0	VDS_HA	R	0b	Indicates VDS overcurrent fault on the A high-side MOSFET

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8.6.1.3 DIAG Status B Register (Address = 0x02) [reset = 0x00]

DIAG Status B is shown in Figure 37 and described in Table 19.

Figure 37. DIAG Status B Register

7	6	5	4	3	2	1	0
RSVD	SHT_GND_B	SHT_BAT_B	OL_PH_B	VGS_LB	VGS_HB	VDS_LB	VDS_HB
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 19. DIAG Status B Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved
6	SHT_GND_B	R	0b	Indicates offline short-to-ground fault in Phase B
5	SHT_BAT_B	R	0b	Indicates offline short to battery fault in Phase B
4	OL_PH_B	R	0b	Indicates open load fault in Phase B
3	VGS_LB	R	0b	Indicates gate drive fault on the B low-side MOSFET
2	VGS_HB	R	0b	Indicates gate drive fault on the B high-side MOSFET
1	VDS_LB	R	0b	Indicates VDS overcurrent fault on the B low-side MOSFET
0	VDS_HB	R	0b	Indicates VDS overcurrent fault on the B high-side MOSFET

8.6.1.4 DIAG Status C Register (address = 0x03) [reset = 0x00]

DIAG Status C iss shown in Figure 38 and described in Table 20.

Figure 38. DIAG Status C Register

7	6	5	4	3	2	1	0
RSVD	SHT_GND_C	SHT_BAT_C	OL_PH_C	VGS_LC	VGS_HC	VDS_LC	VDS_HC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 20. DIAG Status C Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved
6	SHT_GND_C	R	0b	Indicates offline short-to-ground fault in Phase C
5	SHT_BAT_C	R	0b	Indicates offline short to battery fault in Phase C
4	OL_PH_C	R	0b	Indicates open load fault in Phase C
3	VGS_LC	R	0b	Indicates gate drive fault on the C low-side MOSFET
2	VGS_HC	R	0b	Indicates gate drive fault on the C high-side MOSFET
1	VDS_LC	R	0b	Indicates VDS overcurrent fault on the C low-side MOSFET
0	VDS_HC	R	0b	Indicates VDS overcurrent fault on the C high-side MOSFET

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8.6.2 Control Registers

Table 21 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 21 should be considered as reserved locations and the register contents should not be modified.

The IC control registers are used to configure the device. Control registers are read and write capable.

Table 21. Control Registers Summary Table

Address	Register Name	Section
0x04	IC1 Control	Go
0x05	IC2 Control	Go
0x06	IC3 Control	Go
0x07	IC4 Control	Go
0x08	IC5 Control	Go
0x09	IC6 Control	Go
0x0A	IC7 Control	Go
0x0B	IC8 Control	Go
0x0C	IC9 Control	Go
0x0D	IC10 Control	Go
0x0E	IC11 Control	Go
0x0F	IC12 Control	Go
0x10	IC13 Control	Go
0x11	IC14 Control	Go

8.6.2.1 IC1 Control Register (Address = 0x04) [reset = 0x00]

IC1 Control is shown in Figure 39 and described in Table 22.

Figure 39. IC1 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	PWM_MODE			1PWM_COM	1PWM_DIR	1PWM_BRAKE	
R/W-0b	R/W-000b			R/W-0b	R/W-0b	R/W-00b	

Table 22. IC1 Control Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write a 1 to this bit to clear all latched fault bits. This bit automatically resets after being written
6-4	PWN_MODE	R/W	000b	**000b = 6x PWM mode** 001b = 3x PWM mode 010b = 1x PWM mode 011b = Independent half-bridge (for all phases) 100b = Phases A and B are independent half-bridges, Phase C is independent FET 101b = Phases B and C are independent half-bridges, Phase A is independent FET 110b = Phase A is independent half-bridge, Phases B and C are independent FET 111b =Independent FET (for all phases)
3	1PWM_COM	R/W	0b	**0b = 1x PWM mode uses synchronous rectification** 1b = 1x PWM mode uses asynchronous rectification (diode freewheeling)
2	1PWM_DIR	R/W	0b	In 1x PWM mode this bit is OR'ed with the INHC (DIR) input

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Table 22. IC1 Control Field Descriptions (continued)

Bit	Field	Type	Default	Description
1-0	1PWM_BRAKE	R/W	00b	**00b = Outputs follow commanded inputs** 01b = Turn on all three low-side MOSFETs 10b = Turn on all three high-side MOSFETs 11b = Turn off all six MOSFETs (coast)

8.6.2.2 IC2 Control Register (address = 0x05) [reset = 0x40]

IC2 Control is shown in Figure 40 and described in Table 23.

Figure 40. IC2 Control Register

7	6	5	4	3	2	1	0
OTSD_MODE	OLP_SHTS_DLY		EN_SHT_TST	EN_OLP	EN_OLA_C	EN_OLA_B	EN_OLA_A
R/W-0b	R/W-10b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 23. IC2 Control Field Descriptions

Bit	Field	Type	Default	Description
7	OTSD_MODE	R/W	0b	**0b = Overtemperature condition will cause a latched fault** 1b = Overtemperature condition will cause an automatic recovery when the fault condition is removed
6-5	OLP_SHTS_DLY	R/W	10b	00b = OLP delay is 0.25 ms and Shorts test delay is 0.1 ms 01b = OLP delay is 1.25 ms and Shorts test delay is 0.5 ms **10b = OLP delay is 5 ms and Shorts test delay is 2 ms** 11b = OLP delay is 11.5 ms and Shorts test delay is 4.4 ms
4	EN_SHT_TST	R/W	0b	Write a 1 to enable offline short to battery and ground diagnoses
3	EN_OLP	R/W	0b	Write a 1 to enable open load diagnostic in standby mode. When open load test is complete EN_OLP returns to the default setting
2	EN_OLA_C	R/W	0b	Write a 1 to enable open load active diagnostic on Phase C
1	EN_OLA_B	R/W	0b	Write a 1 to enable open load active diagnostic on Phase B
0	EN_OLA_A	R/W	0b	Write a 1 to enable open load active diagnostic on Phase A

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8.6.2.3 IC3 Control Register (Address = 0x06) [reset = 0xFF]

IC3 Control is shown in Figure 41 and described in Table 24.

Figure 41. IC3 Control Register

7	6	5	4	3	2	1	0
IDRIVEP_LA				IDRIVEP_HA			
R/W-1111b				R/W-1111b			

Table 24. IC3 Control Field Descriptions

Bit	Field	Type	Default	Description
7-4	IDRIVEP_LA	R/W	1111b	0000b = 1.5 mA 0001b = 3.5 mA 0010b = 5 mA 0011b = 10 mA 0100b = 15 mA 0101b = 50 mA 0110b = 60 mA 0111b = 65 mA 1000b = 200 mA 1001b = 210 mA 1010b = 260 mA 1011b = 265 mA 1100b = 735 mA 1101b = 800 mA 1110b = 935 mA **1111b = 1000 mA**
3-0	IDRIVEP_HA	R/W	1111b	0000b = 1.5 mA 0001b = 3.5 mA 0010b = 5 mA 0011b = 10 mA 0100b = 15 mA 0101b = 50 mA 0110b = 60 mA 0111b = 65 mA 1000b = 200 mA 1001b = 210 mA 1010b = 260 mA 1011b = 265 mA 1100b = 735 mA 1101b = 800 mA 1110b = 935 mA **1111b = 1000 mA**

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8.6.2.4 IC4 Control Register (Address = 0x07) [reset = 0xFF]

IC4 Control is shown in Figure 42 and described in Table 25.

Figure 42. IC4 Control Register

7	6	5	4	3	2	1	0
IDRIVEP_LB				IDRIVEP_HB			
R/W-1111b				R/W-1111b			

Table 25. IC4 Control Field Descriptions

Bit	Field	Type	Default	Description
7-4	IDRIVEP_LB	R/W	1111b	0000b = 1.5 mA 0001b = 3.5 mA 0010b = 5 mA 0011b = 10 mA 0100b = 15 mA 0101b = 50 mA 0110b = 60 mA 0111b = 65 mA 1000b = 200 mA 1001b = 210 mA 1010b = 260 mA 1011b = 265 mA 1100b = 735 mA 1101b = 800 mA 1110b = 935 mA **1111b = 1000 mA**
3-0	IDRIVEP_HB	R/W	1111b	0000b = 1.5 mA 0001b = 3.5 mA 0010b = 5 mA 0011b = 10 mA 0100b = 15 mA 0101b = 50 mA 0110b = 60 mA 0111b = 65 mA 1000b = 200 mA 1001b = 210 mA 1010b = 260 mA 1011b = 265 mA 1100b = 735 mA 1101b = 800 mA 1110b = 935 mA **1111b = 1000 mA**

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8.6.2.5 IC5 Control Register (Address = 0x08) [reset = 0xFF]

IC5 Control is shown in Figure 43 and described in Table 26.

Figure 43. IC5 Control Register

7	6	5	4	3	2	1	0
IDRIVEP_LC				IDRIVEP_HC			
R/W-1111b				R/W-1111b			

Table 26. IC5 Control Field Descriptions

Bit	Field	Type	Default	Description
7-4	IDRIVEP_LC	R/W	1111b	0000b = 1.5 mA 0001b = 3.5 mA 0010b = 5 mA 0011b = 10 mA 0100b = 15 mA 0101b = 50 mA 0110b = 60 mA 0111b = 65 mA 1000b = 200 mA 1001b = 210 mA 1010b = 260 mA 1011b = 265 mA 1100b = 735 mA 1101b = 800 mA 1110b = 935 mA **1111b = 1000 mA**
3-0	IDRIVEP_HC	R/W	1111b	0000b = 1.5 mA 0001b = 3.5 mA 0010b = 5 mA 0011b = 10 mA 0100b = 15 mA 0101b = 50 mA 0110b = 60 mA 0111b = 65 mA 1000b = 200 mA 1001b = 210 mA 1010b = 260 mA 1011b = 265 mA 1100b = 735 mA 1101b = 800 mA 1110b = 935 mA **1111b = 1000 mA**

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8.6.2.6 IC6 Control Register (Address = 0x09) [reset = 0x99]

IC6 Control is shown in Figure 44 and described in Table 27.

Figure 44. IC6 Control Register

7	6	5	4	3	2	1	0
VDS_LVL_LA				VDS_LVL_HA			
R/W-1001b				R/W-1001b			

Table 27. IC6 Control Field Descriptions

Bit	Field	Type	Default	Description
7-4	VDS_LVL_LA	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V
3-0	VDS_LVL_HA	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V

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8.6.2.7 IC7 Control Register (Address = 0x0A) [reset = 0x99]

IC7 Control is shown in Figure 45 and described in Table 28.

Figure 45. IC7 Control Register

7	6	5	4	3	2	1	0
VDS_LVL_LB				VDS_LVL_HB			
R/W-1001b				R/W-1001b			

Table 28. IC7 Control Field Descriptions

Bit	Field	Type	Default	Description
7-4	VDS_LVL_LB	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V
3-0	VDS_LVL_HB	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V

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8.6.2.8 IC8 Control Register (Address = 0x0B) [reset = 0x99]

IC8 control is shown in Figure 46 and described in Table 29.

Figure 46. IC8 Control Register

7	6	5	4	3	2	1	0
VDS_LVL_LC				VDS_LVL_HC			
R/W-1001b				R/W-1001b			

Table 29. IC8 Control Field Descriptions

Bit	Field	Type	Default	Description
7-4	VDS_LVL_LC	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V
3-0	VDS_LVL_HC	R/W	1001b	0000b = 0.06 V 0001b = 0.13 V 0010b = 0.2 V 0011b = 0.26 V 0100b = 0.31 V 0101b = 0.45 V 0110b = 0.53 V 0111b = 0.6 V 1000b = 0.68 V **1001b = 0.75 V** 1010b = 0.94 V 1011b = 1.13 V 1100b = 1.3 V 1101b = 1.5 V 1110b = 1.7 V 1111b = 1.88 V

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8.6.2.9 IC9 Control Register (Address = 0x0C) [reset = 0x2F]

IC9 Control is shown in Figure 47 and described in Table 30.

Figure 47. IC9 Control Register

7	6	5	4	3	2	1	0
COAST	TRETRY		DEAD_TIME		TDRIVE_MAX	TDRIVE	
R/W-0b	R/W-01b		R/W-01b		R/W-1b	R/W-11b	

Table 30. IC9 Control Field Descriptions

Bit	Field	Type	Default	Description
7	COAST	R/W	0b	Write a 1 to this bit to put all the MOSFETs in the Hi-Z state
6-5	TRETRY	R/W	01b	00b = 2 ms **01b = 4 ms** 10b = 6 ms 11b = 8 ms
4-3	DEAD_TIME	R/W	01b	00b = 500 ns **01b = 1000 ns** 10b = 2000 ns 11b = 4000 ns
2	TDRIVE_MAX	R/W	1b	Write a 0 to this bit to disable the maximum t_{DRIVE} time of 20 µs. This bit is automatically enabled when IDRIVE = 0000b, 0001b, 0010b, or 0011b is selected
1-0	TDRIVE	R/W	11b	00b = 500 ns peak gate-current drive time 01b = 1000 ns peak gate-current drive time 10b = 2000 ns peak gate-current drive time **11b = 3000 ns peak gate-current drive time**

8.6.2.10 IC10 Control Register (Address = 0x0D) [reset = 0x61]

IC10 Control is shown in Figure 48 and described in Table 31.

Figure 48. IC10 Control Register

7	6	5	4	3	2	1	0
LOCK			DIS_CPUV	DIS_GDF	OCP_DEG		
R/W-011b			R/W-0b	R/W-0b	R/W-001b		

Table 31. IC10 Control Field Descriptions

Bit	Field	Type	Default	Description
7-5	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x04h bit 7 (CLR_FLT). Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
4	DIS_CPUV	R/W	0b	**0b = Charge-pump undervoltage lockout fault is enabled** 1b = Charge-pump undervoltage lockout fault is disabled
3	DIS_GDF	R/W	0b	**0b = Gate drive fault is enabled** 1b = Gate drive fault is disabled

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Table 31. IC10 Control Field Descriptions (continued)

Bit	Field	Type	Default	Description
2-0	OCP_DEG	R/W	001b	000b = 2.5 µs **001b = 4.75 µs** 010b = 6.75 µs 011b = 8.75 µs 100b = 10.25 µs 101b = 11.5 µs 110b = 16.5 µs 111b = 20.5 µs

8.6.2.11 IC11 Control Register (Address = 0x0E) [reset = 0x00]

IC11 Control is shown in Figure 49 and described in Table 32.

Figure 49. IC11 Control Register

7	6	5	4	3	2	1	0
RSVD	OTW_REP	CBC	DIS_VDS_C	DIS_VDS_B	DIS_VDS_A	OCP_MODE	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b	

Table 32. IC11 Control Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6	OTW_REP	R/W	0b	**0b = Overtemperature warning is not reported on nFAULT** 1b = Overtemperature warning is reported on nFAULT
5	CBC	R/W	0b	In retry OCP_MODE, for both VDS_OCP, the fault is automatically cleared when a PWM input is given
4	DIS_VDS_C	R/W	0b	Write a 1 to this bit to disable VDS_OCP for MOSFETs in Phase C
3	DIS_VDS_B	R/W	0b	Write a 1 to this bit to disable VDS_OCP for MOSFETs in Phase B
2	DIS_VDS_A	R/W	0b	Write a 1 to this bit to disable VDS_OCP for MOSFETs in Phase A
1-0	OCP_MODE	R/W	00b	**00b = Overcurrent causes a latched fault** 01b = Overcurrent causes an automatic retrying fault 10b = Overcurrent is report only but no action is taken 11b = Overcurrent is not reported and no action is taken

8.6.2.12 IC12 Control Register (Address = 0x0F) [reset = 0x2A]

IC12 Control is shown in and described in .

Figure 50. IC12 Control Register

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD		RSVD		RSVD	
R/W-0b	R/W-0b	R/W-10b		R/W-10b		R/W-10b	

Table 33. IC12 Control Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved. Keep the default value 0b.
6	RSVD	R/W	0b	Reserved.
5-4	RSVD	R/W	10b	Reserved.

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Table 33. IC12 Control Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-2	RSVD	R/W	10b	Reserved.
1-0	RSVD	R/W	10b	Reserved.

8.6.2.13 IC13 Control Register (Address = 0x10) [reset = 0x7F]

IC13 Control is shown in and described in .

Figure 51. IC13 Control Register

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD		RSVD		RSVD	
R/W-0b	R/W-1b	R/W-11b		R/W-11b		R/W-11b	

Table 34. IC13 Control Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6	RSVD	R/W	1b	Reserved
5-4	RSVD	R/W	11b	Reserved
3-2	RSVD	R/W	11b	Reserved
1-0	RSVD	R/W	11b	Reserved

8.6.2.14 IC14 Control Register (Address = 0x10) [reset = 0x00]

IC14 Control is shown in and described in .

Figure 52. IC14 Control Register

7	6	5	4	3	2	1	0
RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 35. IC14 Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	RSVD	R/W	00b	Reserved
5	RSVD	R/W	0b	Reserved
4	RSVD	R/W	0b	Reserved
3	RSVD	R/W	0b	Reserved
2	RSVD	R/W	0b	Reserved
1	RSVD	R/W	0b	Reserved
0	RSVD	R/W	0b	Reserved

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8340-Q1 device is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Typical Application* section highlight how to use and configure the DRV8340-Q1 device.

9.2 Typical Application

9.2.1 Primary Application

The DRV8340-Q1 SPI device is used in this application example.

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Typical Application (continued)

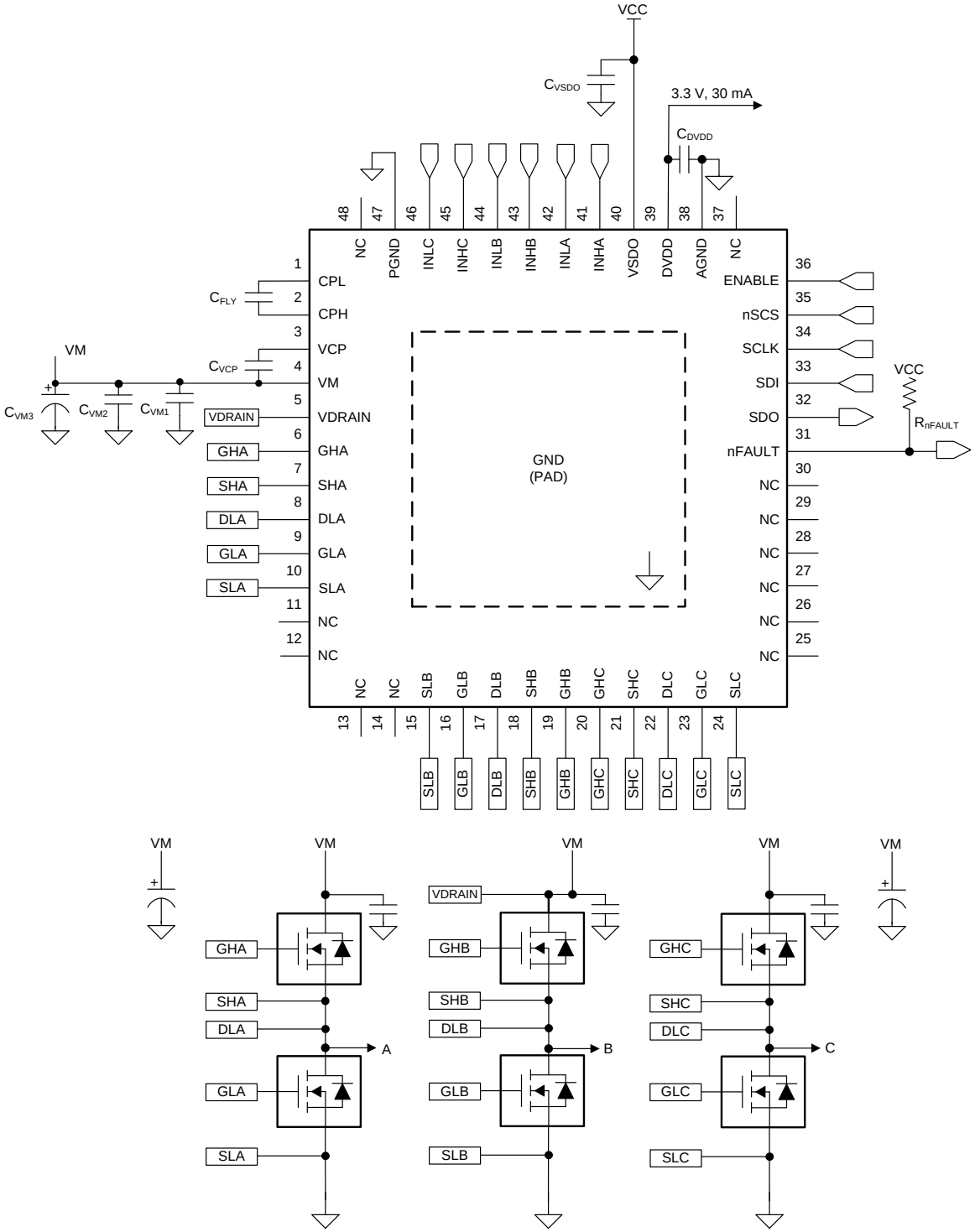

Figure 53. Primary Application Schematic

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Typical Application (continued)

9.2.1.1 Design Requirements

lists the example input parameters for the system design.

Table 36. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	24 V
Supply voltage range		8 V to 45 V
MOSFET part number		CSD18536KCS
MOSFET total gate charge	Q_g	83 nC (typical) at V_{VGS} = 10 V
MOSFET gate to drain charge	Q_{gd}	14 nC (typical)
Target output rise time	t_r	1000 ns
PWM Frequency	f_{PWM}	10 kHz
Maximum motor current	I_{max}	100 A
Winding sense current range	I_{SENSE}	–40 A to +40 A
Motor RMS current	I_{RMS}	28.3 A
System ambient temperature	T_A	–40°C to 125°C

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External MOSFET Support

The DRV8340-Q1 MOSFET support is based on the capacity of the charge pump and PWM switching frequency of the output. For a quick calculation of MOSFET driving capacity, use Equation 4 and Equation 5 for three phase BLDC motor applications.

Trapezoidal 120° Commutation: $I_{VCP} > Q_g \times f_{PWM}$

where

- f_{PWM} is the maximum desired PWM switching frequency.
- I_{VCP} is the charge pump capacity, which depends on the VM pin voltage.
- The multiplier based on the commutation control method, may vary based on implementation. (4)

Sinusoidal 180° Commutation: $I_{VCP} > 3 \times Q_g \times f_{PWM}$ (5)

9.2.1.2.1.1 Example

If a system with a V_{VM} voltage of 8 V (I_{VCP} = 15 mA) uses a maximum PWM switching frequency of 10 kHz, then the charge pump can support MOSFETs using trapezoidal commutation with a Q_g less than 750 nC, and MOSFETs using sinusoidal commutation with a Q_g less than 250 nC.

9.2.1.2.2 IDRIVE Configuration

The strength of the gate drive current, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on completely within the t_{DRIVE} time and a gate drive fault may be asserted. Additionally, slow rise and fall times result in higher switching power losses. TI recommends adjusting these values in the system with the required external MOSFETs and motor to determine the best possible setting for any application.

The I_{DRIVEP} and I_{DRIVEN} current for both the low-side and high-side MOSFETs are independently adjustable on SPI devices through the SPI registers. On hardware interface devices, both source and sink settings are selected at the same time on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge Q_{gd}, desired rise time (t_r), and a desired fall time (t_f), use Equation 6 and Equation 7 to calculate the value of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} > Q_{gd} \times t_r \quad (6)$$

$$I_{DRIVEN} = 2 \times I_{DRIVEP} \quad (7)$$

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9.2.1.2.2.1 Example

Use Equation 8 to calculate the value of I_{DRIVEP} for a gate-to-drain charge of 14 nC and a rise time from 100 to 300 ns.

$$I_{DRIVEP} = \frac{12\ nC}{1000\ ns} 14\ mA \tag{8}$$

Select an I_{DRIVEP} value that is close to 14 mA which will set the I_{DRIVEN} value close to 28 mA. For this example, the value of I_{DRIVEP} was selected as 15 mA.

9.2.1.2.3 V_{DS} Overcurrent Monitor Configuration

The V_{DS} monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs as shown in Equation 9.

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max} \tag{9}$$

9.2.1.2.3.1 Example

The goal of this example is to set the V_{DS} monitor to trip at a current greater than 100 A. According to the *CSD18536KCS 60 V N-Channel NexFET™ Power MOSFET* data sheet, the $R_{DS(on)}$ value is 1.8 times higher at 175°C, and the maximum $R_{DS(on)}$ value at a V_{GS} of 10 V is 1.6 mΩ. From these values, the approximate worst-case value of $R_{DS(on)}$ is 1.8 × 1.6 mΩ = 2.88 mΩ.

Using Equation 9 with a value of 2.88 mΩ for $R_{DS(on)}$ and a worst-case motor current of 100 A, Equation 10 shows the calculated the value of the V_{DS} monitors.

$$V_{DS\_OCP} > 100\ A \times 2.88\ m\Omega$$

$$V_{DS\_OCP} > 0.288\ V \tag{10}$$

For this example, the value of V_{DS_OCP} was selected as 0.31 V.

The SPI devices allow for adjustment of the deglitch time for the V_{DS} overcurrent monitor. The deglitch time can be set to 2 µs, 4 µs, 6 µs, 8 µs, 10 µs, 12 µs, 16 µs, or 20 µs.

9.2.1.2.4 Design consideration of low-side gate drive (IDRIVE, GLx, SLx)

The VGLS linear regulator of low-side gate driver is biased with respect to AGND. Since the external FET is referenced to bridge ground, any difference between the two grounds may cause the effective gate-source voltage on the low-side MOSFET to increase during high current switching events.

Steps can be taken during the design stage to reduce the severity of this effect

- Avoid excessively fast switching transients in the bridge (<100ns slew rates on the phase node)
- Ensure low inductance between SLx pin to MOSFET ground
- Ensure low inductance in the path from GLx pin to MOSFET Gate . As a guidance, the below relationships Equation 11 may be used to estimate the highest V_{GSL} expected. The 1V term in the equation is required for additional margin.

$$V_{GSL\_SWITCHING} = V_{GSL} + 1V + \frac{I_{DRIVEP}^2}{Q_g} \times L_{gate} \tag{11}$$

where

- $V_{GSL\_SWITCHING}$ is the effective gate-source voltage on the low-side MOSFET
- V_{GSL} is the low-side gate drive voltage with no output load of GLx
- I_{DRIVEP} is the peak source gate current
- Q_g is the total gate charge of MOSFET
- L_{gate} is the parasitic inductance in the path from GLx pin to MOSFET gate

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9.2.1.2.5 External Components

lists the recommended external components.

Table 37. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{FLY}	CPH	CPL	47-nF ceramic capacitor X5R or X7R rated for VM(1)
C_{VCP}	VCP	VM	1-µF ceramic capacitor X5R or X7R rated for VCP – VM (1)
C_{VM1}	VM	PGND	0.1-µF ceramic capacitor X5R or X7R rated for VM(1)
C_{VM2}	VM	PGND	4.7-µF ceramic capacitor X5R or X7R rated for VM(1)
C_{VM3}	VM	PGND	> 10-µF electrolytic capacitor rated for VM(1)
C_{DVDD}	DVDD	AGND	1-µF ceramic capacitor X5R or X7R rated for DVDD(1)
C_{VSDO}	VSDO	AGND	0.1-µF ceramic capacitor X5R or X7R rated for VSDO(1). DRV8340S only
R_{nFAULT}	nFAULT	VCC(2)	2.5 – 10 kΩ pulled up the MCU I/O (VCC) power supply

(1) The effective capacitance of ceramic capacitors varies with DC operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50% at the extremes of the operating voltage. The system designer must review the capacitor characteristics and select the component accordingly.
(2) The VCC pin is not a pin on the DRV8340-Q1 device, but a VCC supply voltage pullup is required for the open-drain output, nFAULT. These pins can also be pulled up to DVDD.

9.2.1.3 Application Curves

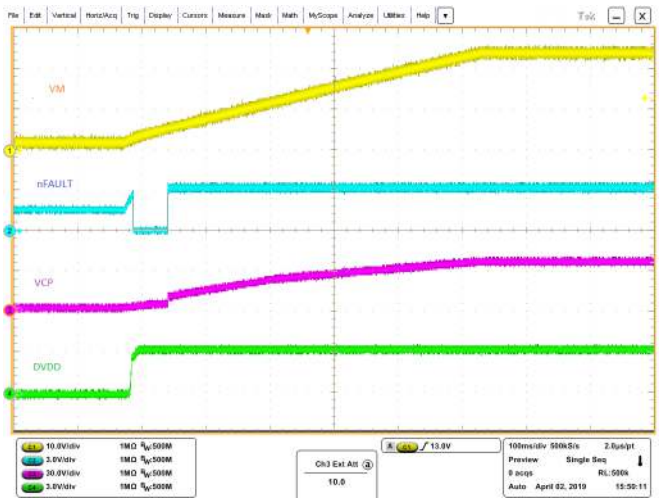

Figure 54. Device Power Up Sequence Waveform

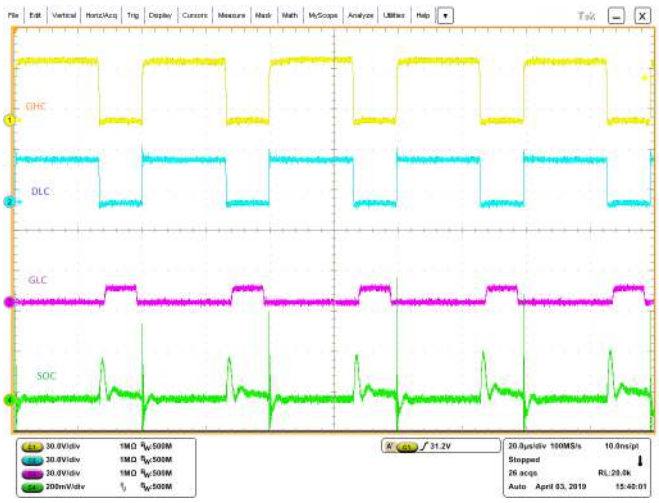

Figure 55. BLDC Motor Commutation (1)

(1) SOC is available for DRV8343-Q1.

10 Power Supply Recommendations

The DRV8340-Q1 device is designed to operate from an input voltage supply (VM) range from 6 V to 60 V.

10.1 Power Supply Consideration in Generator Mode

When the motor shaft of BLDC or PMSM motor is turned by an external force, the motor windings will generate a voltage on the motor inputs. This condition is known as generator mode or motor back-drive. In the generator mode, a positive voltage can be observed on SHx pins of the device. If there is a switch between VDRAIN and VM (SW_{VDRAIN} in Figure 56) and the following conditions exist in the system, the absolute max voltage of VCP with respect to VM needs to be reviewed;

- Generator mode
- SW_{VDRAIN} is off
- VM and VCP are low voltage (e.g. VM = 0V)

If SHx voltage (V_{SHx}) exceeds VCP voltage, the VCP voltage starts following V_{SHx} because of the device internal diodes D1 and D2 (or D3). If VCP - VM voltage exceeds the absolute max voltage of DRV8340-Q1, the ESD diode D4 starts conducting and results in a big current from SHx to VM through the diodes D2, D1 and D4. To avoid this condition, it is recommended to add an external diode D_{VDRAIN_VM} between VDRAIN and VM.

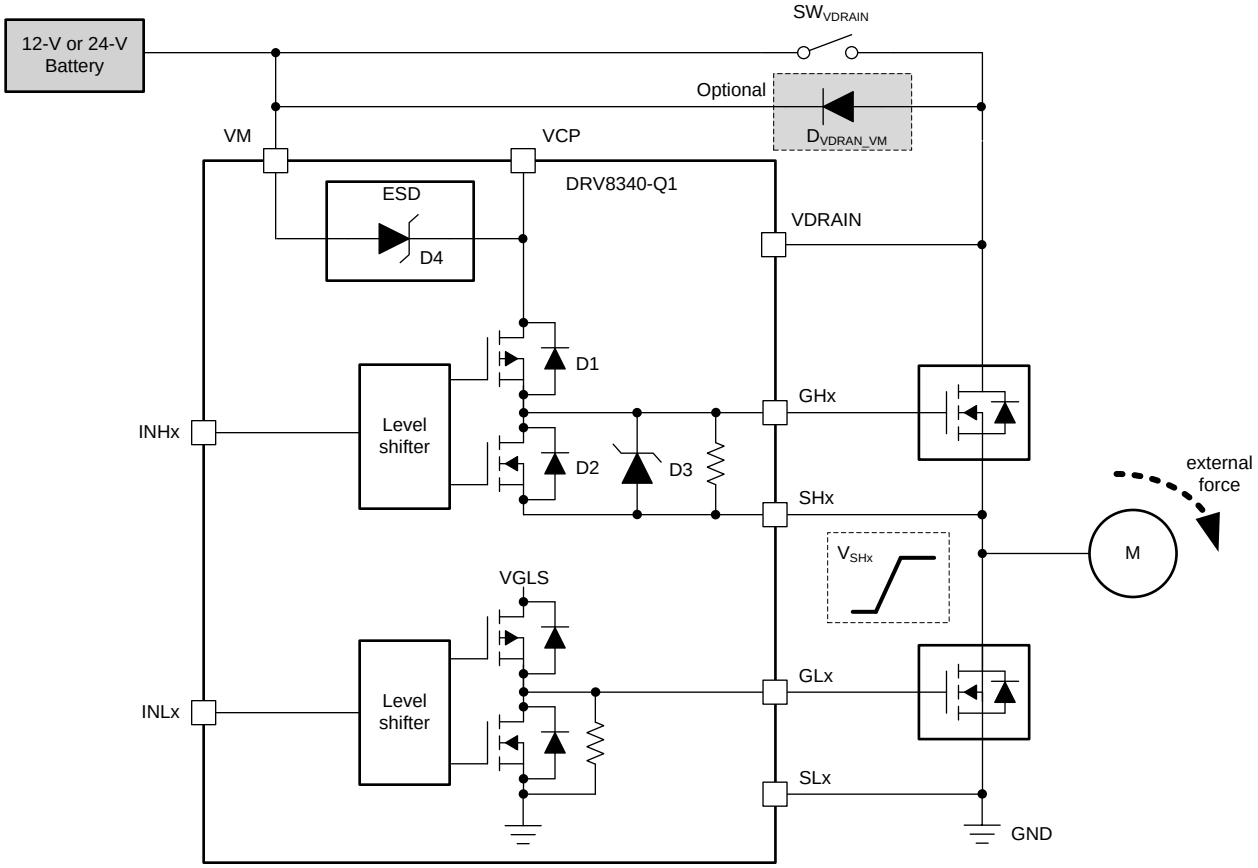

Figure 56. Power Supply Consideration in Generator mode

10.2 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current

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Bulk Capacitance Sizing (continued)

- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage stays stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

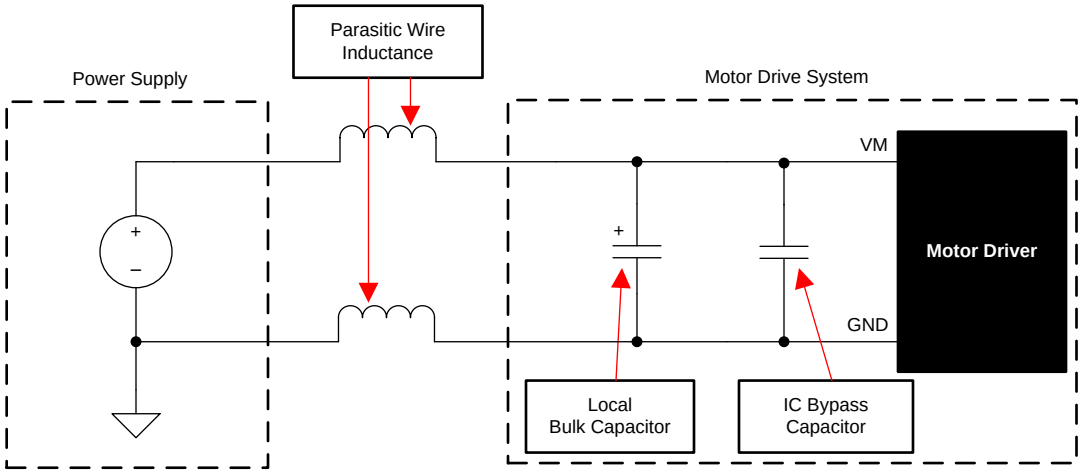

Figure 57. Motor Drive Supply Parasitics Example

11 Layout

11.1 Layout Guidelines

Bypass the VM pin to the PGND pin using a low-ESR ceramic bypass capacitor C_{VM1}. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor C_{FLY} between the CPL and CPH pins. Additionally, place a low-ESR ceramic capacitor C_{VCP} between the VCP and VM pins.

Bypass the DVDD pin to the AGND pin with C_{DVDD}. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

The VDRAIN pin can be shorted directly to the VM pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SLx pins directly to PGND. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations offer more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

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11.2 Layout Example

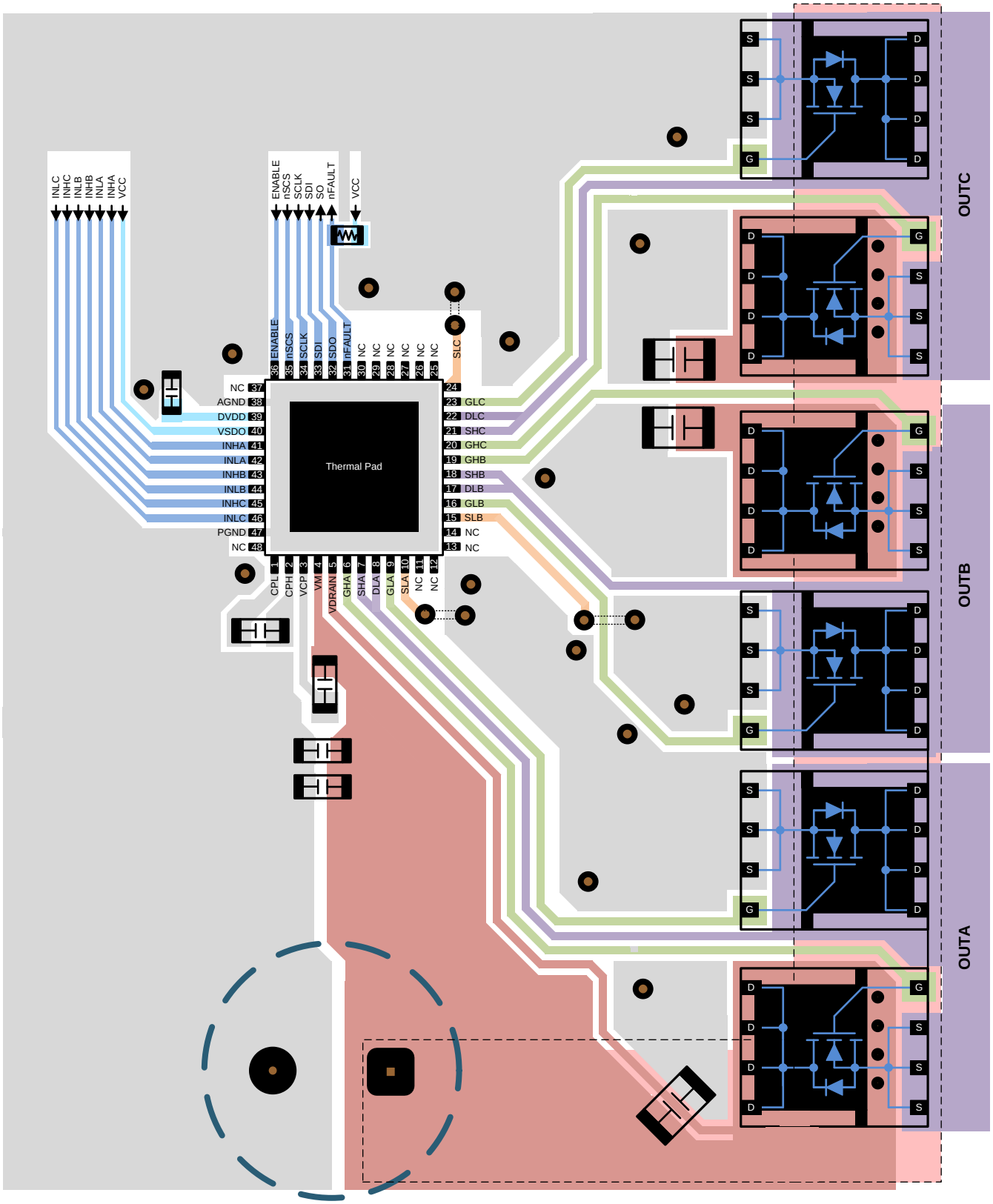


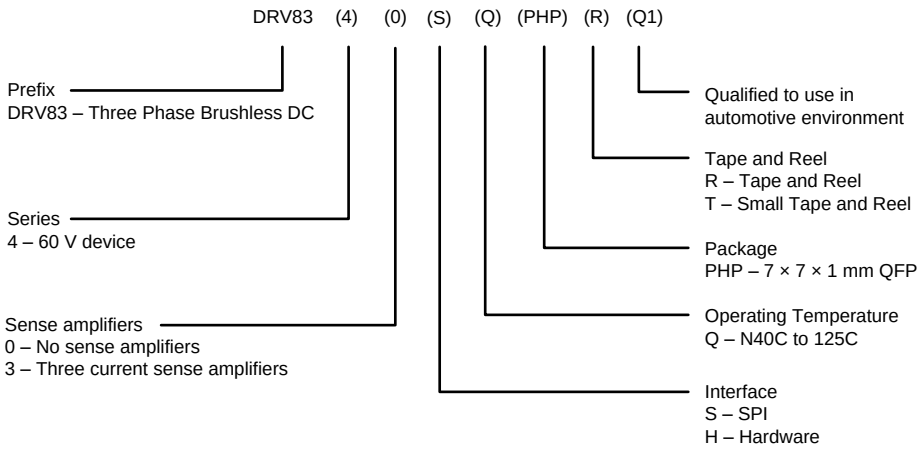
Figure 58. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:



12.2 Documentation Support

12.2.1 Related Documentation

- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Enhanced Fault Diagnostics in DRV834x-Q1* TI TechNote
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle using BLDC Motor*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies*
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™* application report
- Texas Instruments, *Understanding IDRIVE and TDRIVE In TI Motor Gate Drivers* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8340HPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8340H	Samples
DRV8340SPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8340S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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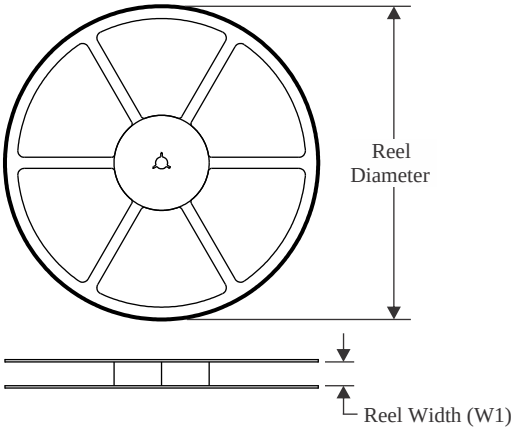
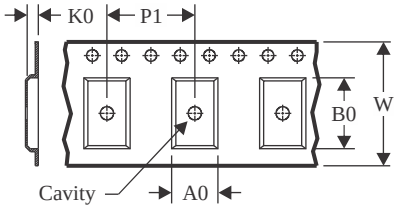
TAPE AND REEL INFORMATION

REEL DIMENSIONS

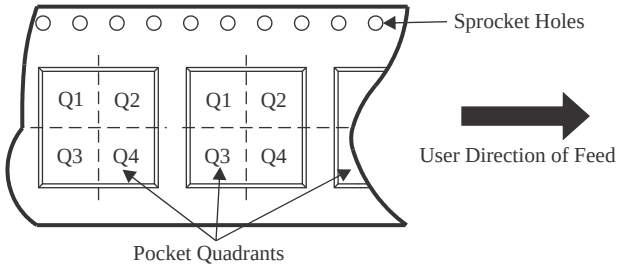


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

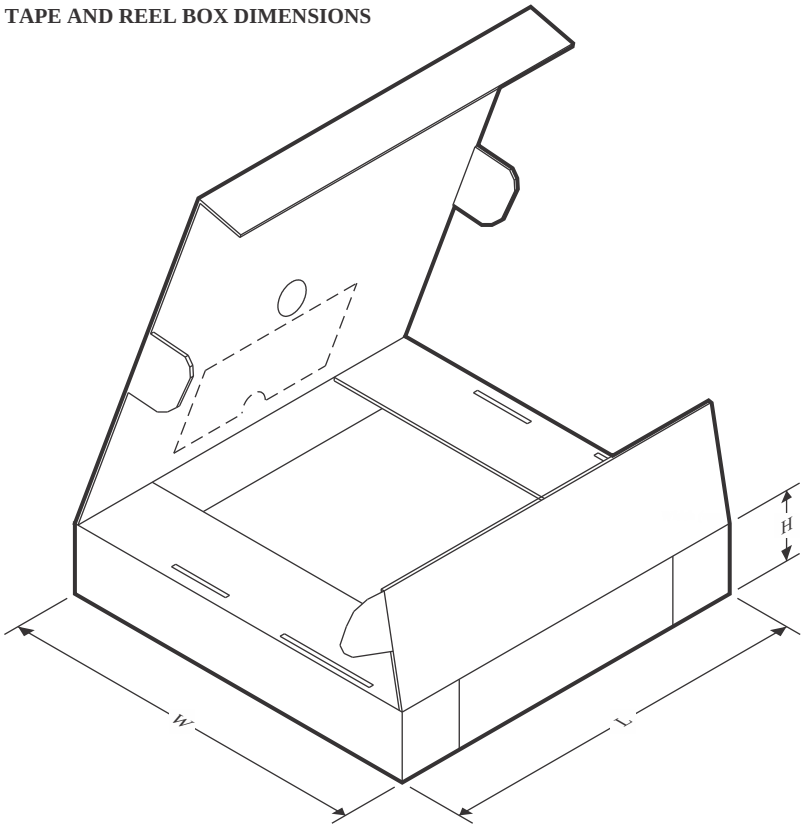
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8340HPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV8340SPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8340HPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0
DRV8340SPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

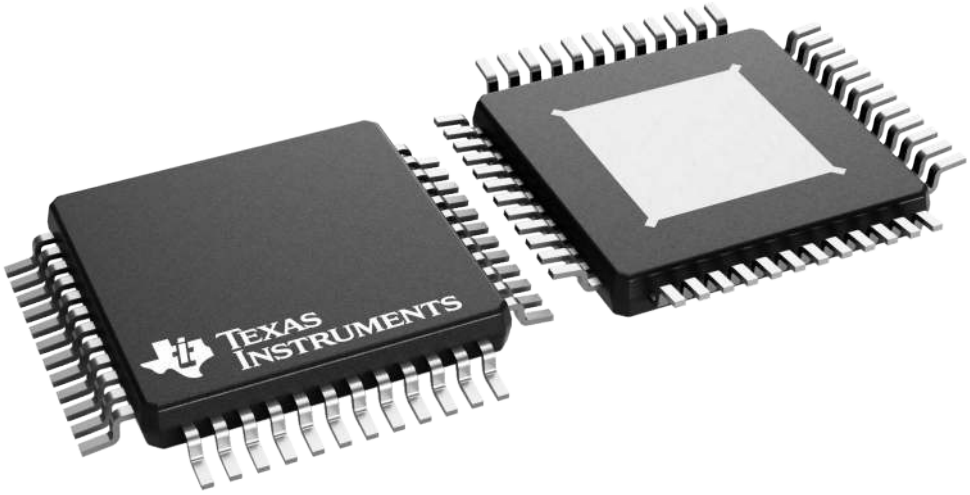
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



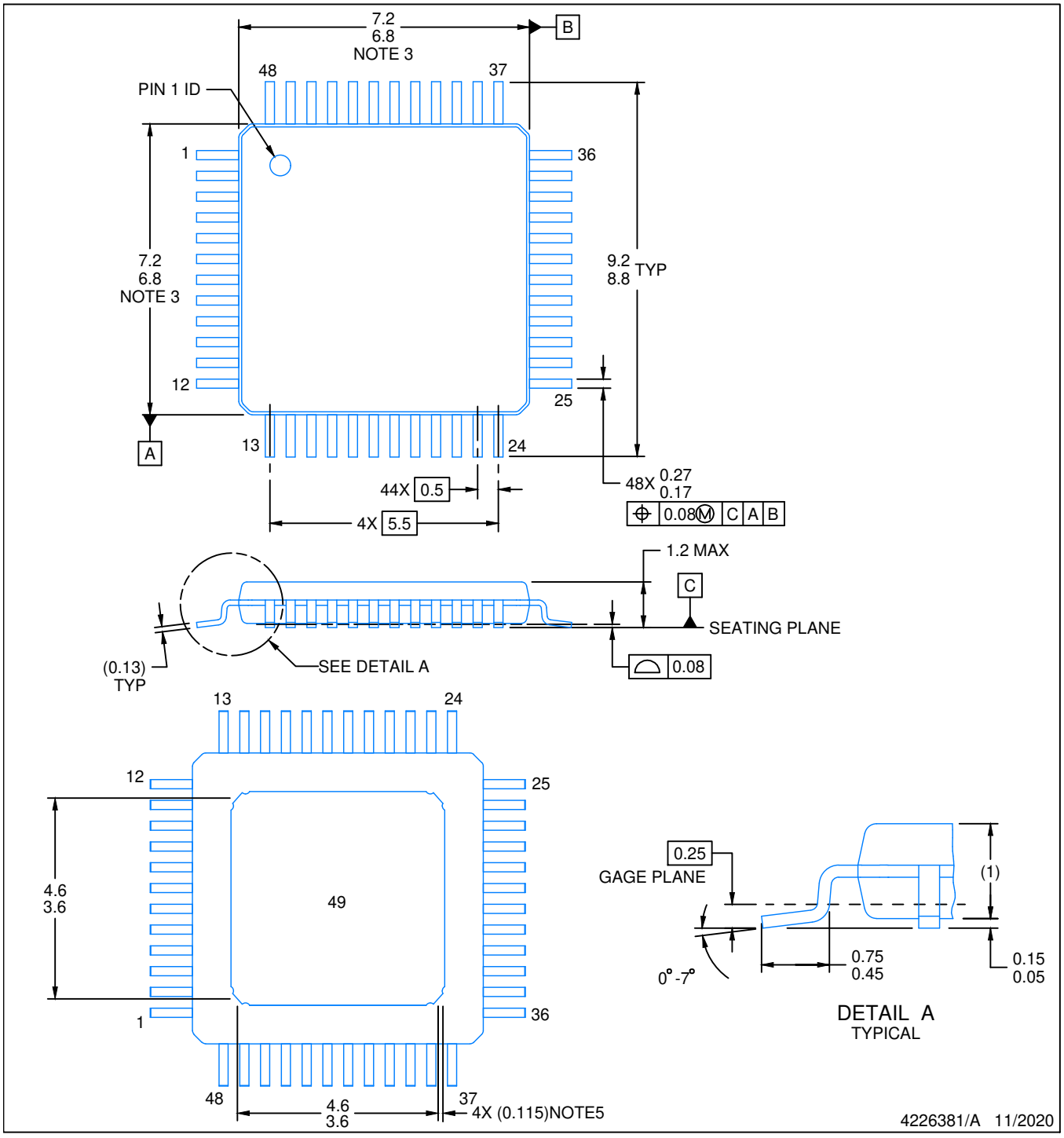
4226443/A

PACKAGE OUTLINE

PHP0048C

PowerPAD™ TQFP - 1.2 mm max height

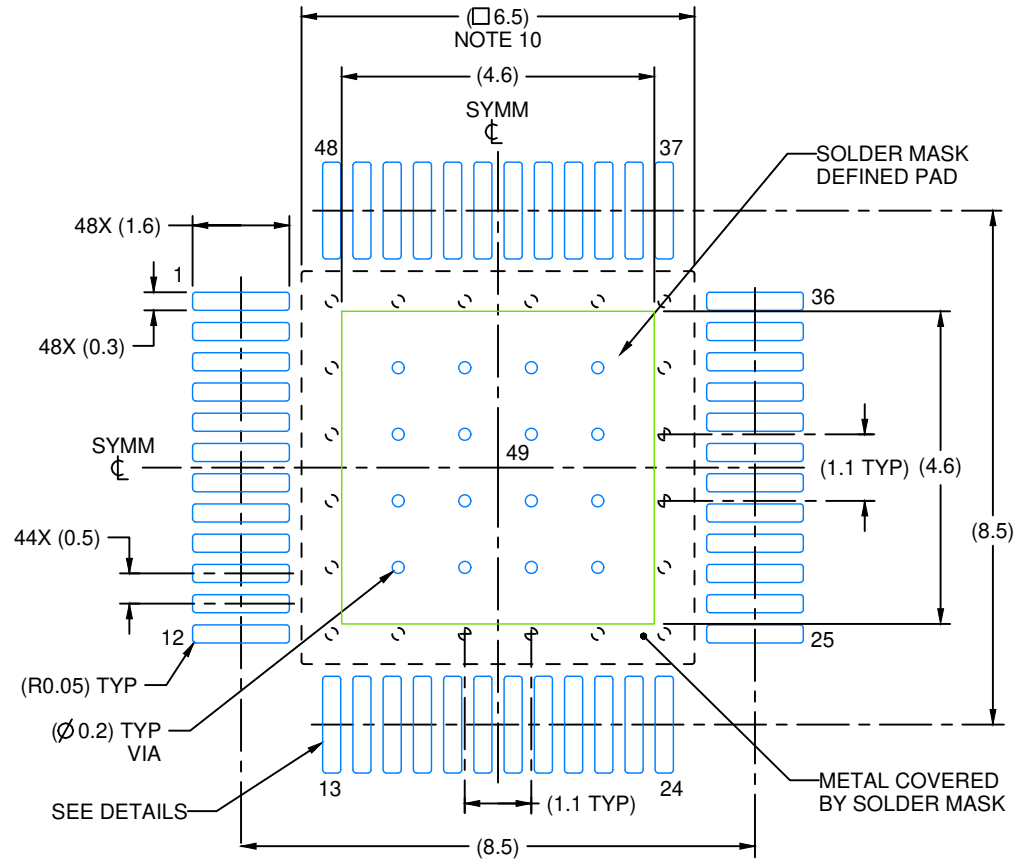
PLASTIC QUAD FLATPACK



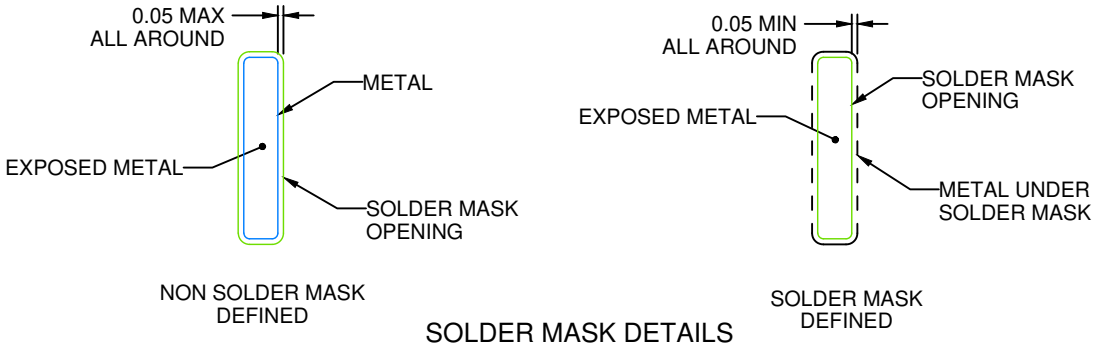
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

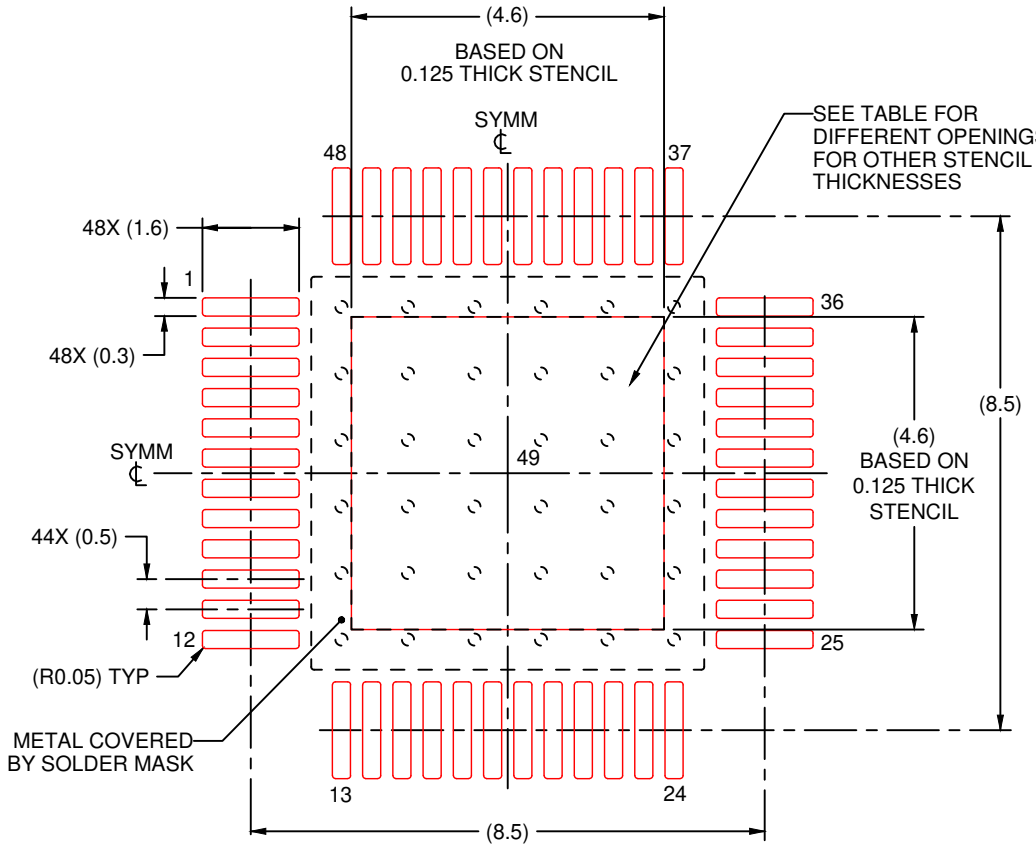


SOLDER MASK DETAILS

4226381/A 11/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.14 X 5.14
0.125	4.6 X 4.6 (SHOWN)
0.150	4.2 X 4.2
0.175	3.89 X 3.89

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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