

## 1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 plastic package intended for use in general purpose bidirectional switching and phase control applications. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- Enhanced current surge capability
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

## 3. Applications

- Air conditioner indoor fan control
- Battery powered applications
- General purpose switching and phase control

## 4. Quick reference data

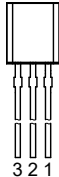
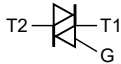
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	1	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	16	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	-	17.5	A
$T_j$	junction temperature		-	-	125	°C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	2	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	2.5	5	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2\text{- G-}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	2.5	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2\text{- G+}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	5	10	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	1.2	10	mA
$V_T$	on-state voltage	$I_T = 5\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	1.4	1.7	V
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$	-	5	-	V/ $\mu$ s

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

## 6. Ordering information

Table 3. Ordering information

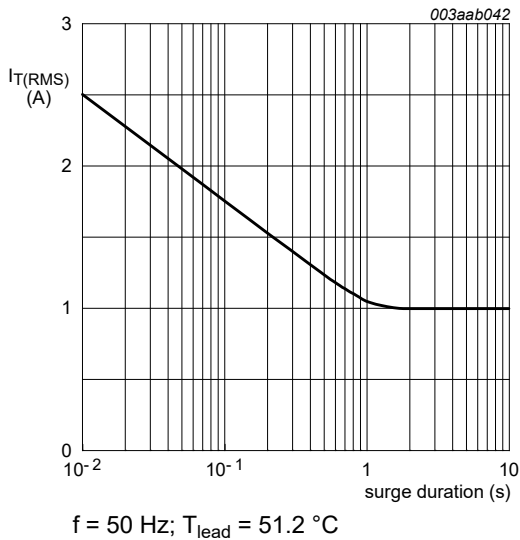
Type number	Package		
	Name	Description	Version
BT132-600D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## 7. Limiting values

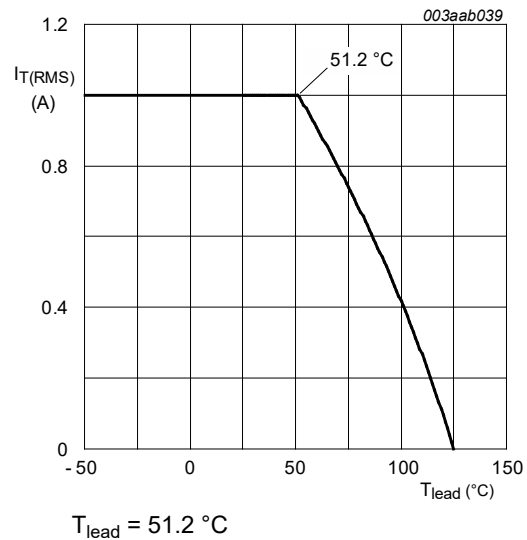
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51.2\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	1	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	16	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	17.5	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	1.28	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_G = 0.2\text{ A}$	-	50	A/ $\mu$ s
			-	50	A/ $\mu$ s
			-	50	A/ $\mu$ s
			-	10	A/ $\mu$ s
$I_{GM}$	peak gate current		-	2	A
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		-	125	°C



**Fig. 1. RMS on-state current as a function of surge duration; maximum values**



**Fig. 2. RMS on-state current as a function of lead temperature; maximum values**

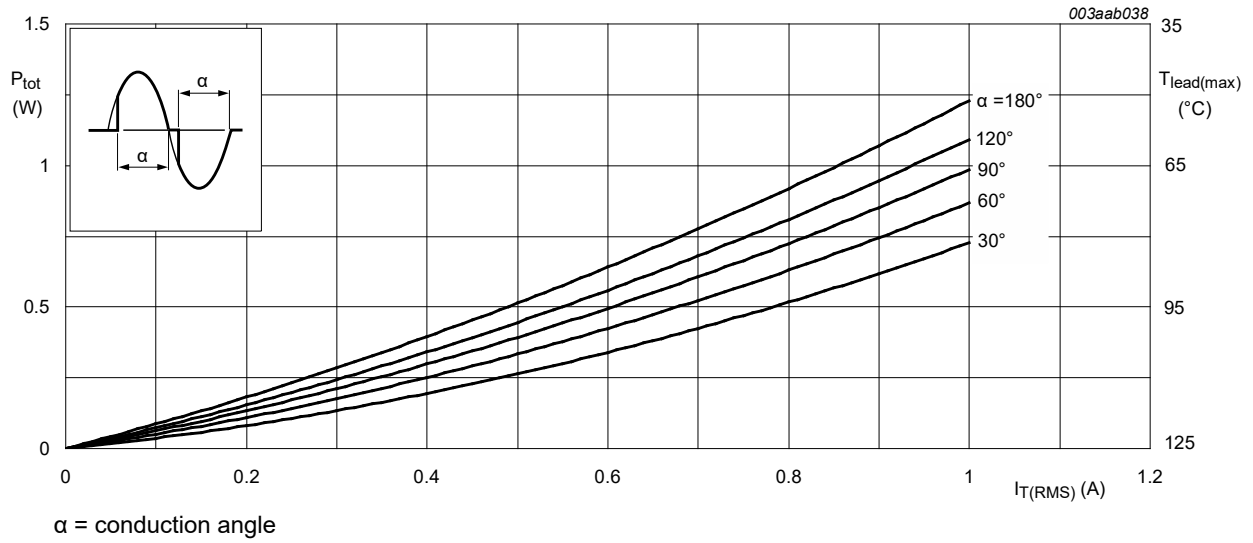


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

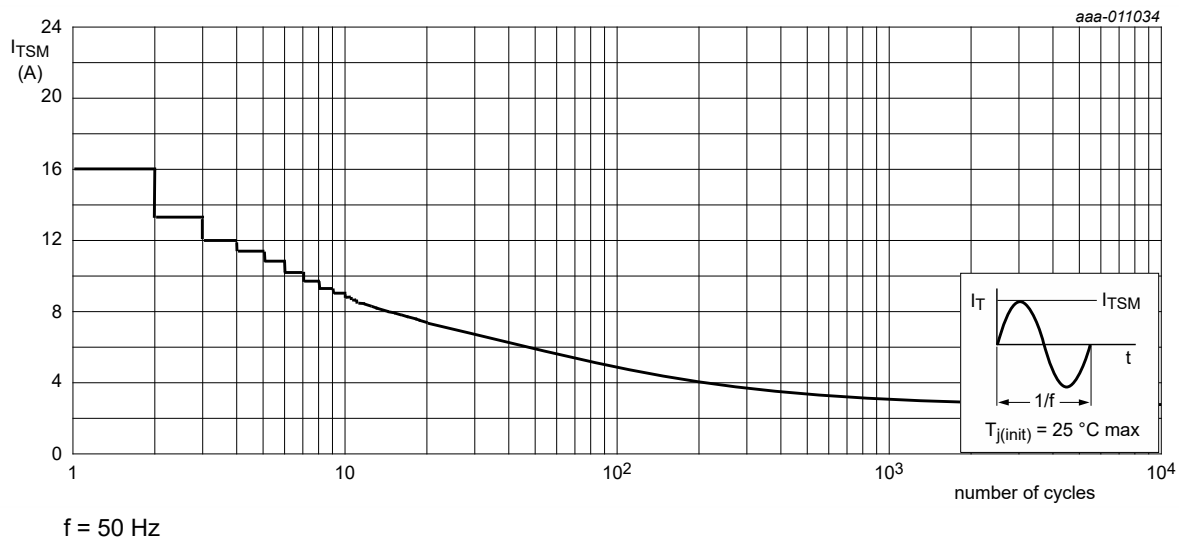
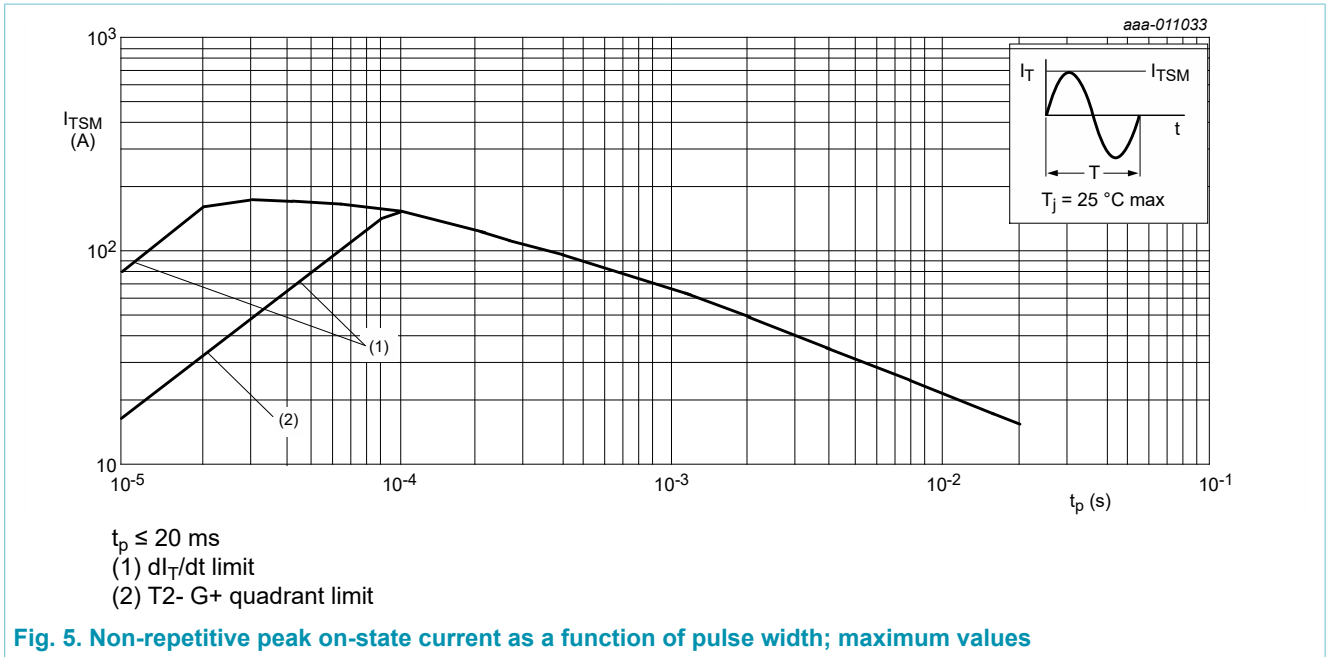


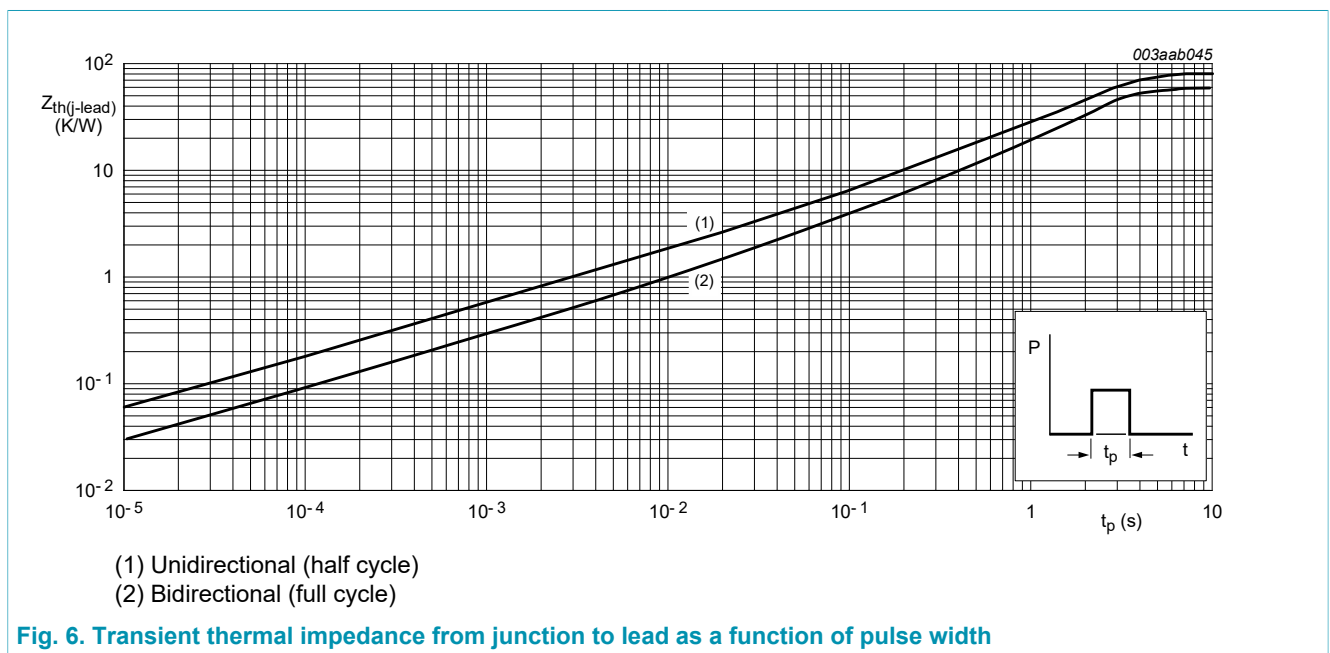
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



### 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>th(j-lead)</sub>	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
		half cycle; Fig. 6	-	-	80	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	printed circuit mounted: lead length = 4 mm	-	150	-	K/W



## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	2	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	2.5	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	2.5	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G+;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	5	10	mA
$I_L$	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	1.6	10	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	4.5	15	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	1.2	10	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2- G+;$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	2.2	15	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	1.2	10	mA
$V_T$	on-state voltage	$I_T = 5\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	1.4	1.7	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	0.7	1	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$	-	5	-	V/ $\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 6\text{ A}; V_D = 600\text{ V}; I_G = 0.1\text{ A}; dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$

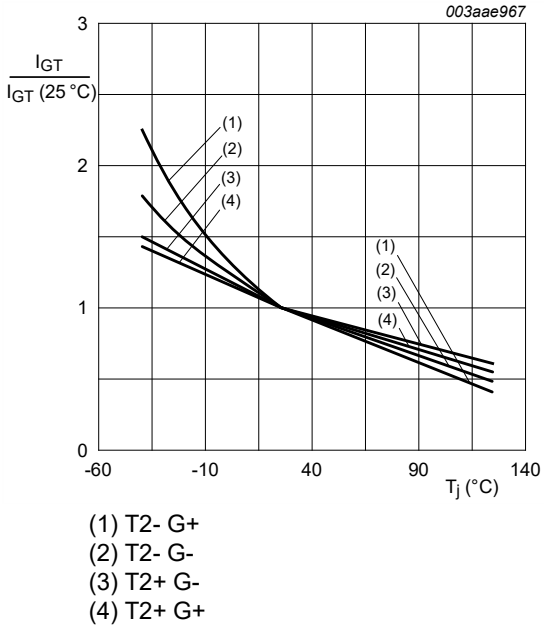


Fig. 7. Normalized gate trigger current as a function of junction temperature

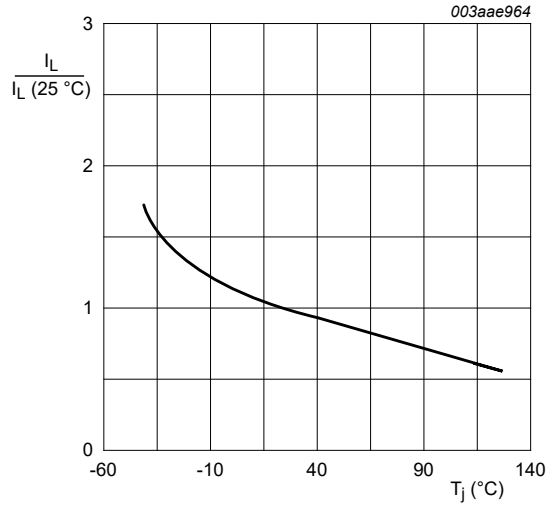


Fig. 8. Normalized latching current as a function of junction temperature

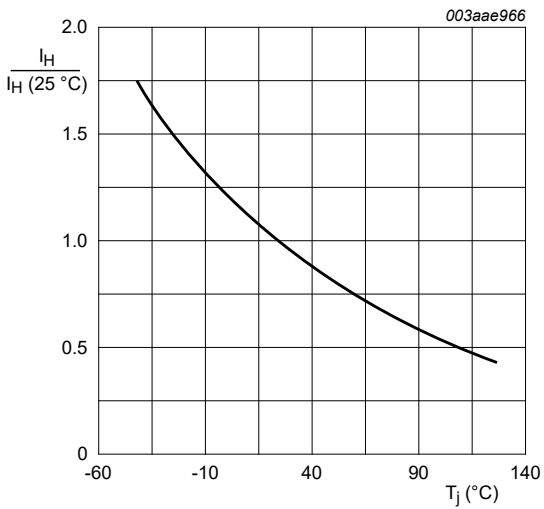


Fig. 9. Normalized holding current as a function of junction temperature

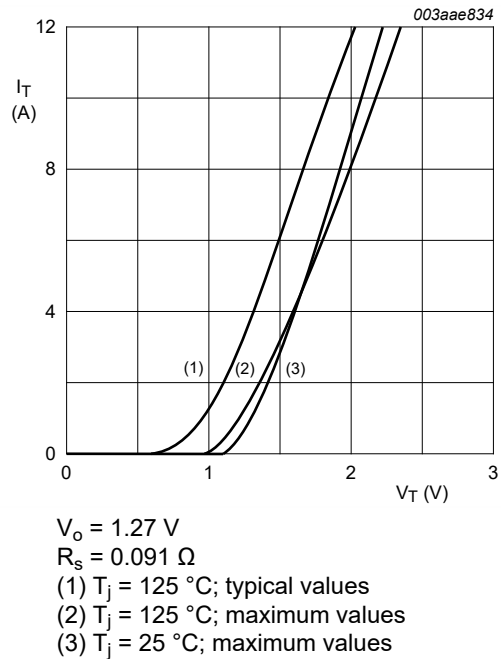


Fig. 10. On-state current as a function of on-state voltage



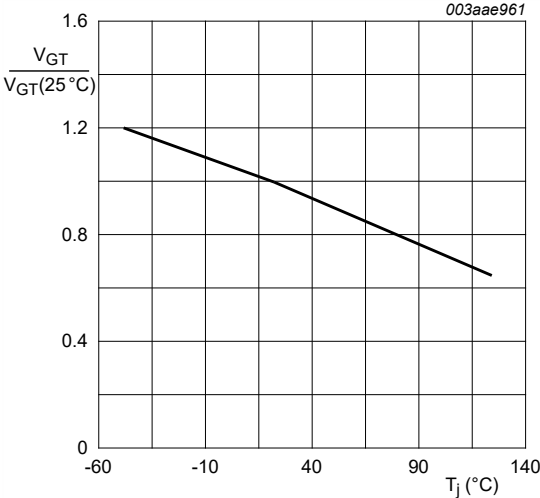
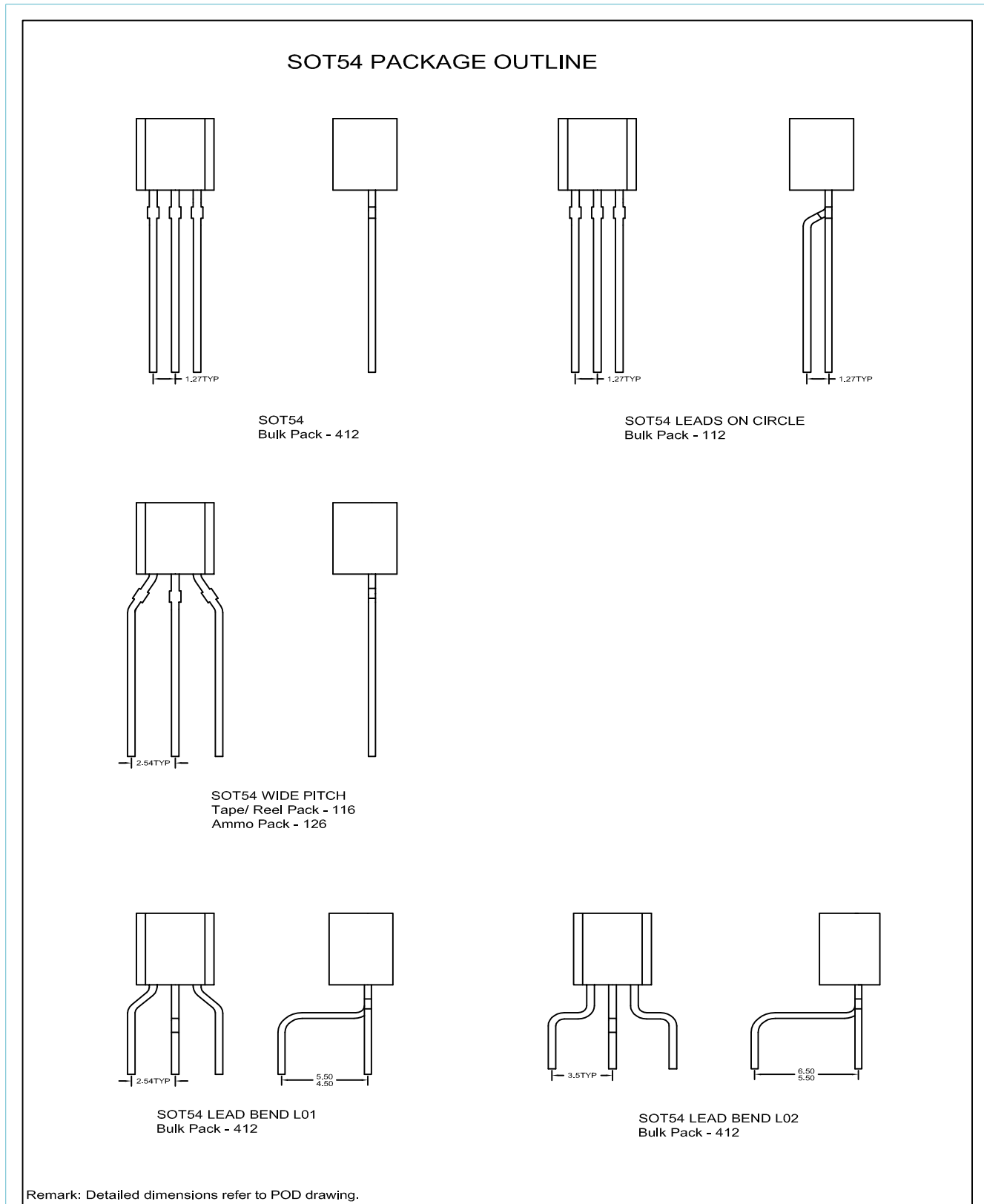


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

### 10. Package outline



**Fig. 12. Package outline TO-92 (SOT54)**

# 11. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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