

## N-channel 900 V, 0.91 $\Omega$ typ., 6 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

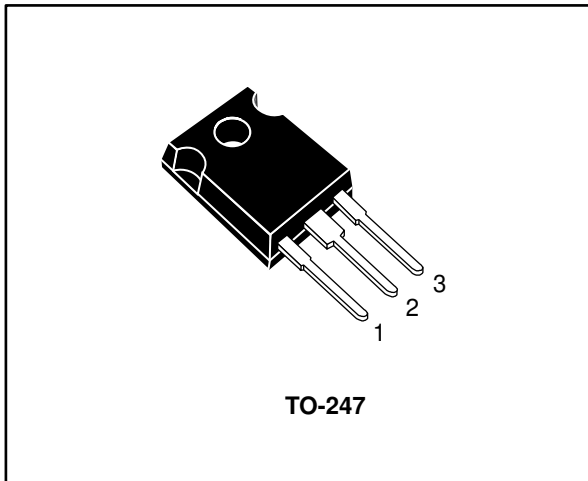
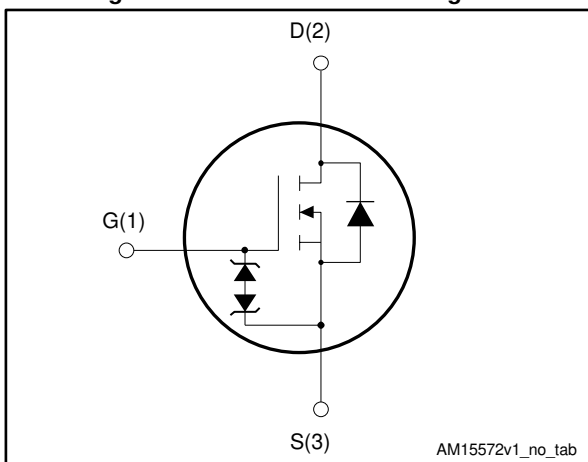


Figure 1: Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STW6N90K5  | 900 V           | 1.10 $\Omega$            | 6 A            |

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|---------|---------|
| STW6N90K5  | 6N90K5  | TO-247  | Tube    |

**Contents**

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol        | Parameter   | Value       | Unit             |
|---------------|---|-------------|------------------|
| $V_{GS}$      | Gate-source voltage   | $\pm 30$    | V                |
| $I_D$         | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 6           | A                |
| $I_D$         | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 4           | A                |
| $I_D^{(1)}$   | Drain current (pulsed)  | 24          | A                |
| $P_{TOT}$     | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$           | 110         | W                |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope                               | 4.5         | V/ns             |
| $dv/dt^{(3)}$ | MOSFET $dv/dt$ ruggedness                                       | 50          |                  |
| $T_j$         | Operating junction temperature range                            | - 55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$     | Storage temperature range                                       |             |                  |

**Notes:**

(1) Pulse width limited by safe operating area

(2)  $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 450\text{ V}$ .

(3)  $V_{DS} \leq 720\text{ V}$

**Table 3: Thermal data**

| Symbol         | Parameter                           | Value | Unit                      |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 1.14  | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 62.5  | $^\circ\text{C}/\text{W}$ |

**Table 4: Avalanche characteristics**

| Symbol   | Parameter  | Value | Unit |
|----------|--|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )                                 | 2     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 210   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 5: On/off-state**

| Symbol        | Parameter                         | Test conditions  | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                    | 900  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$                                |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$<br>$T_C = 125\text{ °C}^{(1)}$ |      |      | 50       | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$                             |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DD} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                             | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$                                    |      | 0.91 | 1.10     | $\Omega$      |

**Notes:**

<sup>(1)</sup> Defined by design, not subject to production test.

**Table 6: Dynamic**

| Symbol            | Parameter                             | Test conditions   | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|---|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0\text{ V}$   | -    | 342  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |   | -    | 31   | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |   | -    | 1.2  | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related   | $V_{DS} = 0\text{ to }720\text{ V}$ ,<br>$V_{GS} = 0\text{ V}$  | -    | 55   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related |   | -    | 20   | -    | pF       |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$   | -    | 6.4  | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 720\text{ V}$ , $I_D = 6\text{ A}$<br>$V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 11   | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |   | -    | 2.5  | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                     |   | -    | 7    | -    | nC       |

**Notes:**

<sup>(1)</sup>  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

<sup>(2)</sup>  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

Table 7: Switching times

| Symbol       | Parameter           | Test conditions  | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 450\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\ \Omega$<br>$V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 12.4 | -    | ns   |
| $t_r$        | Rise time           |  | -    | 12.2 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |  | -    | 30.4 | -    | ns   |
| $t_f$        | Fall time           |  | -    | 15.5 | -    | ns   |

Table 8: Source-drain diode

| Symbol          | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |  | -    |      | 6    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -    |      | 24   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 6\text{ A}$ , $V_{GS} = 0\text{ V}$  | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                     | -    | 342  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 3.13 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 18.3 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 536  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 4.42 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 16.5 |      | A             |

**Notes:**

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

| Symbol        | Parameter                     | Test conditions                                 | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$ | 30   | -    | -    | V    |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

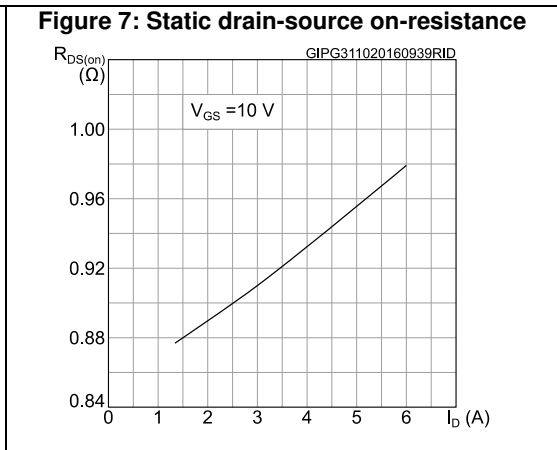
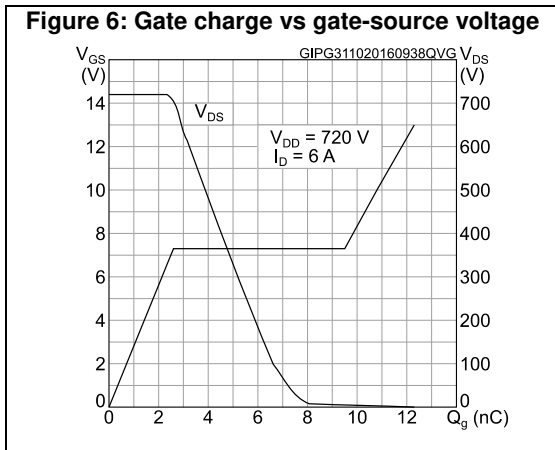
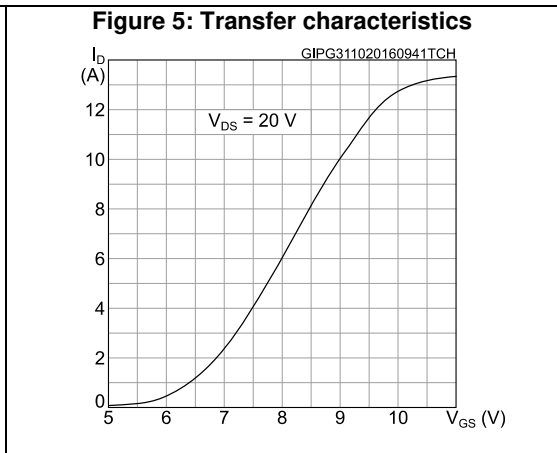
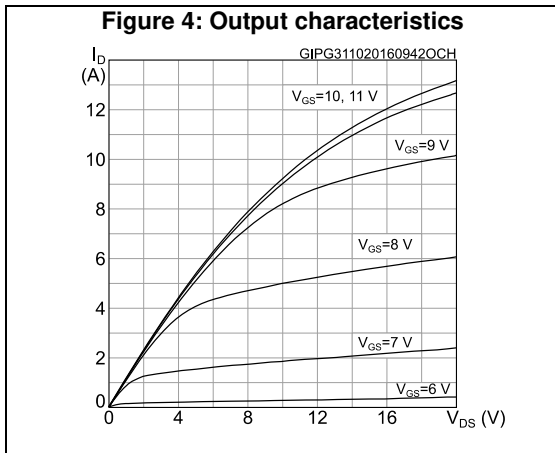
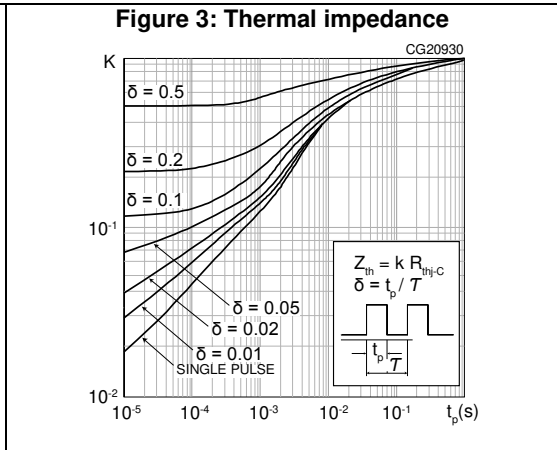
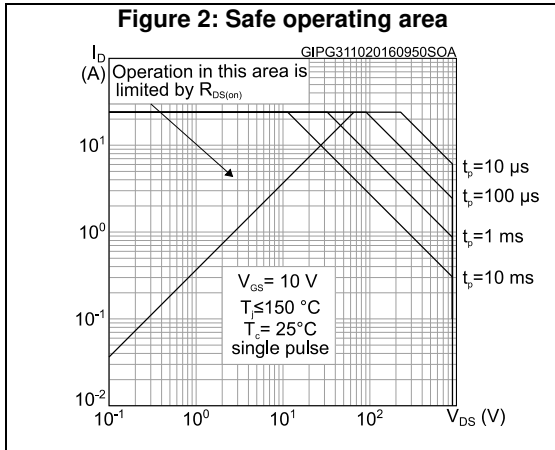


Figure 8: Capacitance variations

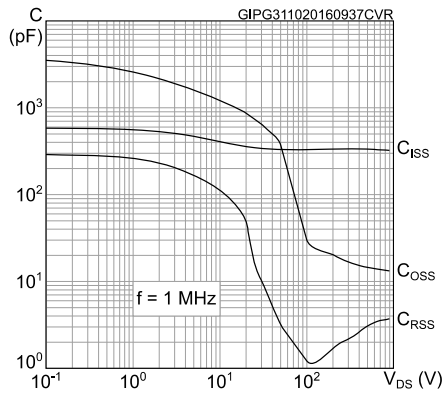


Figure 9: Normalized gate threshold voltage vs temperature

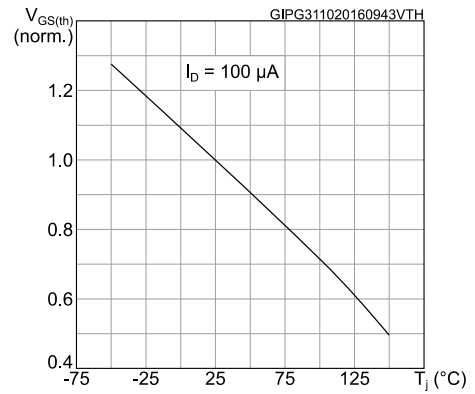


Figure 10: Normalized on-resistance vs temperature

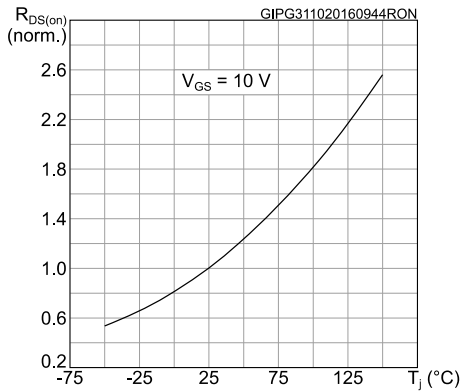


Figure 11: Normalized V<sub>(BR)DSS</sub> vs temperature

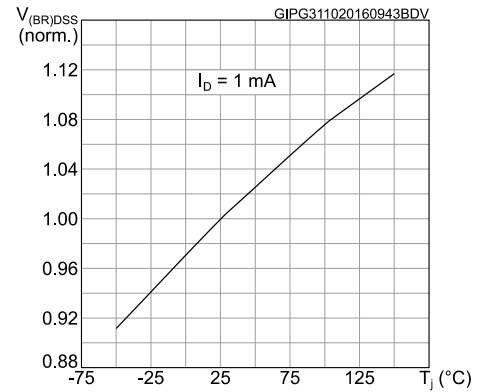


Figure 12: Maximum avalanche energy vs starting T<sub>J</sub>

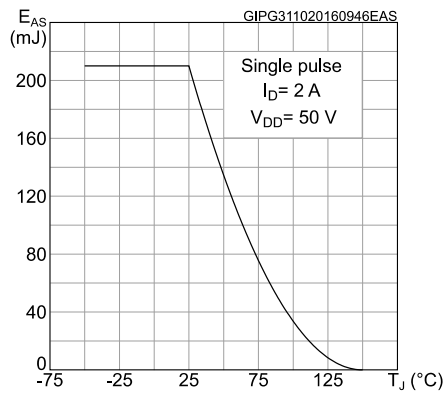
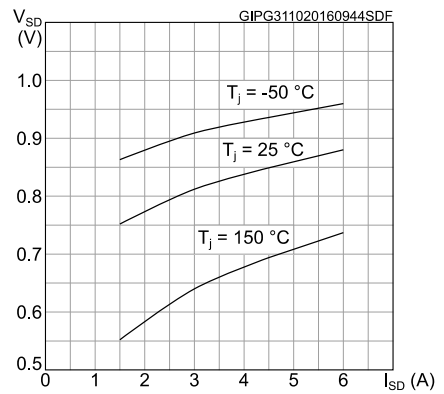
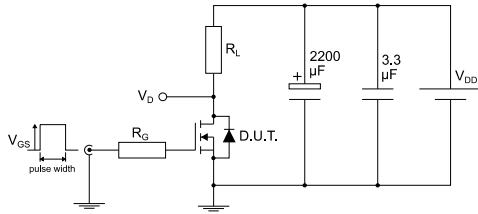


Figure 13: Source-drain diode forward characteristics



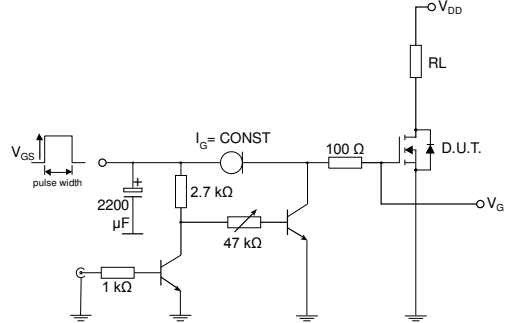
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



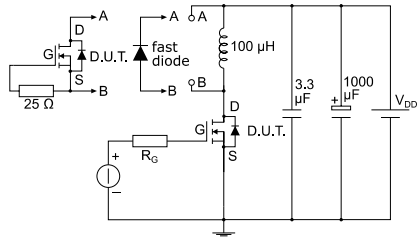
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



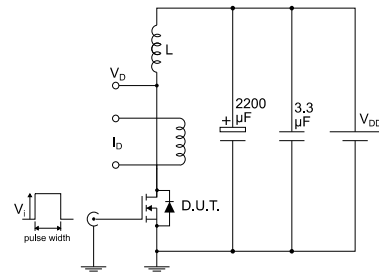
AM01469v10

**Figure 16: Test circuit for inductive load switching and diode recovery times**



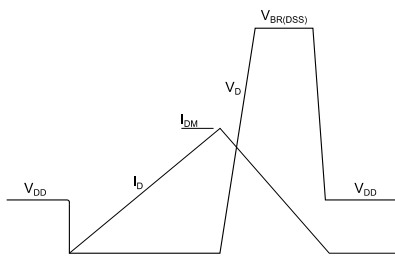
AM01470v1

**Figure 17: Unclamped inductive load test circuit**



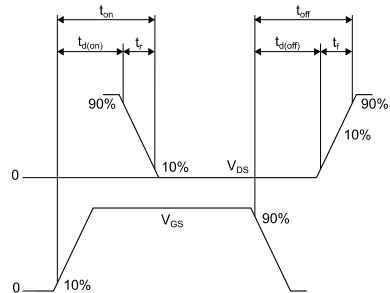
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

Figure 20: TO-247 package outline

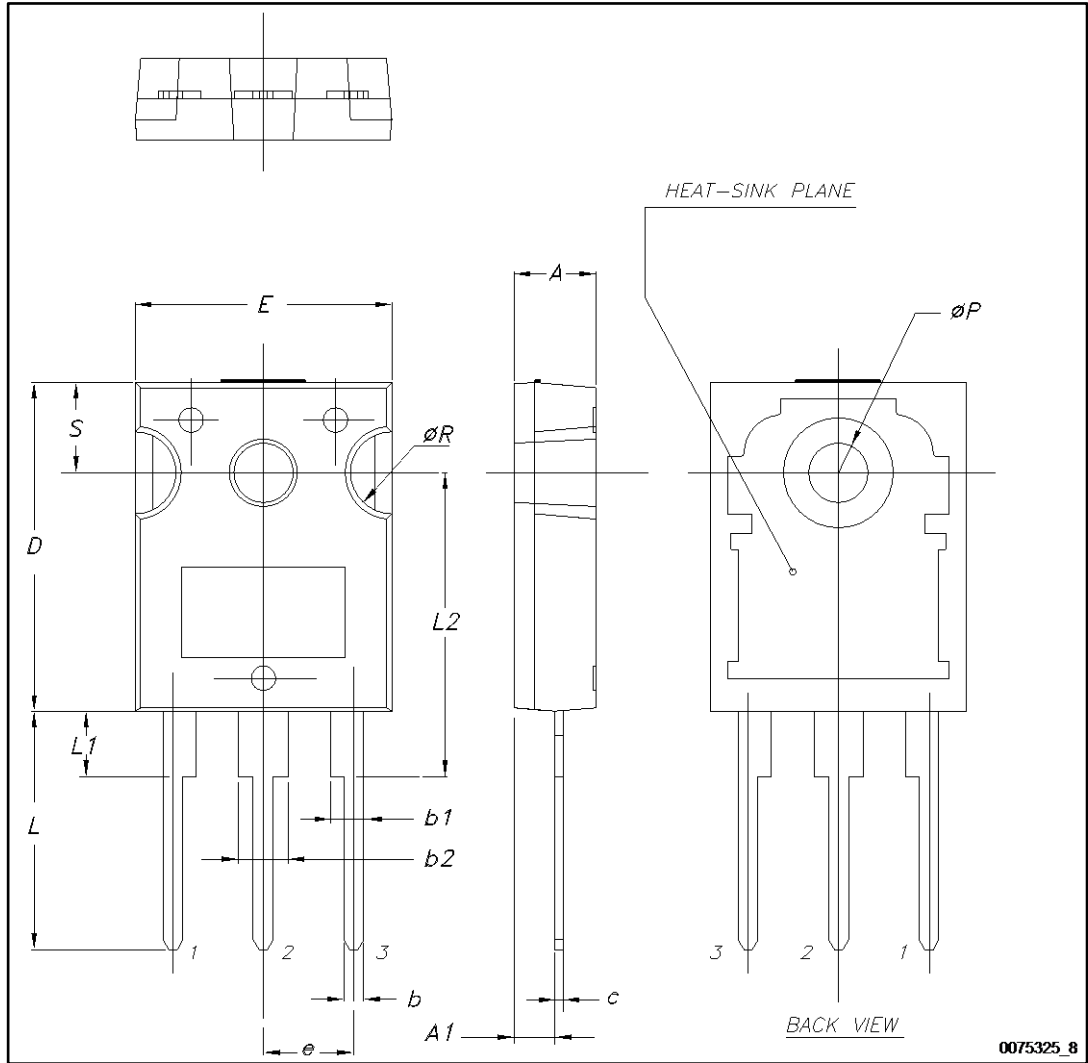


Table 10: TO-247 package mechanical data

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## 5 Revision history

Table 11: Document revision history

| Date        | Revision | Changes        |
|-------------|----------|----------------|
| 02-Nov-2016 | 1        | First release. |

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