CDCVF25081 3.3-V Phased-Lock Loop Clock Driver

1 Features

- Phase-locked loop based, zero-delay buffer
  - 1 clock input to 2 banks of 4 outputs
  - No external RC network required
- Supply voltage: 3 V to 3.6 V
- Operating frequency: 8 MHz to 200 MHz
- Low additive jitter (cycle-cycle): ±100 ps for 66 MHz to 200 MHz
- Power-down mode available
  - Current consumption: < 20 µA in Power-down mode
- 25-Ω on-chip series damping resistors
- Industrial temperature range: –40°C to 85°C
- Spread Spectrum Clock Compatible (SSC)
- Packaged in
  - 9.9-mm × 3.91-mm, 16-pin SOIC (D)
  - 5.0-mm × 4.4-mm, 16-pin TSSOP (PW)

2 Applications

- Defense radio
- Production switchers and mixers
- Radar
- In-vitro diagnostics
- CT & PET scanner

3 Description

The CDCVF25081 is a high performance, low skew, low jitter, phased-locked loop clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal. The outputs are divided into 2 banks for a total of 8 buffered CLKIN outputs. The device automatically puts the outputs to a low state when no CLKIN signal is present (power down mode).

The S1 and S2 pins allow selection between PLL or bypassed PLL outputs. When left open, the outputs are disabled to a logic low state.

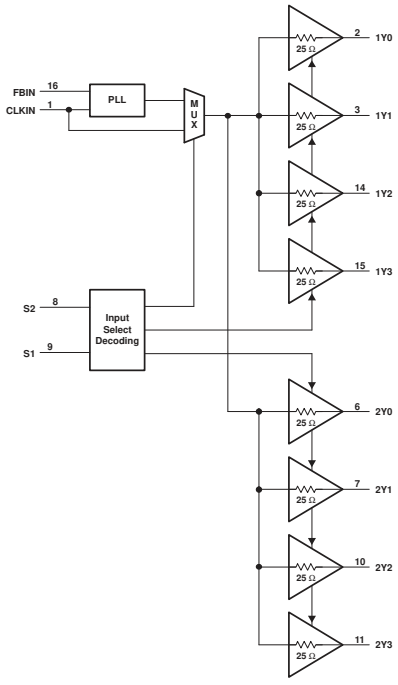
The part supports a fail-safe function. The device further incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

The device operates in 3.3V supply environment and is characterized from –40°C to 85°C (ambient temperature).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCVF25081	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2003) to Revision B (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

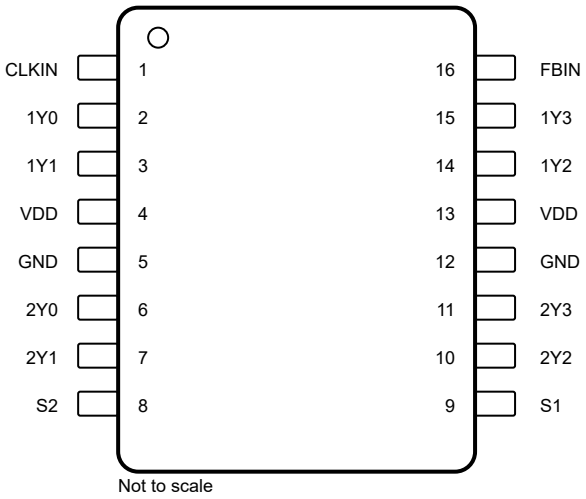


Figure 5-1. D or PW Package 16-Pin SOIC or TSSOP Top View

Table 5-1. Pin Functions

PIN		I/O TYPE(1)	DESCRIPTION
NAME	NO.		
INPUT CLOCK			
CLKIN	1	I	Clock input. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN.
INPUT SELECT			
S1, S2	9, 8	I	Input Selection. Selects input port. (See Table 8-2.)
FEEDBACK			
FBIN	16	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock.
OUTPUT CLOCKS			
1Y0	2	O	Bank 1 Y0 clock output with an integrated 25-Ω series-damping resistor.
1Y1	3	O	Bank 1 Y1 clock output with an integrated 25-Ω series-damping resistor.
1Y2	14	O	Bank 1 Y2 clock output with an integrated 25-Ω series-damping resistor.
1Y3	15	O	Bank 1 Y3 clock output with an integrated 25-Ω series-damping resistor.
2Y0	6	O	Bank 2 Y0 clock output with an integrated 25-Ω series-damping resistor.
2Y1	7	O	Bank 2 Y1 clock output with an integrated 25-Ω series-damping resistor.
2Y2	10	O	Bank 2 Y2 clock output with an integrated 25-Ω series-damping resistor.
2Y3	11	O	Bank 2 Y3 clock output with an integrated 25-Ω series-damping resistor.
SUPPLY VOLTAGE AND GROUND			
VDD	4, 13	P	3.3V power supply for output channels and core voltage.
GND	5, 12	G	Ground. Connect ground pad to system ground.

(1) The definitions below define the I/O type for each pin.

- I = Input
- O = Output
- P = Power Supply
- G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Power supply voltage		−0.5	4.6	V
V_I	Input voltage range(2) (3)		−0.5	4.6	V
V_O	Output voltage range(2) (3)		−0.5	$V_{DD,}$ + 0.5	V
I_{IK}	Input clamp current (V_I < 0)		-50		mA
I_{OK}	Output clamp current (V_O < 0)		-50		mA
I_O	Continuous total output current (V_O = 0 to V_{DD})		-50		mA
θ_{JA}	Package thermal impedance(4)	PW package		147	°C/W
		D package		112	°C/W
T_{stg}	Storage temperature		−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Low level input voltage, V_{IL}			0.8	V
High level input voltage, V_{IH}	2			V
Input voltage, V_I	0		3.6	V
High-level output current, I_{OH}			-12	mA
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		CDCVF25081		UNIT
		SOIC (D)	TSSOP (PW)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.5	109.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.0	40.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.2	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.7	3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.8	55.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V, I_I = –18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}			±5	µA
I_{PD} [2]	Power down current	f_{CLKIN} = 0 MHz, V_{DD}= 3.3 V			20	µA
I_{OZ}	Output 3-state	V_o = 0 V or V_{DD}, V_{DD} = 3.6 V			±5	µA
C_I	Input capacitance at FBIN, CLKIN	V_I = 0 V or V_{DD}		4		pF
C_I	Input capacitance at S1, S2	V_I = 0 V or V_{DD}		2.2		pF
C_O	Output capacitance	V_I= 0 V or V_{DD}		3		pF
V_{OH}	High-level output voltage	V_{DD} = min to max, I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V, I_{OH} = –12 mA	2.1			
		V_{DD} = 3 V, I_{OH} = –6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max, I_{OL} = 100 µA			0.2	V
		V_{DD} = 3 V, I_{OL} = 12 mA			0.8	
		V_{DD} = 3 V, I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V, V_O = 1 V	–24			mA
		V_{DD} = 3.3 V, V_O = 1.65 V		–30		
		V_{DD} = 3.6 V, V_O = 3.135 V			–15	
I_{OL}	Low-level output current	V_{DD} = 3 V, V_O = 1.95 V	26			mA
		V_{DD} = 3.3 V, V_O = 1.65 V		33		
		V_{DD} = 3.6 V, V_O = 0.4 V			14	

(1) All typical values are at respective nominal V_{DD}.
(2) For I_{DD} over frequency see Figure 9-2.

6.6 Timing Requirements

over recommended ranges of supply voltage, load, and operating free-air temperature

		MIN	NOM	MAX	UNIT
Clock frequency, f_{clk}	C_L = 25 pF	8		100	MHz
	C_L = 15 pF	66		200	

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(lock)}$	PLL lock time	f = 100 MHz		10		µs
$t_{(phoffset)}$	Phase offset (CLKIN to FBIN)	f = 8 MHz to 66 MHz, Vth = V_{DD}/2 (3)	–200		200	ps
		f = 66 MHz to 200 MHz, Vth = V_{DD}/2 (3)	–150		150	
t_{PLH}	Low-to-high level output propagation delay	S2 = High, S1 = Low (PLL bypass), f = 1 MHz, C_L = 25 pF	2.5		6	ns
t_{PHL}	High-to-low level output propagation delay		2.5		6	
$t_{sk(o)}$	Output skew (Yn to Yn) (2)				150	ps
$t_{sk(pp)}$	Part-to-part skew	S2 = high, S1 = high (PLL mode)			600	ps
		S2 = high, S1 = low (PLL bypass)			700	
$t_{jit(cc)}$	Jitter (cycle-to-cycle)	f = 66 MHz to 200 MHz, C_L = 15 pF			±100	ps
		f = 66 MHz to 100 MHz, C_L = 25 pF, f = 8 MHz to 66 MHz (see Figure 6-2)			±150	
odc	Output duty cycle	f = 8 MHz to 200 MHz	43%		57%	
$t_{sk(p)}$	Pulse skew	S2 = High, S1 = low (PLL bypass), f = 1 MHz, C_L = 25 pF			0.7	ns
t_{RISE}	Rise time rate	C_L = 15 pF, See Figure 7-4	0.8		3.3	V/ns
		C_L = 25 pF, See Figure 7-4	0.5		2	
t_{FALL}	Fall time rate	C_L = 15 pF, See Figure 7-4	0.8		3.3	V/ns
		C_L = 25 pF, See Figure 7-4	0.5		2	

(1) All typical values are at respective nominal V_{DD}.
(2) The $t_{sk(o)}$specification is only valid for equal loading of all outputs.
(3) Similar waveform at CLKIN and FBIN are required. For phase displacement between CLKIN and Y-outputs see Figure 6-1.

6.8 Typical Characteristics

Figure 6-1 captures the variation of the CDCVF25081 current consumption with capacitive load and phase displacement. Figure 6-2 shows the variation of the cycle-to-cycle jitter across frequency.

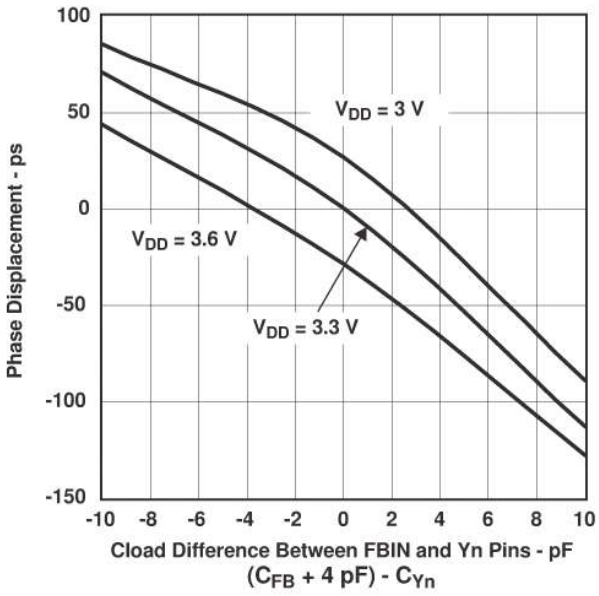


Figure 6-1. Phase Displacement vs. Load

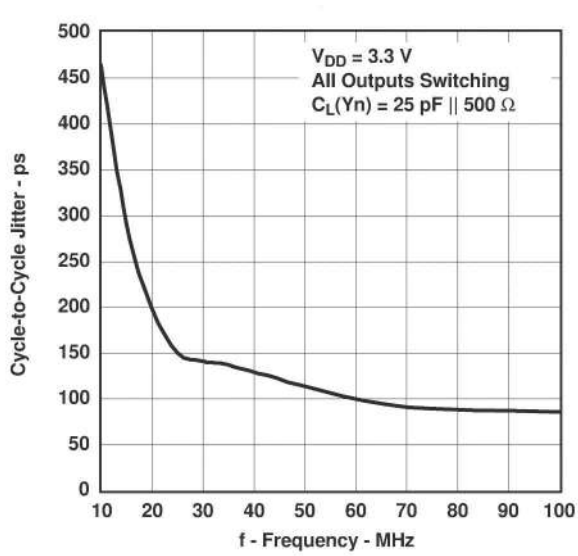
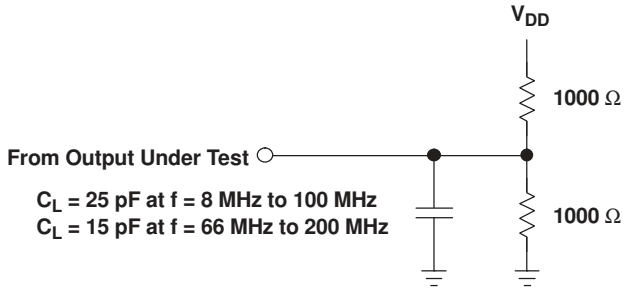


Figure 6-2. Cycle-to-Cycle Jitter vs. Frequency

7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 7-1. Test Load Circuit

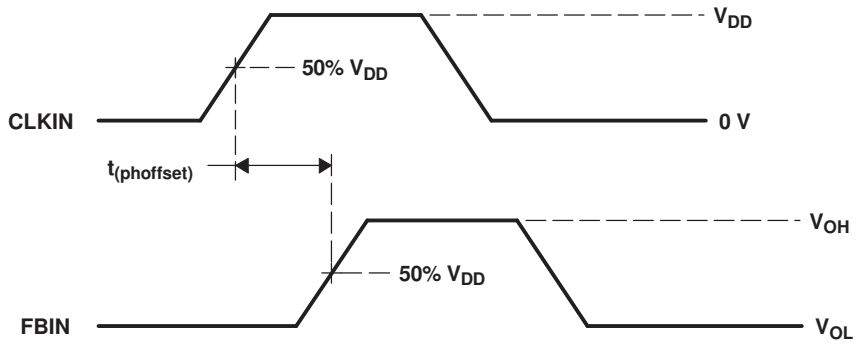
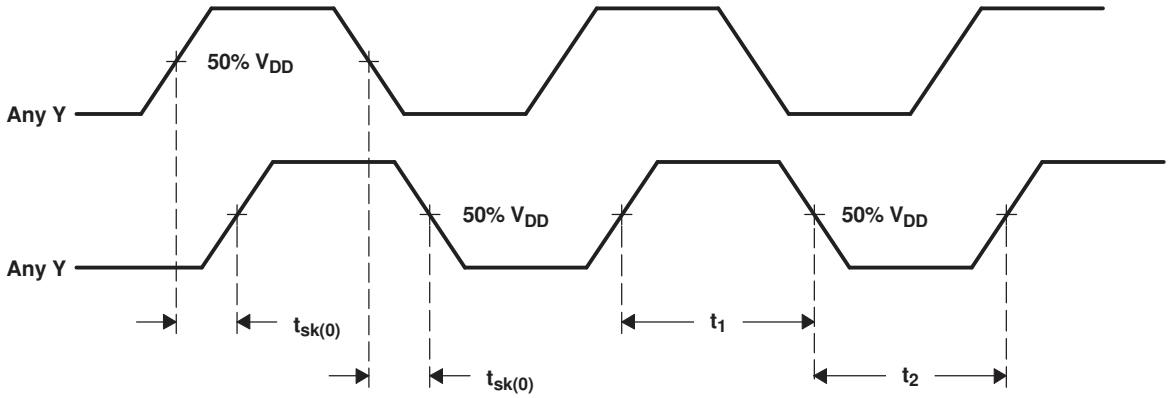
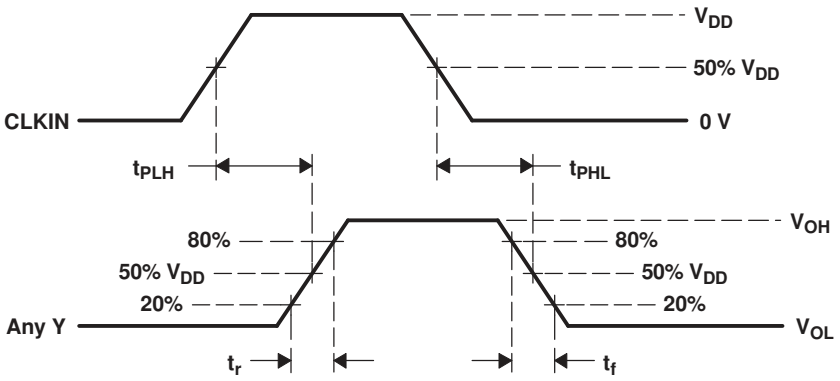


Figure 7-2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)



NOTE: odc = $t_1/(t_1 + t_2)$ x 100%

Figure 7-3. Output Skew and Output Duty Cycle (PLL Mode)



NOTE: $t_{sk(p)}=|t_{PLH}-t_{PHL}|$

Figure 7-4. Propagation Delay and Pulse Skew (Non-PLL Mode)

8 Detailed Description

8.1 Overview

The CDCVF25081 is a low jitter, low skew, phase-locked loop clock buffer solution. Unlike many products containing PLLs, the CDCVF25081 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost. Two banks of four outputs each provide buffered copies of the CLKIN.

8.2 Functional Block Diagram

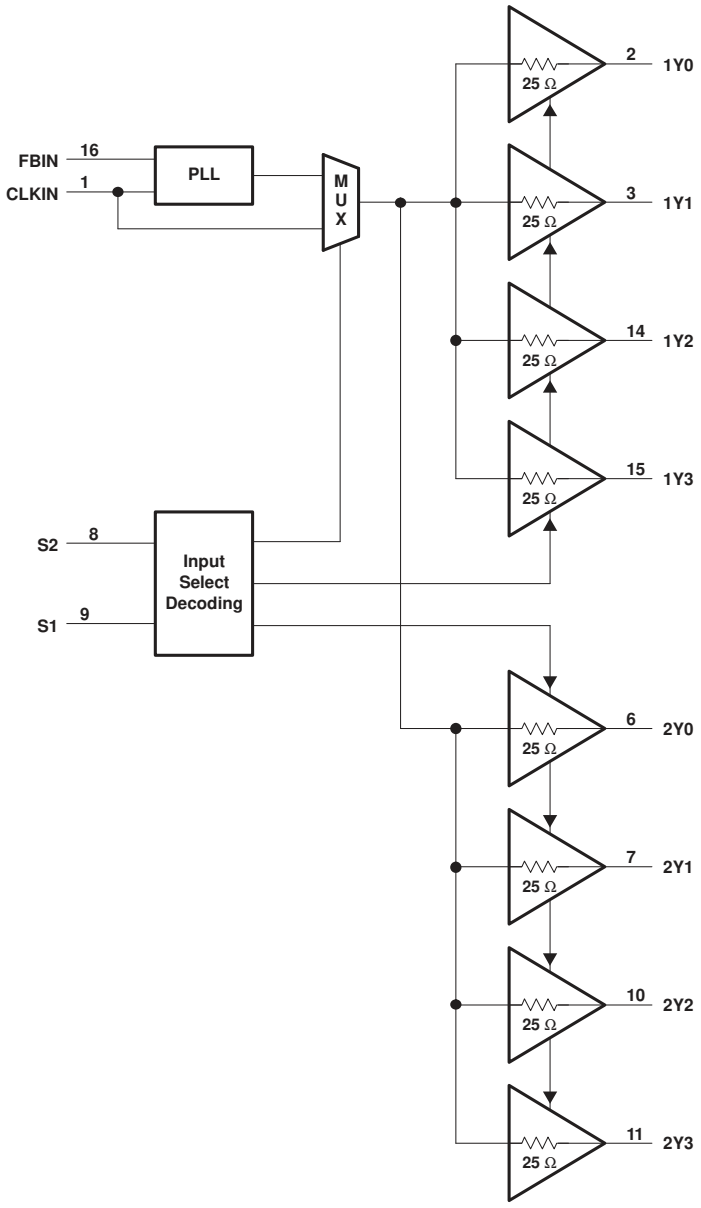


Figure 8-1. Functional Block Diagram

8.3 Feature Description

The CDCVF25081 has an integrated PLL with a dedicated feedback pin (FBIN) for synchronization and zero-delay. FBIN must be directly routed to a clock output to complete the feedback loop. When no input is applied to the CLKIN pin, the device powers down the outputs by setting them to a low logic level.

Because it is based on a PLL circuitry, the CDCVF25081 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This time is required following power up and application of a fixed-frequency signal at CLKIN and any changes to the PLL reference.

Output duty cycles are adjusted to 50%, independent of duty cycle at CLKIN. Each output has an internal series damping resistor of 25 ohms useful in driving point-to-point loads. Unused outputs can be left floating to reduce overall system cost.

Table 8-1 lists the output bank mapping of the CDCVF25081.

Table 8-1. Output Bank Mapping

BANK	CLOCK OUTPUTS
0	1Y0, 1Y1, 1Y2, 1Y3
1	2Y0, 2Y1, 2Y2, 2Y3

8.4 Device Functional Modes

The CDCVF25081 operates from a 3.3-V supply. Table 8-2 shows the output logic states of the device based on the selection pins. Based on the input selection pins (S1 and S2), the two output banks can be set as PLL outputs, bypassed PLL outputs, or high impedance.

Table 8-2. Output Logic Table

S2	S1	Bank 1	Bank 2	OUTPUT SOURCE	PLL SHUTDOWN
0	0	Hi-Z	Hi-Z	N/A	Yes
0	1	Active	Hi-Z	PLL(1)	No
1	0	Active	Active	Input clock (PLL bypass)	Yes
1	1	Active	Active	PLL(1)	No

(1) If CLKIN < 2 MHz, then the outputs are switched to a LOW level.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The CDCVF25081 is a low additive jitter, phase-locked loop driver that can operate up to 200 MHz with a 3.3-V supply. The PLL circuitry is internal to device requiring no additional configuration by the user.

9.2 Typical Application

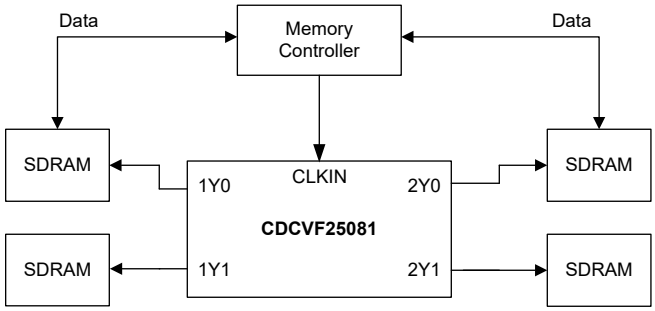


Figure 9-1. System Configuration Example

9.2.1 Design Requirements

Any output pin can be used to synchronize the FBIN to the outputs. TI recommends to not have a load on the output routed to the FBIN pin for optimum results.

9.2.2 Detailed Design Procedure

Unused outputs can be left floating. See the *Power Supply Recommendations* section for recommended filtering techniques.

9.2.3 Application Curves

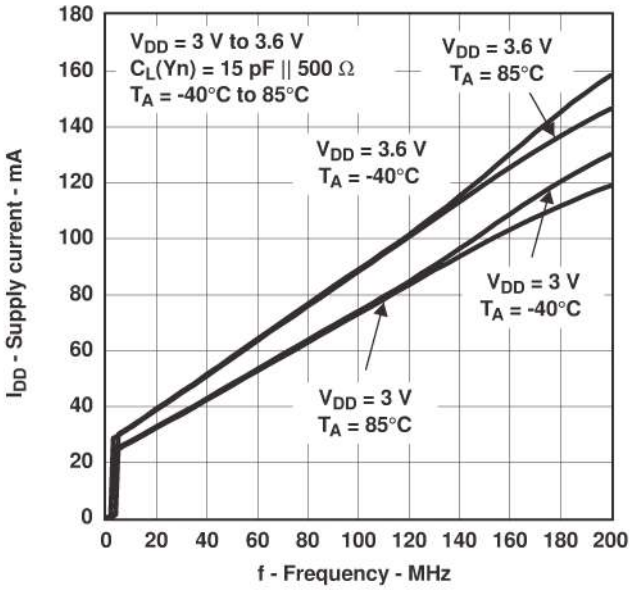


Figure 9-2. Supply Current vs. Frequency

10 Power Supply Recommendations

High-performance clock buffers can be sensitive to noise on the power supply, which may dramatically increase the additive jitter of the buffer. Thus, it is essential to manage any excessive noise from the system power supply, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer. These beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 10-1 shows the recommended power supply decoupling method.

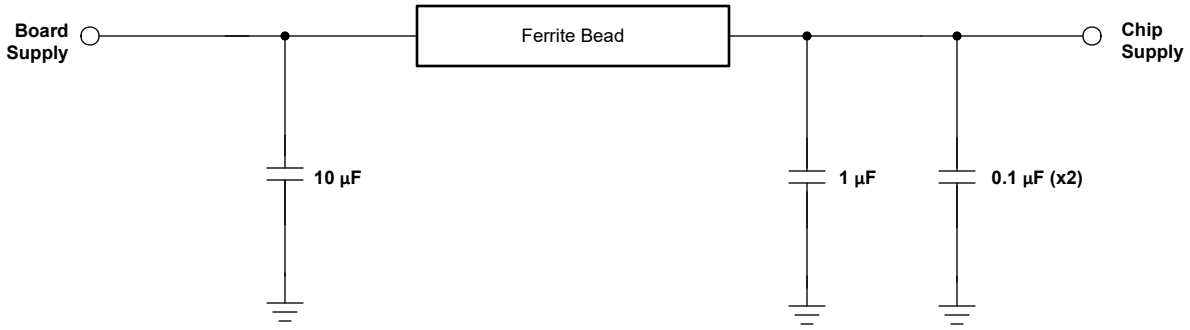


Figure 10-1. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

Figure 11-1 shows a conceptual layout detailing recommended placement of power-supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

11.2 Layout Example

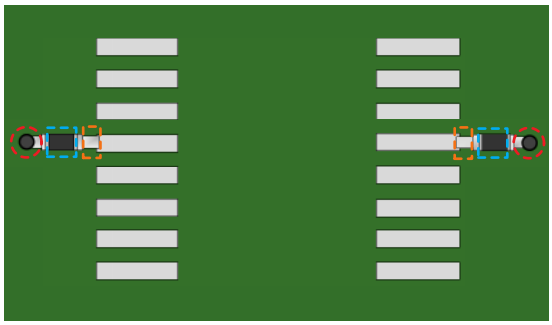


Figure 11-1. PCB Conceptual Layout

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF25081D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

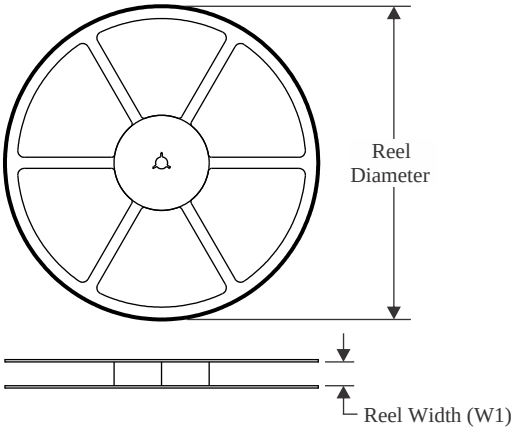
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

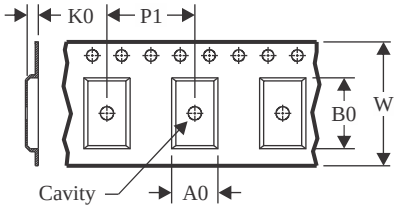
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

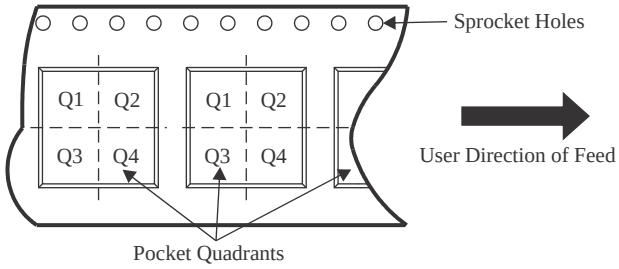


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

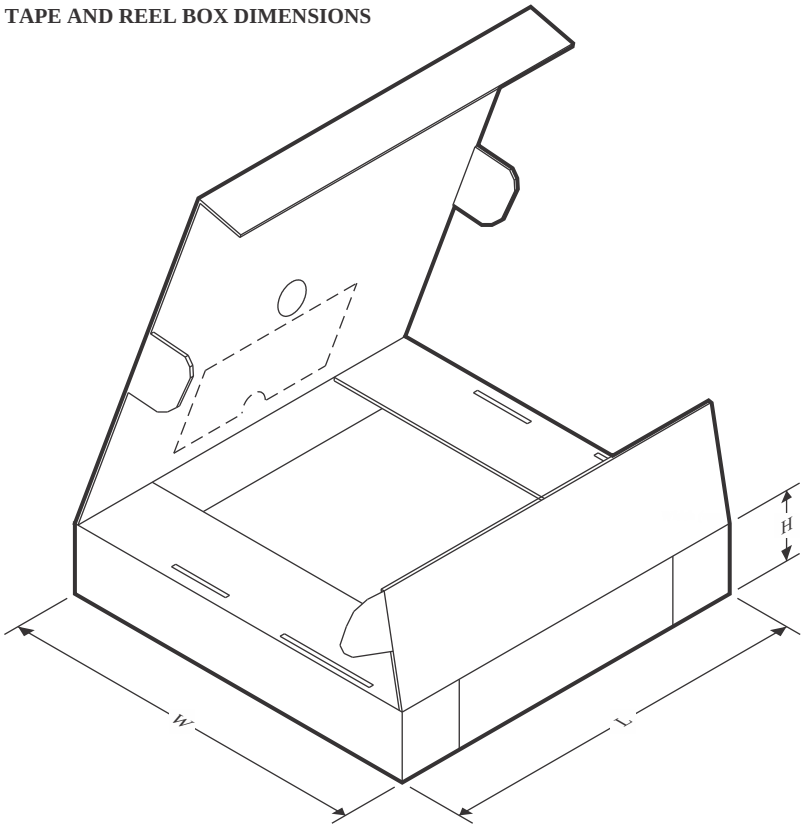
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF25081DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CDCVF25081PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

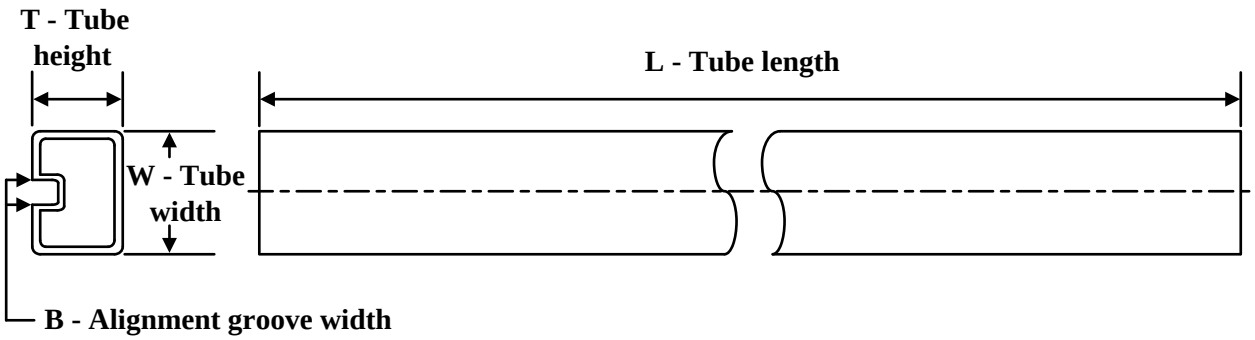
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF25081DR	SOIC	D	16	2500	350.0	350.0	43.0
CDCVF25081PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

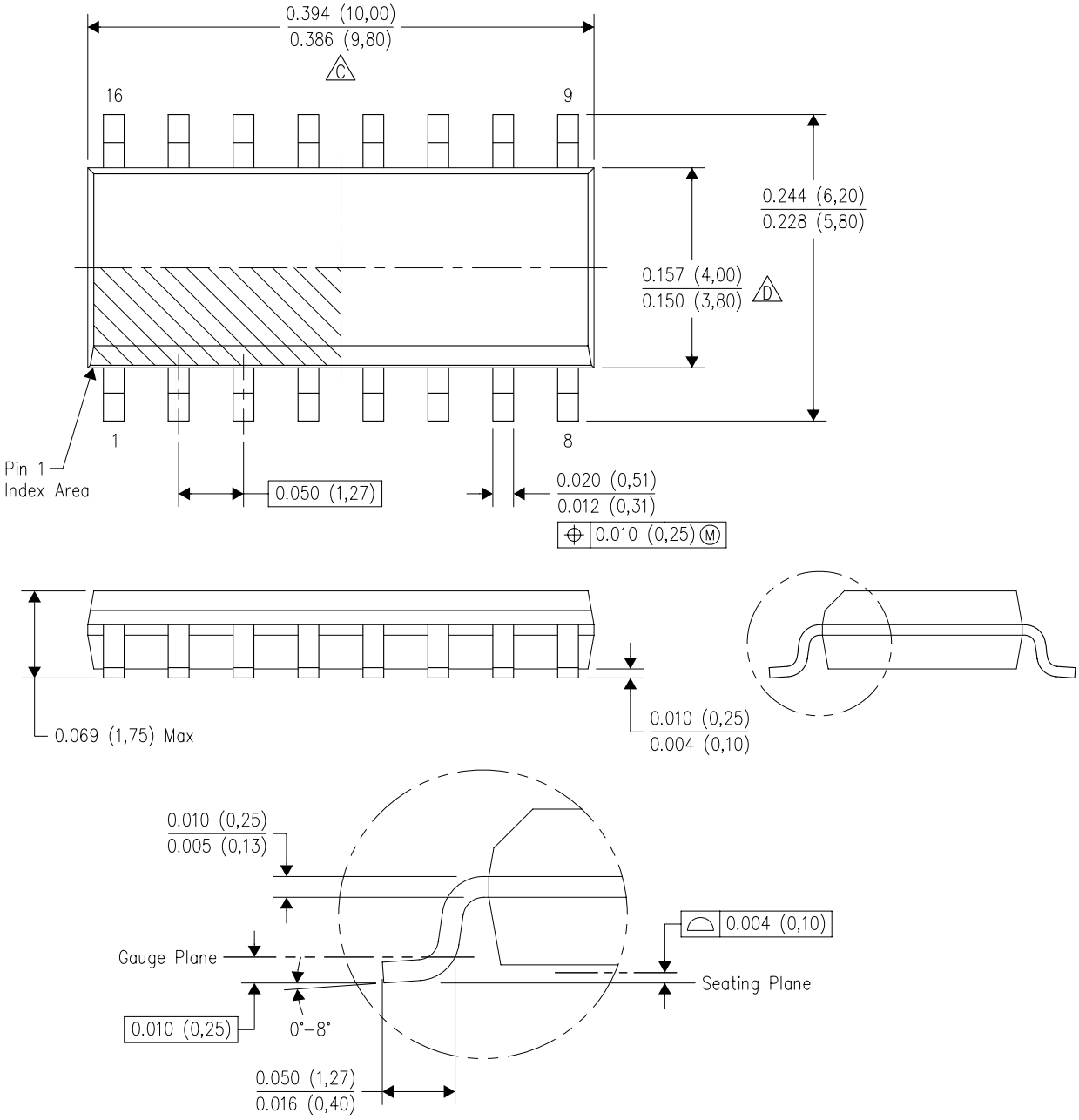
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDCVF25081D	D	SOIC	16	40	505.46	6.76	3810	4
CDCVF25081PW	PW	TSSOP	16	90	530	10.2	3600	3.5
CDCVF25081PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

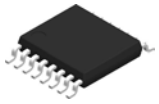
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

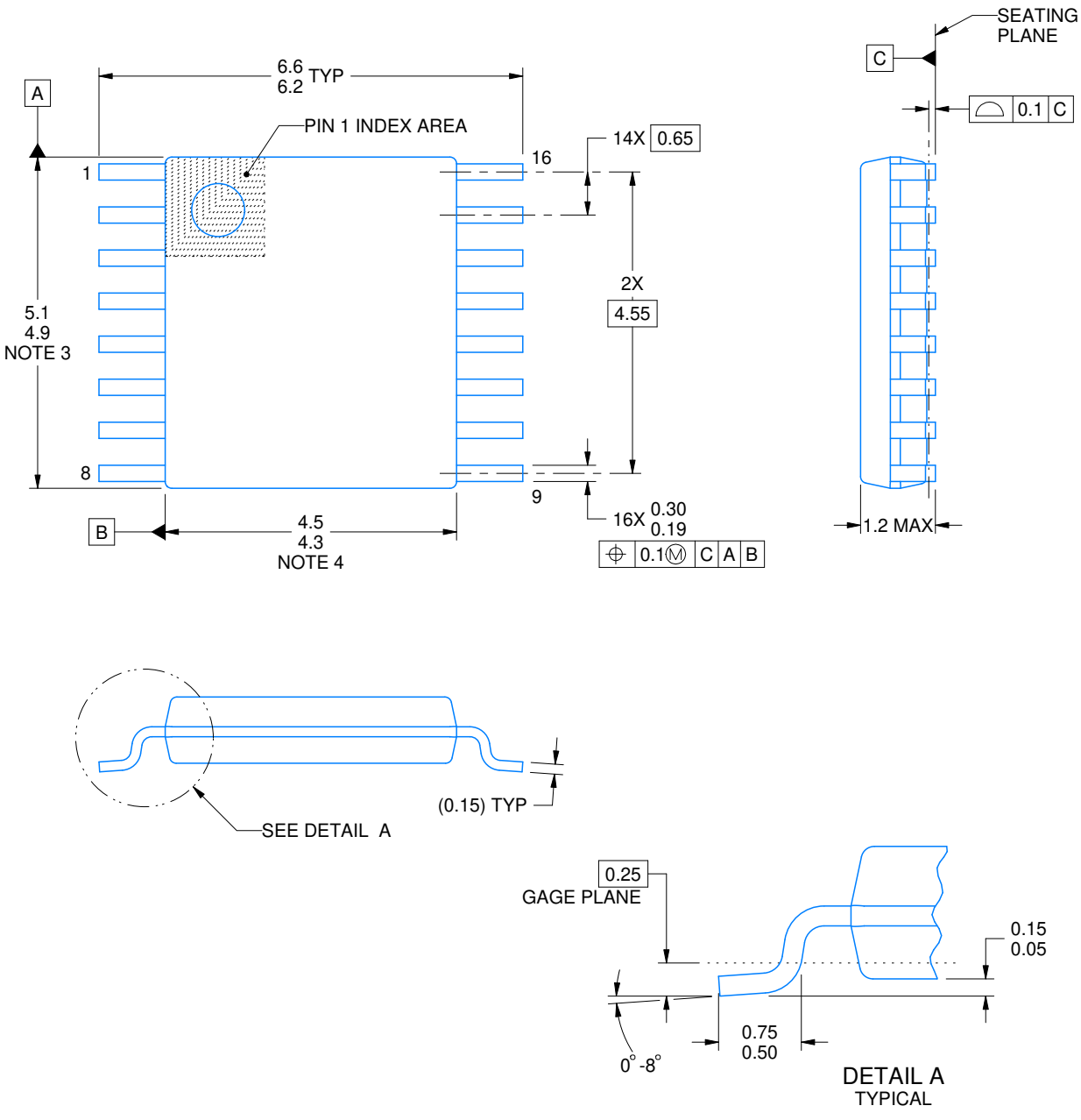
PACKAGE OUTLINE

PW0016A



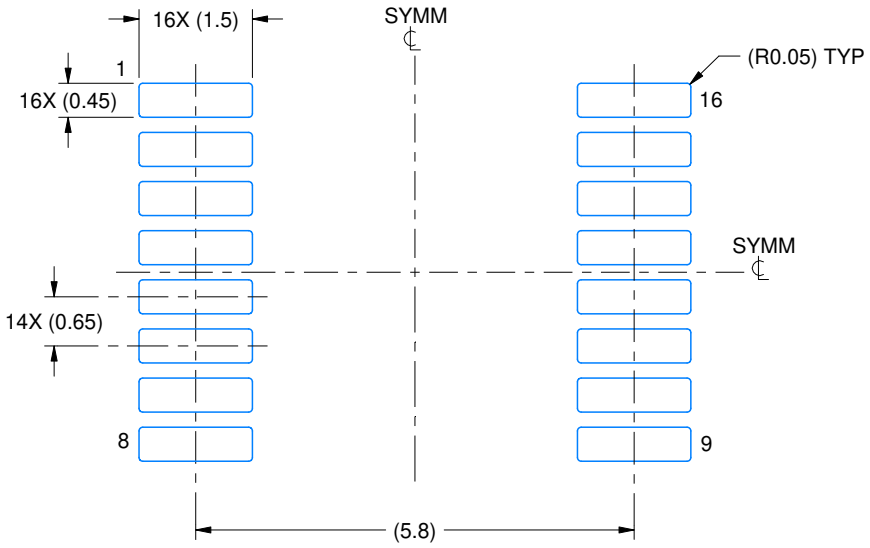
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

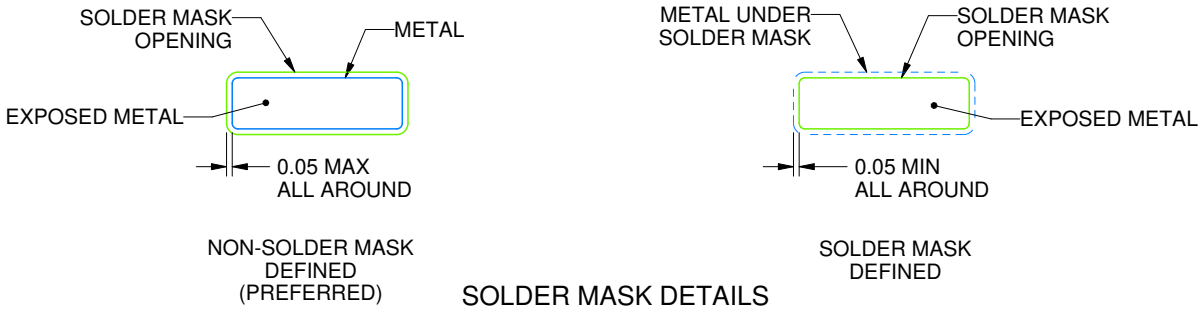


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

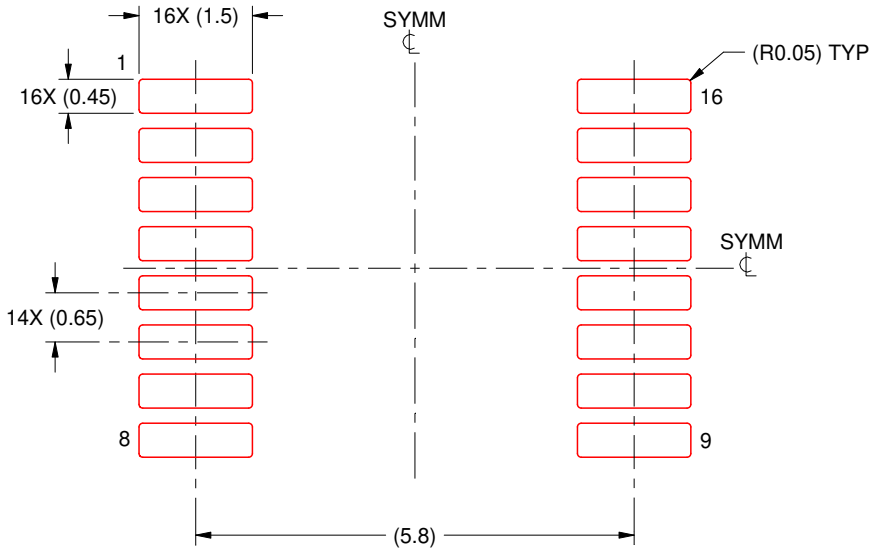


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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