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ATP AN32V6416SQGAM

256MB PC133 UNBUFFERED NON-ECC SODIMM

DESCRIPTION

The ATP AN32V6416SQGAM is a high performance 256MB PC133 Unbuffered NON-ECC SDRAM memory module. It is organized as 32M x 64 in a 144-pin Small Outline Dual-In-Line Memory Module (SODIMM) package. The module utilizes eight 16Mx16 SDRAMs in TSOP-II package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- DIMM Density: 256MB (32M x 64)
- DIMM Rank: 2 Rank
- Cycle Time: 7.5ns (133MHz)
- CAS Latency: 3
- LVTTL compatible inputs and outputs
- Power supply: 3.3V ± 0.3V
- Burst lengths: 1, 2, 4, 8 & Full page
- JEDEC compatible pin out
- Separate power and ground planes to improve noise immunity
- PCB Height: 1.25 inches
- Minimum Thickness of Golden Finger: 30 Micro-inch
- RoHS compliant

Part No.	Max Freq	Interface
AN32V6416SQGAM	133MHz (7.5ns@CL=3)	LVTTL

PIN DESCRIPTION

Pin Name	Description	Pin Name	Description
A0~A12	Addresses Input	SA0~SA2	Address in EEPROM
BA0, BA1	Bank Select	SCL	Serial Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	Serial Data Input / Output
CK0~CK1	Clock Inputs	VDD	Power Supply (3.3V)
$\overline{RAS}$	Row Address Strobes	VSS	Ground
$\overline{CAS}$	Column Address Strobes	CKE0	Clock Enable
S0#-S1#	Chip Select	NC	No Connection
$\overline{WE}$	Write Enable	DNU	Do Not Use
DQMB0~DQMB7	Data Mask		

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PIN ASSIGNMENT

No.	Front	No.	Back	No.	Front	No.	Back
1	Vss	2	Vss	71	S1#	72	DNU
3	DQ0	4	DQ32	73	NC	74	CK1
5	DQ1	6	DQ33	75	Vss	76	Vss
7	DQ2	8	DQ34	77	DNU	78	DNU
9	DQ3	10	DQ35	79	DNU	80	DNU
11	VDD	12	VDD	81	VDD	82	VDD
13	DQ4	14	DQ36	83	DQ16	84	DQ48
15	DQ5	16	DQ37	85	DQ17	86	DQ49
17	DQ6	18	DQ38	87	DQ18	88	DQ50
19	DQ7	20	DQ39	89	DQ19	90	DQ51
21	Vss	22	Vss	91	Vss	92	Vss
23	DQMB0	24	DQMB4	93	DQ20	94	DQ52
25	DQMB1	26	DQMB5	95	DQ21	96	DQ53
27	VDD	28	VDD	97	DQ22	98	DQ54
29	A0	30	A3	99	DQ23	100	DQ55
31	A1	32	A4	101	VDD	102	VDD
33	A2	34	A5	103	A6	104	A7
35	Vss	36	Vss	105	A8	106	BA0
37	DQ8	38	DQ40	107	Vss	108	Vss
39	DQ9	40	DQ41	109	A9	110	BA1
41	DQ10	42	DQ42	111	A10	112	A11
43	DQ11	44	DQ43	113	VDD	114	VDD
45	VDD	46	VDD	115	DQMB2	116	DQMB6
47	DQ12	48	DQ44	117	DQMB3	118	DQMB7
49	DQ13	50	DQ45	119	Vss	120	Vss
51	DQ14	52	DQ46	121	DQ24	122	DQ56
53	DQ15	54	DQ47	123	DQ25	124	DQ57
55	Vss	56	Vss	125	DQ26	126	DQ58
57	DNU	58	DNU	127	DQ27	128	DQ59
59	DNU	60	DNU	129	VDD	130	VDD
Voltage Key				131	DQ28	132	DQ60
				133	DQ29	134	DQ61
61	CK0	62	CKE0	135	DQ30	136	DQ62
63	VDD	64	VDD	137	DQ31	138	DQ63
65	$\overline{RAS}$	66	$\overline{CAS}$	139	Vss	140	Vss
67	$\overline{WE}$	68	CKE1	141	SDA	142	SCL
69	S0#	70	A12	143	VDD	144	VDD

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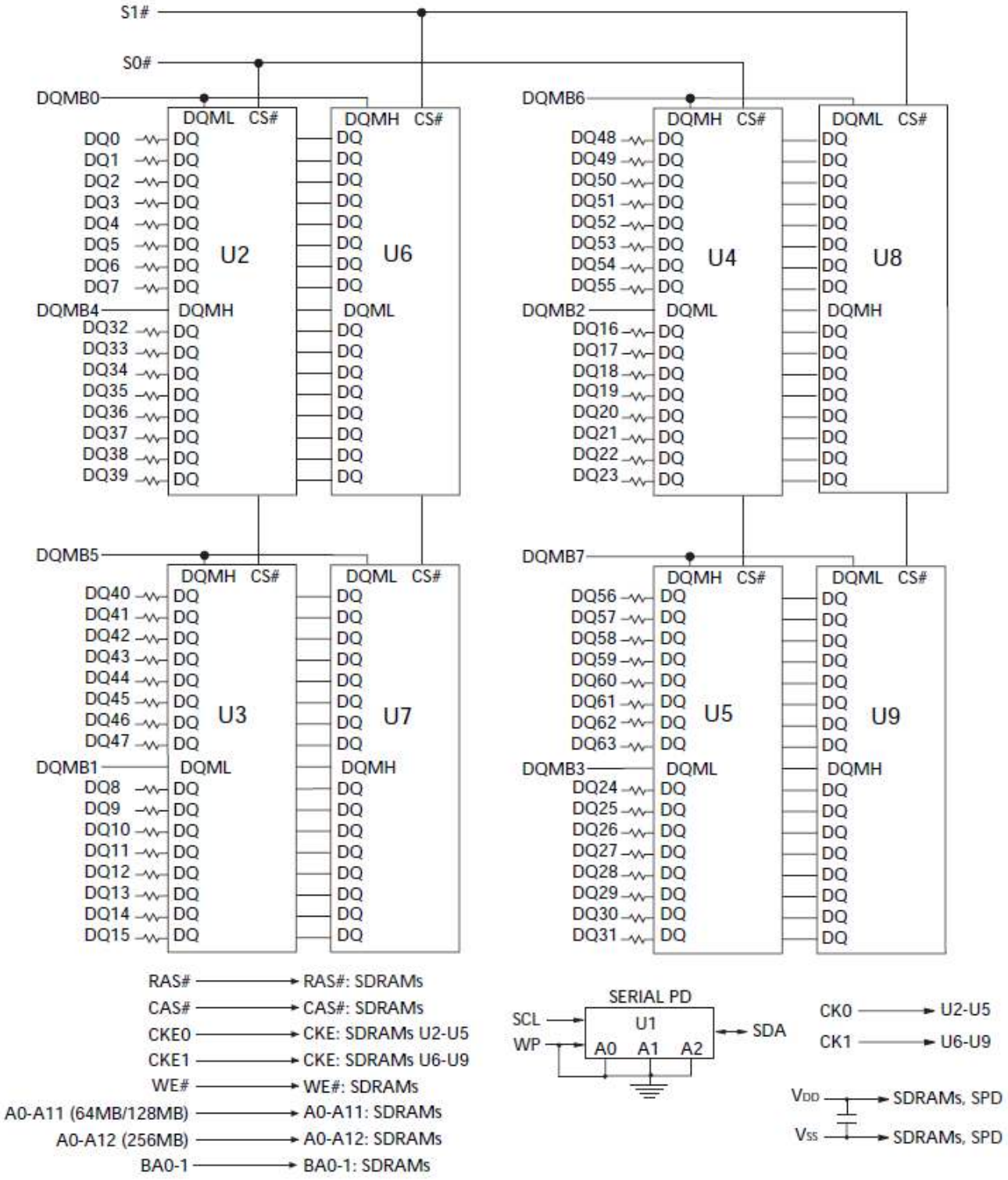
FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-1.0V ~ 4.6V	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0V ~ 4.6V	V	1
Short Circuit Output Current	I_{OS}	50	mA	1
Storage Temperature	T_{STG}	-55 to +150	^{o}C	1,2
Operating Temperature (Ambient)	T_A	0 to +70	^{o}C	1

Note:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC OPERATING CONDITIONS (LVTTL)

Item	Symbol	Min.	Typical	Max.	Units	Notes
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{DD} + 0.3	V	1
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH}=-4mA
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL}=4mA

Note:
1. VIH (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

CAPACITANCE

(V_{DD}=3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Max.	Unit
Input Capacitance (CKE)	C_{I1}	40	pF
Input Capacitance (Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}	40	pF
Input Capacitance ($\overline{CS}$)	C_{I3}	40	pF
Input Capacitance (CK)	C_{CK}	16	pF
Input/Output Capacitance (DQMB)	C_{IO}	6	pF

IDD SPECIFICATION PARAMETER

Values are for the AN32V6416SQGAM DDR SDRAM only and are computed from values specified in the MT48LC16M16A2P-6A:G component data sheet

Symbol	Proposed Conditions	Value	Units
IDD1	**OPERATING CURRENT: Active Mode;** Burst = 2; READ or WRITE; tRC = tRC (MIN)	510	mA
IDD2	**STANDBY CURRENT: Power-Down Mode;** All device device banks idle; CKE = LOW	16	mA
IDD3	**STANDBY CURRENT: Active Mode** CKE = HIGH; CS0# = HIGH; All device banks active after tRCD met; No accesses in progress	170	mA
IDD4	**Operating current(Burst mode)** IO = 0 mA; Page burst; 4Banks activated; tCCD = 2CLKs	550	mA
IDD5	**AUTO REFRESH CURRENT**; tRFC = tRFC (MIN)	2,160	mA
IDD6	**AUTO REFRESH CURRENT** tRFC = 15.625μs	28	mA
IDD7	**Self refresh current** CKE ≤ 0.2V, Standard	20	mA
	Self refresh current CKE ≤ 0.2V,Low Power	12	mA

TIMING PARAMETER

Parameter	Symbol	PC133		Units
		min	Max	
CLK cycle time(CAS latency=3)	t_{CC} [3]	7.5	1,000	ns
Row Active Time	t_{RAS} [1]	44	120,000	ns
RAS Precharge Time	t_{RP} [1]	20	-	ns
Row Cycle Time	t_{RC} [1]	66	-	ns
RAS to CAS Delay Time	t_{RCD} [1]	20	-	ns
RAS to RAS Delay Time	t_{RRD} [1]	15	-	ns
CAS to CAS Delay Time	t_{CCD} [2]	1	-	CLK
CLK to valid output delay	t_{SAC} [3, 4]	-	5.4	ns
Output Hold Time	t_{OH} [4]	3.0	-	ns
Clock High Time	t_{CH} [5]	2.5	-	ns
Clock Low Time	t_{CL} [5]	2.5	-	ns
Input Setup Time	t_{SS} [5]	1.5	-	ns
Input Hold Time	t_{SH} [5]	0.8	-	ns
CLK to output in Low-Z	t_{SLZ} [4]	1.0	-	ns
CLK to output in Hi-Z	t_{SHZ}	-	5.4	ns

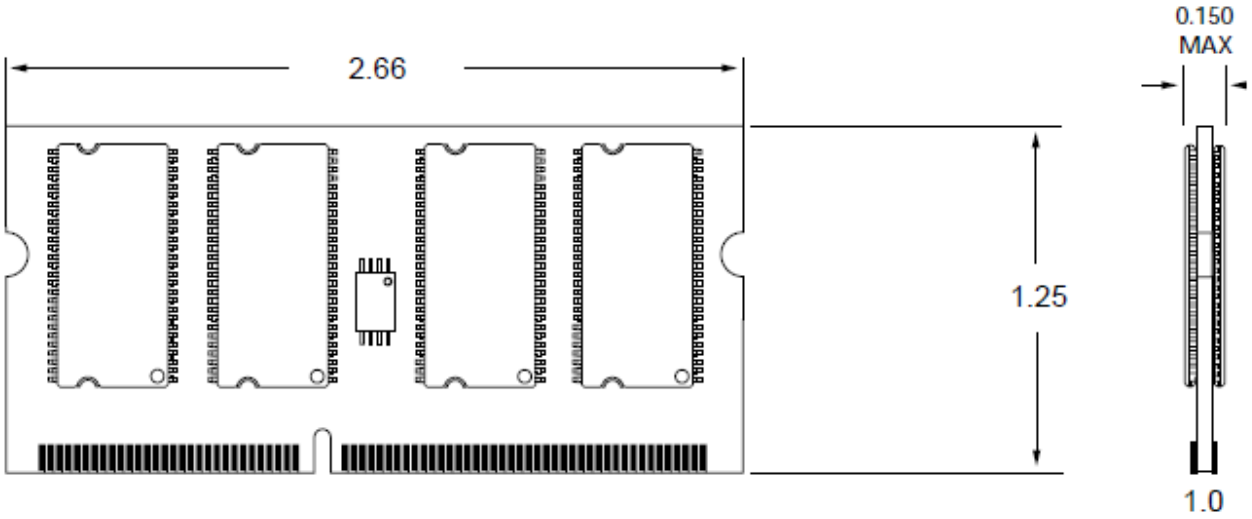
Notes:
1. The minimum number of clock cycles is determined and then rounding off to the next higher integer.
2. All parts allow every cycle column address change.
3. Parameters depend on programmed CAS latency.
4. If clock rising time is longer than 1ns, (tr/2-0.5) ns should be added to the parameter.
5. Assumed input rise and fall time (tr & tf) = 1ns. If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1] ns should be added to the parameter.

PHYSICAL DIMENSIONS (UNITS IN INCHES)

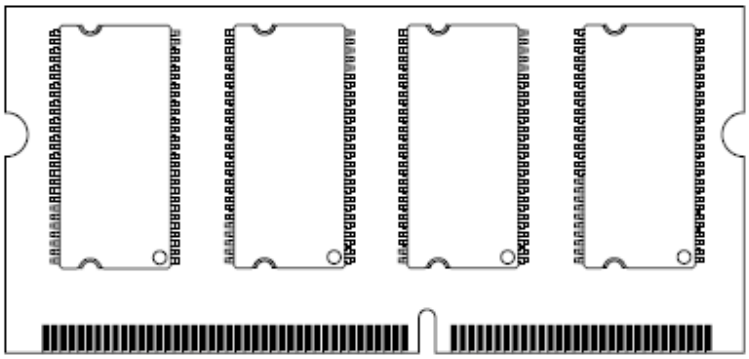
(Drawing not to scale)

144-pin DIMM

Front



Back



Note: Tolerance on all dimensions ±0.006 inch (0.15mm) unless otherwise noted

Disclaimer:

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