NCT80

Hardware Monitor with I²C Serial Interface

The NCT80 is a two−wire serially programmable hardware monitor. It can monitor its on chip temperature via its local sensor, 7 analog inputs and measure the speed of two fans. Each of the measured values are compared with programmable limits and if any channel is outside the programmed limit an interrupt is generated via the $\overline{\text{INT}}$ output pin. It also has a chassis intrusion detection input pin which is latched on an intrusion event.

Communication with the NCT80 is accomplished via the I²C interface which is compatible with industry standard protocols. Through this interface the NCT80s internal registers may be accessed. These registers allow the user to read the current temperature, fan speed and voltages, change the configuration settings and adjust each channels limits.

The NCT80 is available in a 24−lead TSSOP package and operates over a wide supply range of 2.8 to 5.75 V. This makes the NCT80 ideal for a wide variety of applications ranging from computers to servers and test equipment.

Features

- On−chipTemperature Sensor
- 2 Fan Speed Monitoring Inputs
- 7 Analog Inputs for Voltage Monitoring
- Chassis Intrusion Detection
- Overtemperature Output
- Limit Comparison of Monitored Channels
- 3 Address Selection Pins
- Power Saving Shutdown Mode
- I²C Compliant Interface
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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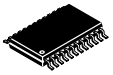
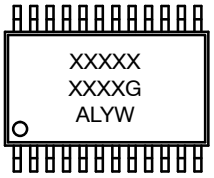
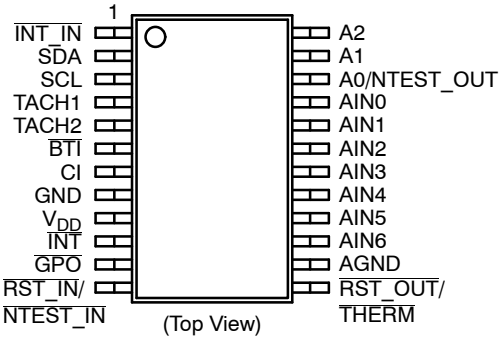


TSSOP−24
DB SUFFIX
CASE 948H



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCT80DBR2G	TSSOP−24 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

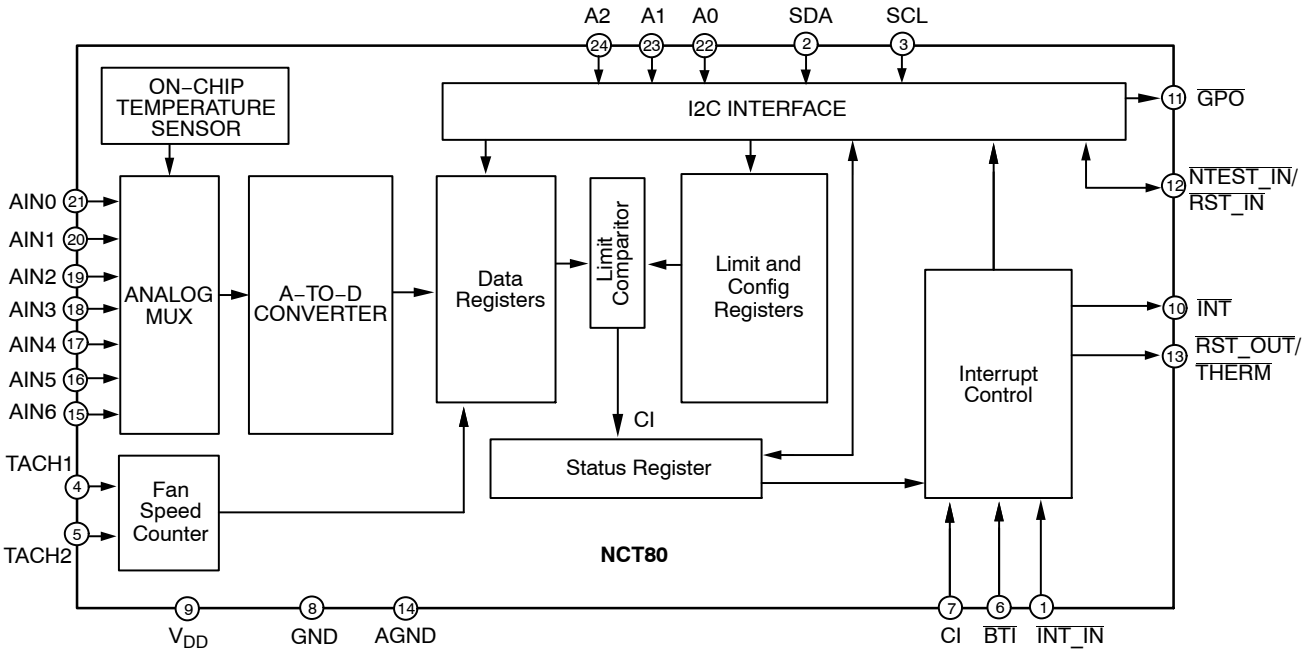


Figure 1. Functional Block Diagram of NCT80

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	$\overline{\text{INT\_IN}}$	Active low digital input. This signal is propagated to the $\overline{\text{INT}}$ output pin of the NCT80.
2	SDA	I^2C Serial Bi−directional Data Input/Output. Open−drain pin; needs a pull−up resistor.
3	SCL	Serial Clock Input. Open−drain pin; needs a pull−up resistor.
4	TACH1	Digital Input. Fan tachometer input to measure speed of Fan.
5	TACH2	Digital Input. Fan tachometer input to measure speed of Fan.
6	$\overline{\text{BTI}}$	Digital Input. Board Temperature Interrupt driven by O.S. outputs of additional temperature sensors such as the NCT75.
7	CI (Chassis Intrusion)	Digital I/O. An active high input from an external latch which captures a Chassis Intrusion event. This line can go high without any clamping action, regardless of the powered state of the NCT80
8	GND	Power Supply Ground.
9	V_{DD}	Positive Supply Voltage. Bypass to ground with a 0.1 μF bypass capacitor.
10	$\overline{\text{INT}}$	Digital Output. Open drain Interrupt Request pin.
11	$\overline{\text{GPO}}$	Digital Output. An active low open drain output intended to drive an external P−channel power MOSFET in order to offer software power control.
12	$\overline{\text{NTEST\_IN}}/\overline{\text{RST\_IN}}$	Dual function pin. Active low input that enables NAND Tree Test functionality. Once enabled the part is reset to its power on default.
13	$\overline{\text{RST\_OUT}}/\overline{\text{THERM}}$	Dual function pin. RST_OUT: Active low reset output pin. $\overline{\text{THERM}}$: Overtemperature shutdown output pin.
14	AGND	Analog Ground.
15	AIN6	Analog Input. 0 V to 2.56 V.
16	AIN5	Analog Input. 0 V to 2.56 V.
17	AIN4	Analog Input. 0 V to 2.56 V.
18	AIN3	Analog Input. 0 V to 2.56 V.
19	AIN2	Analog Input. 0 V to 2.56 V.
20	AIN1	Analog Input. 0 V to 2.56 V.
21	AIN0	Analog Input. 0 V to 2.56 V.
22	A0/NTEST_OUT	Dual function pin. Functions as an I^2C address selection bit. This is the LSB of the address. Pin also functions as an output when performing a NAND test.
23	A1	Functions as an I^2C address selection bit.
24	A2	Functions as an I^2C address selection bit.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{DD})	V_{DD}	−0.3 to +6.5	V
Voltage on any input or output pin		−0.3 to V_{DD} + 0.3	V
Input Current at any pin	I_{IN}	±5	mA
Maximum Junction Temperature	$T_{J(max)}$	150.7	°C
Storage Temperature Range	T_{STG}	−65 to 160	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2500	V
ESD Capability, Machine Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Supply Voltage	V_{DD}	2.8	5.75	V
Operating Ambient Temperature Range	T_A	−40	125	°C

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 4. ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = 2.8 V to 5.75 V. All specifications for −40°C to +125°C, unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY CHARACTERISTICS					
Supply Voltage		2.8		5.75	V
Supply Current	Interface inactive			0.580	mA
Shutdown Current	Shutdown mode enabled		200		μA
TEMPERATURE TO DIGITAL CONVERTER CHARACTERISTICS					
Local Sensor Accuracy V_{DD} = 2.8 V to 5.75 V	T_A = 0°C to +100°C			±2	°C
	T_A = −40°C to +125°C			±3	°C
Resolution				0.0625	°C
ANALOG−to−DIGITAL CONVERTER CHARACTERISTICS					
ADC Resolution (bits)			10		Bits
Resolution (10 bits with full−scale at 2.56 V)			2.5		mV
Total Unadjusted Error (TUE)				±1	%
Differential Nonlinearity (DNL)				±1	LSB
Round Robin Cycle Time		662	728	810	ms
MULTIPLEXER/ADC INPUT CHARACTERISTICS					
On resistance			11.5	13	kΩ
Input current (on channel leakage current)			±0.005		μA
Off channel leakage current			±0.005		μA
FAN RPM−to−DIGITAL CONVERTER					
Fan RPM Error	T_A = −40°C to +125°C			±10	%
Full scale count				255	(max)
TACH1 & TACH2 Nominal Input RPM	Divisor = 1, Fan count = 153		8800		rpm

Table 4. ELECTRICAL CHARACTERISTICS
($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = 2.8 V to 5.75 V. All specifications for −40°C to +125°C, unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
FAN RPM−to−DIGITAL CONVERTER					
TACH1 & TACH2 Nominal Input RPM	Divisor = 2, Fan count = 153		4400		rpm
	Divisor = 3, Fan count = 153		2200		rpm
	Divisor = 4, Fan count = 153		1100		rpm
Internal Clock Frequency		20.2	22.5	24.8	kHz
DIGITAL OUTPUTS (A0/ $\overline{\text{NTEST\_OUT}}$, $\overline{\text{INT}}$)					
Output high voltage, logical “1”	I_{OUT} = +5.0 mA, V_{DD} = 2.8 V – 5.75 V	2.4			V
Output low voltage, logical “0”	I_{OUT} = −5.0 mA, V_{DD} = 2.8 V – 5.75 V			0.4	V
OPEN DRAIN OUTPUTS ($\overline{\text{GPO}}$, $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$, CI, SDA)					
Output low voltage, logical “0”	I_{OUT} = +5.0 mA, V_{DD} = 3.6 V			0.4	V
High level output current	$V_{OUT} = V_{DD}$		0.1	1	μA
$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$, CI pulse width		10	22.5		ms
DIGITAL INPUTS (Except for $\overline{\text{BTI}}$)					
Input high voltage, logical “1”		0.7 x V_{DD}			V
Input low voltage, logical “0“				0.3 x V_{DD}	V
ALL DIGITAL INPUTS (Except for $\overline{\text{BTI}}$)					
Input current (Logical “1“)	$V_{IN} = V_{DD}$	−1	−0.005		μA
Input current (Logical “0“)	V_{IN} = 0 V		0.005	1	μA
Input capacitance			20		pF
$\overline{\text{BTI}}$ DIGITAL INPUT					
Input current (Logical “1“)	$V_{IN} = V_{DD}$	−10			μA
Input current (Logical “0“)	V_{IN} = 0 V			2000	μA
Input capacitance			20		pF

Table 5. I²C TIMING

Parameter (Note 4)	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Clock Frequency	f_{SCLK}	10		400	kHz
Clock Period	t_1	2.5		100	μs
Data Setup Time (Note 5)	t_2	100			ns
Data Out Stable	t_3	0		0.9	μs
Start Hold Time (Note 6)	t_4	100			ns
Stop Setup Time	t_5	100			ns
SCL High Time	t_6	0.6			μs
SCL Low Time	t_7	1.3			μs
Start Setup Time	t_8	0.6			μs
SCL, SDA Rise Time	t_9			300	ns
SCL, SDA Fall Time	t_{10}			300	ns
Bus Free Time	t_{11}	1.3			μs
Glitch Immunity	t_{12}	0		50	ns
Timeout	$t_{Timeout}$	25		35	ms

4. Guaranteed by design, but not production tested.
5. Time for 10% or 90% of SDA to 10% of SCL.
6. Time from 10% of SDA to 90% of SCL.

TYPICAL CHARACTERISTICS

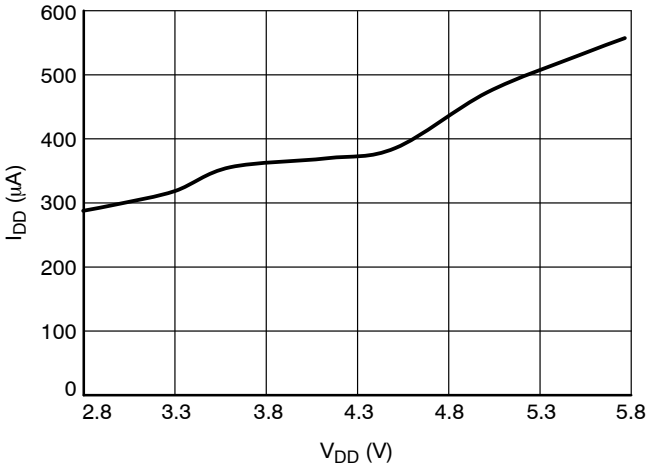


Figure 2. Supply Current vs. V_{DD}

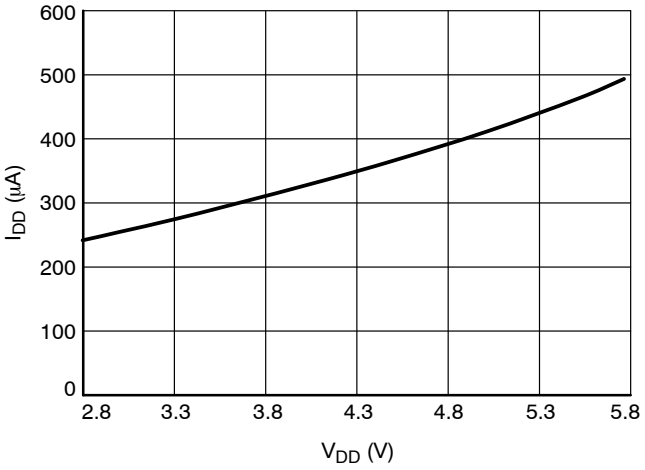


Figure 3. Supply Current vs. V_{DD} (Voltage Conversion)

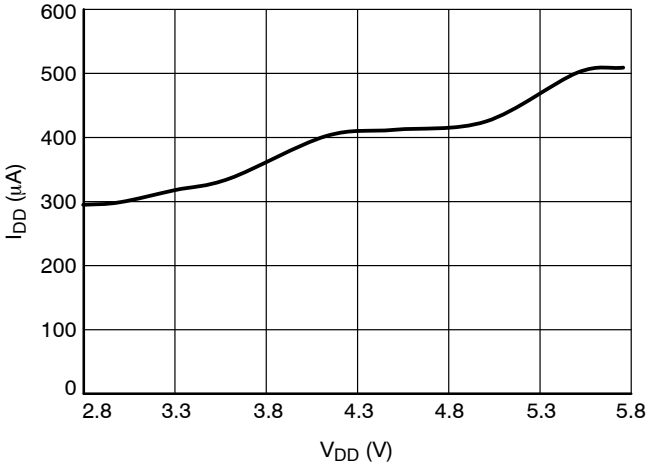


Figure 4. Supply Current vs. V_{DD} (Temperature Conversion)

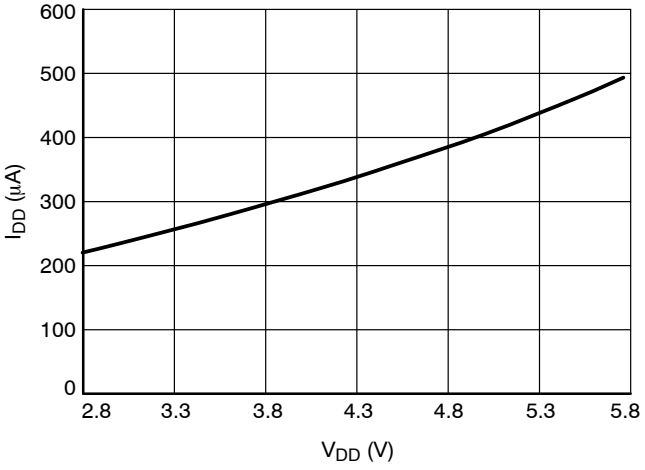


Figure 5. Shutdown Current vs. V_{DD}

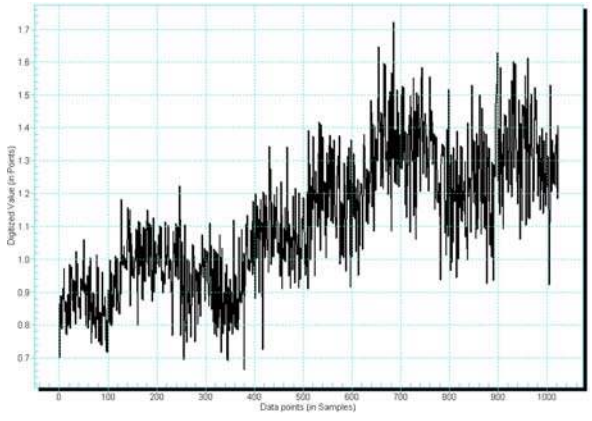


Figure 6. TUE vs. Code

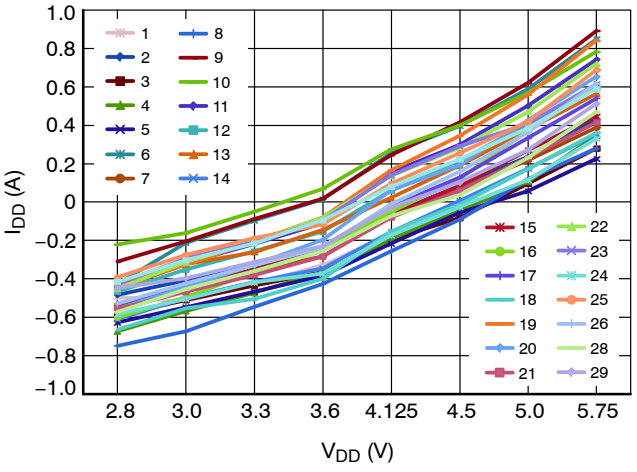


Figure 7. Local Temp Error vs. V_{DD}

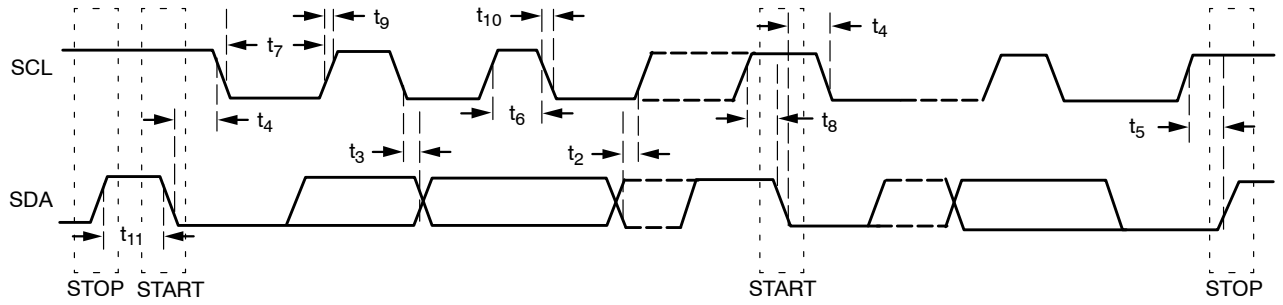


Figure 8. Serial Interface Timing

Theory of Operation

The NCT80 contains an on chip local temperature sensor, an 8 channel multiplexer, a 10 bit sigma−delta analog to digital converter and different internal registers in a single package. It has the capability to monitor 7 analog inputs AIN0−AIN6. The effective use of these analog inputs can be accomplished by connecting them to monitor different power supplies level present in any communication system. It also has two fan speed measurement inputs that can be configured either as fan failure signal or the tachometer signal. The fan inputs are digital signals with transition levels according to the fan tach pulse inputs in the electrical characteristics table. The signal conditioning circuitry is present on the chip to accommodate slow rise and fall times. The nominal fan speeds are programmable from 1100 to 8800 RPM (based on count of 153). Full scale fan counts are 255 (8bit counter) which represents a very slow or stopped fan.

The communication interface with the device is accomplished by an I^2C interface that is compatible to both Standard Mode and Fast Mode operations. The standard and fast modes correspond to 100 kHz and 400 kHz. NCT80 also has a three address selection pins A0−A2 that facilitate the use of eight devices on a single bus.

Internal Registers

In this section the overview of important internal registers is presented. NCT80 contains 41 internal registers the details of whom can be seen in the register map section.

Configuration Register: This register can be accessed for control and configuration.

Interrupt Status Registers: There are two registers that provide the status of each interrupt alarm. Continuous reading of the status register can make the bits in the register toggle intermittently and momentarily clears the $\overline{\text{INT}}$ pin also.

Interrupt Mask Registers: These registers can be accessed for masking of individual interrupt sources, as well as separate masking for both hardware interrupt outputs.

Fan Divisor Output pin Configuration: This register can be accessed to configure fan reading modes and also the $\overline{\text{OS}}$ and $\overline{\text{RST\_OUT}}$ pin configuration. Bits 0 to 5 of this register contain the divisor bits for the TACH1 and TACH2 inputs. Bits 6 and 7 control the function of the $\overline{\text{RST\_OUT}}/\overline{\text{OS}}$ output.

OS Configuration/Temperature Resolution Register: This register can be accessed to configure the $\overline{\text{OS}}$ output pin and the temperature sensor resolution. The resolution can be configured either 9 bit or 12 bit. Bit 3 enables 12−bit temperature conversions. In 12−bit mode, bits 4 to 7 represent the four LSBs of the temperature measurement. In 9−bit mode, bit 4 represents the LSB of the temperature measurement.

Conversion Rate Register: This register can be accessed to control the conversion rate of the ADC.

Channel Add/Remove Register: This register can be accessed by the user to manually add or remove measurement channels from the ADC.

RAM Registers: The results for monitoring fan counts, temperature, voltages etc are all contained in it. It consists of 31 bytes with the first 10 bytes are the results and the next 20 bytes are the interrupt alarm limit registers. Limit values for analog measurements are stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt request will be generated if the measured value goes above or below acceptable values. In the case of temperature, a Hot Temperature (high limit), and a Hot Temperature Hysteresis (low limit) can be programmed. The hysteresis value is usually a few degrees lower than the high limit. These limits allow the system to be shut down when the hot limit is exceeded and restarted automatically when the temperature has dropped below the hysteresis limit.

The last byte is the upper locations for manufacturer ID.

Application Details

Power−ON_RESET

When NCT80 is turned ON by applying power to V_{DD} pin it undergoes to a reset mode where most of the internal registers are reset. The Interrupt and RAM registers do not reset on power ON and their values are determined immediately after the reset process. The configuration register bit 7 has the same function as the power ON reset. This bit can be set to 1 to initiate the reset process which clears automatically afterwards.

Initiating Inputs Monitoring

The monitoring cycle of the NCT80 begins when a one is written to the Start bit (bit 0) and a zero to the INT_Clear bit (bit 3) of the Configuration Register. When the NCT80 monitoring sequence is started, it cycles sequentially

through the measurement of the 7 analog inputs. Each input is multiplexed separately into the NCT80's 10 bit ADC and stored in the appropriate value register. The on−chip temperature sensor is monitored through a 12 bit sigma delta ADC giving the temperature a resolution of 0.0625°C. At the same time the fan speed inputs are independently monitored. Once each conversion is completed the data is compared with programmed limits stored in the limit registers of RAM. It can then be read back over the serial bus.

The sequence of items that are monitored except for the temperature reading corresponds to locations in the RAM registers as follows:

1. Temperature
2. AIN0
3. AIN1
4. AIN2
5. AIN3
6. AIN4
7. AIN5
8. AIN6
9. TACH 1
10. TACH 2

Reading Results

The conversion results are stored in the value registers at addresses from 20h to 29h. These conversion results can be read at any time and correspond to the result of the last conversion. A typical sequence of events after NCT80 power−on is as follows:

1. Set alarm limits
2. Set interrupt masks
3. Start the NCT80 monitoring process

Analog Inputs

NCT80 has a 10−bit ADC which has an LSB value of 2.5 mV. The input has a full scale input range of 0 to 2.56 V. The analog inputs are often connected to power supplies whose values can be 2.5, 3.3, 5 or 12 V. This poses a requirement to attenuate the voltage inputs within the acceptable input range of the ADC.

Voltage divider can be used to attenuate the analog input voltages with in the desired range. For any applications a voltage divider with an output signal of 1.9 V to the analog inputs will be an appropriate selection. This selection will give a tolerance for upward excursion in the power supply of 25%.

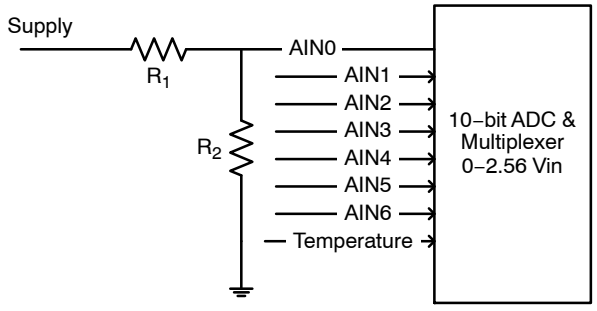


Figure 9. Resistor Divider to Attenuate the Power Supply Voltage within Required Range

The selection of resistors value can be simplified by first selecting the value of R_2. The value of R_2 should be high enough to protect both inputs under overdrive conditions and must be low enough to avoid leakage current errors. A typical value for R_2 with in 10 kΩ−100 kΩ range will serve this purpose. The value of R1 then can be selected to provide 1.9 V at the AINx pins as follows:

$$R_1 = \frac{\text{Supply} - 1.9}{1.9} \times R_2$$

It is necessary to limit input currents to avoid the Absolute maximum rating value. Extra external resistors must be used to achieve this at any pin.

Temperature Measurement

Temperature data can be read from the Temperature Reading Register at 27h. Temperature limits can be read from and written to the Hot Temperature, Hot Temperature Hysteresis, OS Temperature, and OS Temperature Hysteresis Limit Registers. These registers have addresses from 38h to 3Bh respectively. The temperature data limit is represented by 8 bit, 9 bit and 12 bit two's complement word with an LSB equal to 1°C.

Table 6. 8 BIT TEMPERATURE DATA REPRESENTATION

Temperature	Binary Output	HEX Output
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1°C	0000 0001	01h
+0°C	0000 0000	00h
−1°C	1111 1111	FFh
−25°C	1110 0111	E7h
−55°C	1100 1001	C9h

Table 7. 9 BIT TEMPERATURE DATA REPRESENTATION

Temperature	Binary Output	HEX Output
+125°C	0 1111 1010	0 FAh
+25°C	0 0011 0010	0 32h
+1.5°C	0 0000 0011	0 03h
+0°C	0 0000 0000	0 00h
−0.5°C	1 1111 1111	1 FFh
−25°C	1 1100 1110	1 CEh
−55°C	1 1001 0010	1 92h

Table 8. 12 BIT TEMPERATURE DATA REPRESENTATION

Temperature	Binary Output	HEX Output
+125°C	0111 1101 0000	7 D0h
+25°C	0001 1001 0000	1 90h
+1°C	0000 0001 0000	0 10h
+0.0625°C	0000 0000 0001	0 01h
+0°C	0000 0000 0000	0 00h
−0.0625°C	1111 1111 1111	F FFh
−1.0°C	1111 1111 0000	F F0h
−25°C	1110 0111 0000	E 70h
−55°C	1100 1001 0000	C 90h

When using a single−byte read, the eight MSBs of the temperature reading can be found in the Value RAM Register at 27h. The remainder of the temperature reading can be found in the OS_CONFIG_TEMP_RESOLUTION Register at address 06h, bits 4 to 7. In 9−bit format, bit 7 is the only valid bit. In addition, all nine or 12 bits can be read using a double−byte read at register address 27h.

Temperature Interrupts

There are four Value RAM Register limits for the temperature reading that affect the INT and OS outputs of the NCT80. These are the HOT_TEMP_HIGH_LIMIT (HTHL), HOT_TEMP_HYSTERESIS_LIMIT (HTHT_HYST), OS_TEMP_HIGH_LIMIT (TOS) and OS_TEMP_HYSTERESIS_LIMIT (T_{OS}_HYST) having address from 38h−3Bh.

There are three interrupt modes of operation: Default Interrupt, One−Time Interrupt, and Comparator. The OS output of the NCT80 can be programmed for One−Time Interrupt mode and Comparator mode. INT can be programmed for Default Interrupt mode and One−Time Interrupt mode. These modes are explained in the following subsections.

Default Interrupt Mode

In Default Interrupt mode, exceeding HTHL causes an interrupt that remains active indefinitely until reset by reading Interrupt Status Register 1 at address 01h or cleared by the INT_Clear bit in the Configuration Register at address 00h, bit 3. When an interrupt event has occurred by exceeding HTHL, and is then reset, another interrupt occurs again when the next temperature conversion has completed. The interrupts continue to occur in this manner until the temperature falls below HTHL_HYST, at which time the interrupt output automatically clears.

One−Time Interrupt Mode

In One−Time Interrupt mode, exceeding HTHL causes an interrupt that remains active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration Register. When an interrupt event has occurred by exceeding HTHL, and is then reset, an interrupt does not occur again until the temperature falls below HTHL_HYST.

Comparator Mode

In Comparator mode, exceeding T_{OS} causes the OS output to go low (default) and remain low until the temperature falls below T_{OS}_HYST. When the temperature falls below T_{OS}_HYST, OS goes high.

Chassis Intrusion

A chassis intrusion input (pin 7) is provided to detect unauthorised tampering with the equipment.

$\overline{\text{RESET}}$

A $\overline{\text{RESET}}$ input (pin 12) and $\overline{\text{RESET}}$ output (pin 13) is also provided. Pulling the input pin low will reset all the NCT80 internal registers to their default values. This pin must be pulled high in order for the user to be able to configure the device.

The $\overline{\text{RESET}}$ output is at least 10 ms.

ADC Converter

The analog inputs (AIN0−AIN6) are multiplexed into the on−chip successive approximation, analog−digital converter. This has a resolution of 10 bits. The basic input range is zero to 2.56 V.

When the ADC is running, it samples and converts an input every 728 ms, except for the internal temperature. This is converted using a sigma delta ADC.

Fan Monitoring Cycle Time

When a monitoring cycle is started, monitoring of the fan speed inputs begins at the same time as monitoring of the analog inputs. However, the two monitoring cycles are not synchronized in any way. The monitoring cycle time for the fan inputs is dependent on fan speed and is much slower than for the analog inputs. The monitoring cycle time depends on the fan speed and number of tach output pulses per revolution. Two complete periods of the fan tach output (three rising edges) are required for each fan measurement. Therefore, if the start of a fan measurement just misses a rising edge, the measurement can take almost three tach periods. In order to read a valid result from the fan value registers, the total monitoring time allowed after starting the monitoring cycle should, therefore, be three tach periods of TACH1 plus three tach periods of TACH2 at the lowest normal fan speed.

Fan Inputs

Pins 4 and 5 are fan speed inputs. Signal conditioning in the NCT80 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to VCC. In the event that these inputs are supplied from fan outputs that exceed 0 V to 6.5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range. Figure 10 to Figure 13 show circuits for most common fan tach outputs. If the fan tach output has a resistive pull−up to VCC it can be directly connected to the fan input, as shown in Figure 10.

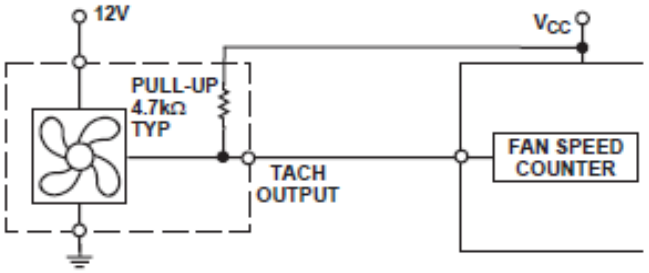


Figure 10. Fan with Tach. Pull−Up to +VCC

If the fan output has a resistive pull−up to 12 V (or other voltage greater than 6.5 V), the fan output can be clamped with a zener diode, as shown in Figure 11. The zener voltage should be chosen so it is greater than VIH but less than 6.5 V, allowing for the voltage tolerance of the zener. A value of between 3 V and 5 V is suitable.

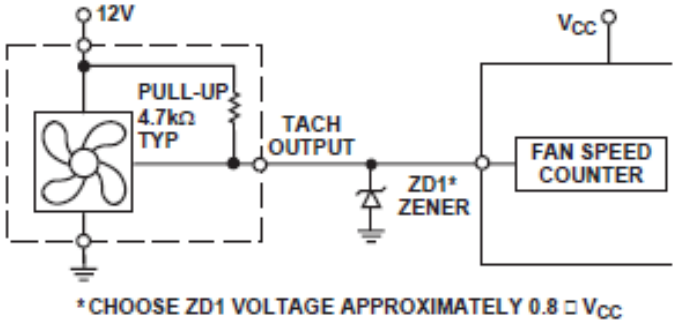


Figure 11. Fan with Tach. Pull−Up to Voltage >6.5 V

If the fan has a strong pull−up (less than 1 kΩ) to 12 V, or a totem−pole output, then a series resistor can be added to limit the zener current, as shown in Figure 12. Alternatively, a resistive attenuator may be used, as shown in Figure 13. R1 and R2 should be chosen such that:

$$2\ V < V_{pull-up} \times \frac{R_2}{\left(R_{pull-up} + R_1 + R_2\right)} < 5\ V$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, so this should be taken into account when calculating resistor values. With a pull−up voltage of 12 V and pull−up resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ

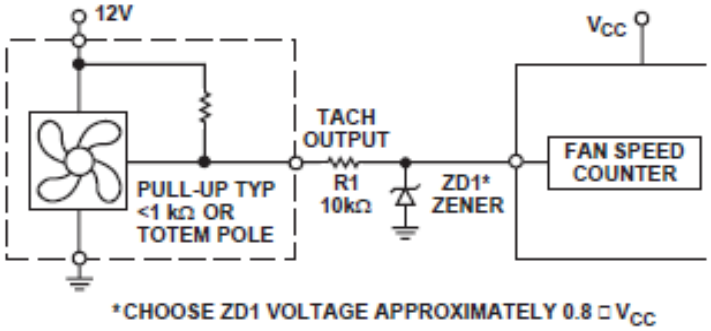


Figure 12. Fan with Strong Tach. Pull−Up to >VCC or Totem−Pole Output, Clamped with Zener and Resistor

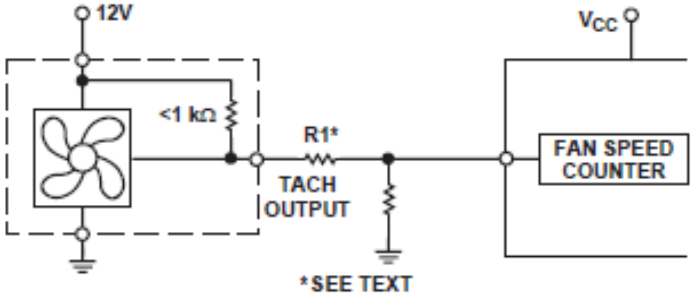


Figure 13. Fan with Strong Tach. Pull−Up to >VCC or Totem−Pole Output, Attenuated with R1/R2

Fan Speed Measurement

The fan counter does not count the fan tach output pulses directly, because the fan speed may be less than 1000 rpm and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on−chip 22.5 kHz oscillator into the input of an 8−bit counter for two periods of the fan tach output, as shown in Figure 14; the accumulated count is actually proportional to the fan tach period and inversely proportional to the fan speed.

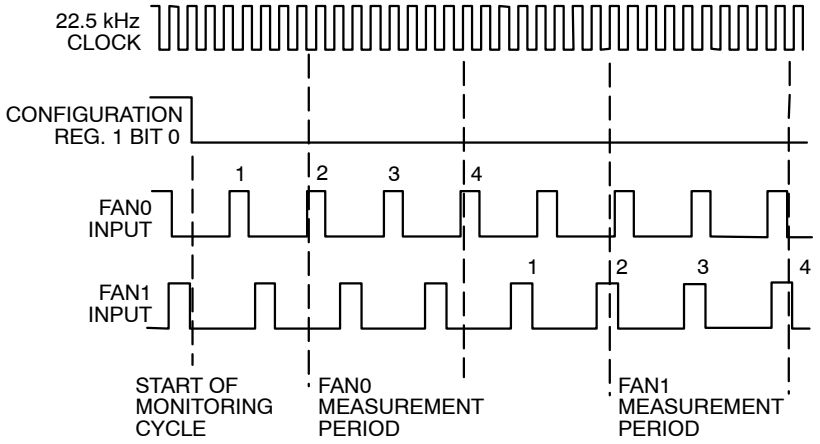


Figure 14. Fan Speed Measurement

The measurement begins on the rising edge of a fan tach pulse, and ends on the next−but−one rising edge. The fans are monitored sequentially, so if only one fan is monitored the monitoring time is the time taken after the Start Bit for it to produce two complete tach cycles or for the counter to reach full scale, whichever occurs sooner. If more than one fan is monitored, the monitoring time depends on the speed of the fans and the timing relationship of their tach pulses. This is illustrated in Figure 14. Once the fan speeds have been measured, they will be stored in the Fan Speed Value Registers and the most recent value can be read at any time. The measurements will be updated as long as the monitoring cycle continues. To accommodate fans of different speed and/or different numbers of output pulses per revolution, a prescaler (divisor) of 1, 2, 4, or 8 may be added before the counter. The default value is 2, which gives a count of 153 for a fan running at 4400 rpm producing two output pulses per revolution. The count (stored in the TACH registers) is calculated by the equation:

$$\text{Count} = \frac{(22.5 \times 10^3 \times 60)}{(\text{rpm} \times \text{Divisor})}$$

$22.5\text{x}10^3$ = oscillator frequency

Divisor = number of poles in the fan

Fan Limit Values

Fans in general will not over speed if run from the correct voltage, so the failure condition of interest is under speed due to electrical or mechanical failure. For this reason only, low−speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement *exceeds* the limit value.

Table 9. REGISTER MAP

Register Name	Type	Reset Value	Address Offset
CONFIGURATIONREGISTER	RW	0x08	0x00
STATUSREGISTER1	RO	0x00	0x01
STATUSREGISTER2	RO	0x00	0x02
MASKREGISTER1	RW	0x00	0x03
MASKREGISTER2	RW	0x00	0x04
FAN_DIVISOR_OUTPUT_PIN_CONFIG	RW	0x14	0x05
OS_CONFIG_TEMP_RESOLUTION	RW	0x01	0x06
CONVERSION_RATE	RW	0x00	0x07
CHANNEL_SELECT_REGISTER	RW	0x00	0x08
CONVERSION_RATE	RW	0x00	0x09
IN0_READING	RO	0x0000	0x20
IN1_READING	RO	0x0000	0x21
IN2_READING	RO	0x0000	0x22
IN3_READING	RO	0x0000	0x23
IN4_READING	RO	0x0000	0x24
IN5_READING	RO	0x0000	0x25
IN6_READING	RO	0x0000	0x26
TEMP_READING	RO	0x0000	0x27
TACH1_READING	RO	0x00	0x28
TACH2_READING	RO	0x00	0x29
IN0_HIGH_LIMIT	RW	0x00	0x2A
IN0_LOW_LIMIT	RW	0x00	0x2B
IN1_HIGH_LIMIT	RW	0x00	0x2C
IN1_LOW_LIMIT	RW	0x00	0x2D
IN2_HIGH_LIMIT	RW	0x00	0x2E
IN2_LOW_LIMIT	RW	0x00	0x2F
IN3_HIGH_LIMIT	RW	0x00	0x30
IN3_LOW_LIMIT	RW	0x00	0x31
IN4_HIGH_LIMIT	RW	0x00	0x32
IN4_LOW_LIMIT	RW	0x00	0x33
IN5_HIGH_LIMIT	RW	0x00	0x34
IN5_LOW_LIMIT	RW	0x00	0x35
IN6_HIGH_LIMIT	RW	0x00	0x36
IN6_LOW_LIMIT	RW	0x00	0x37
HOT_TEMP_HIGH_LIMIT	RW	0x00	0x38
HOT_TEMP_HYSTERESIS_LIMIT	RW	0x00	0x39
OS_TEMP_HIGH_LIMIT	RW	0x00	0x3A
OS_TEMP_HYSTERESIS_LIMIT	RW	0x00	0x3B
TACH1_COUNT_LIMIT	RW	0x00	0x3C
TACH2_COUNT_LIMIT	RW	0x00	0x3D
MANUFACTURERID	RO	0x1A	0x3E

CONFIGURATIONREGISTER

Register Information				
Description	Allows the user to configure many features of the NCT80 device.			
Offset	0x00			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7	INITIALIZATION	Setting this bit to 1 resets the main user writeable registers to their power on default values.	RW	0
6	GPO	Setting this bit to 1 drives the $\overline{\text{GPO}}$ pin low.	RW	0
5	Chassis_clear	Setting this bit to 1 clears the GPI (chassis intrusion pin). After 10 ms this bit self clears.	RW	0
4	RESET	Setting this bit to 1 outputs at least a 10 ms $\overline{\text{RESET}}$ (active low) pulse on $\overline{\text{RST\_OUT}}$. If bits 7 and 6 of register 0x05 are set to 1 and 0 respectively then this $\overline{\text{RESET}}$ bit is cleared once the pulse is inactive.	RW	0
3	INT_clear	Setting this bit to 1 disables the $\overline{\text{INT}}$ output. This does not affect the Interrupt Status Registers/ The device will stop monitoring temperature and voltage. Monitoring will resume upon the clearing of this bit.	RW	1
2	INT_polarity_select	Setting this bit to 1 selects an active high output while setting it to 0 selects active low output.	RW	0
1	INT_en	Setting this bit to 1 enables the $\overline{\text{INT}}$ output.	RW	0
0	Start	Setting this bit to 1 enables the monitoring of temperature, voltage and fan readings. Setting this bit to 0 disables these monitoring operations and effectively puts the device in shutdown mode.	RW	0

STATUSREGISTER1

Register Information				
Description	Register to indicate if a high or low limit has been exceeded.			
Offset	0x01			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7	INT_IN	The NCT80 sets this bit to 1 if a low has been detected on the $\overline{\text{INT\_IN}}$ pin.	RO	0
6	IN6	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0
5	IN5	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0
4	IN4	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0
3	IN3	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0
2	IN2	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0
1	IN1	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0
0	IN0	The NCT80 sets this bit to 1 if the high or low limit has been exceeded.	RO	0

STATUSREGISTER2

Register Information				
Description		Register to indicate if a high or low limit has been exceeded.		
Offset		0x02		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:6	Reserved		RO	0x0
5	OS_bit	The NCT80 sets this bit to 1 if the temperature exceeds either the high or low $\overline{OS}$ limit. The interrupt mode can be selected in register 0x04 bit 7.	RO	0
4	GPI	The NCT80 sets this bit to 1 if the GPI (chassis intrusion) pin has gone high.	RO	0
3	TACH2	The NCT80 sets this bit to 1 if the fan speed limit has been exceeded.	RO	0
2	TACH1	The NCT80 sets this bit to 1 if the fan speed limit has been exceeded.	RO	0
1	BTI	If this bit is set to 1 then it indicates that an interrupt has occurred on the Board Temperature Input ($\overline{BTI}$) pin.	RO	0
0	Temperature	The NCT80 sets this bit to 1 if the temperature exceeds either the high or low limit. The interrupt mode can be selected in register 0x04 bit 6.	RO	0

MASKREGISTER1

Register Information				
Description		Register to mask out of limit conditions shown in the corresponding status register.		
Offset		0x03		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7	INT_IN	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
6	IN6	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
5	IN5	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
4	IN4	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
3	IN3	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
2	IN2	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
1	IN1	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
0	IN0	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0

MASKREGISTER2

Register Information				
Description	Register to mask out of limit conditions shown in the corresponding status register.			
Offset	0x04			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7	Mode_select_OS_ temp_interrupt	Writing zero to this bit selects the default interrupt mode which gives the user an interrupt if the temperature goes above the $\overline{OS}$ limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the hysteresis limit. Writing a 1 to this bit selects the one time interrupt mode which only gives the user one interrupt when it goes above the $\overline{OS}$ limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature goes below the hysteresis limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the $\overline{OS}$ limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done.	RW	0
6	Mode_select_hot_ temp_interrupt	Writing zero to this bit selects the default interrupt mode which gives the user an interrupt if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the hysteresis limit. Writing a 1 to this bit selects the one time interrupt mode which only gives the user one interrupt when it goes above the hot limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature goes below the hysteresis limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the hot limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done.	RW	0
5	OS_bit	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
4	GPI	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
3	TACH2	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
2	TACH1	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
1	BTI	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0
0	Temperature	Writing a 1 to this bit disables the corresponding status bit for the $\overline{INT}$ output.	RW	0

FAN_DIVISOR_OUTPUT_PIN_CONFIG

Register Information				
Description	This register allows the user to configure the TACH reading modes and also the $\overline{OS}$ and $\overline{RST\_OUT}$ pin configuration.			
Offset	0x05			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7	RST_en	Setting this bit to 1 enables the $\overline{RST\_OUT}$ functionality on the $\overline{RST\_OUT}$ / $\overline{OS}$ output pin. If bits 6 and 7 are set to 0 then this pin is disabled.	RW	0
6	OS_pin_en	Setting this bit to 1 enables the $\overline{OS}$ functionality on the $\overline{RST\_OUT}$ / $\overline{OS}$ output pin. For the $\overline{OS}$ pin to function, bit 7 of this register must be set to 0. If bits 6 and 7 are set to 0 then this pin is disabled.	RW	0
5:4	TACH2_divisor	If level sensitive input is selected setting bit <4> = 1 selects and active−low input (An interrupt will be generated if the TACH2 input is Low), if bit <4> = 0 selects an active−high input (an interrupt will be generated if the TACH2 input is High).	RW	0x1
		0x0: Divide by 1		
		0x1: Divide by 2		
		0x2: Divide by 4		
		0x3: Divide by 8		
3:2	TACH1_divisor	If level sensitive input is selected setting bit <2> = 1 selects and active−low input (An interrupt will be generated if the TACH1 input is Low), if bit <2> = 0 selects an active−high input (an interrupt will be generated if the TACH1 input is High).	RW	0x1
		0x0: Divide by 1		
		0x1: Divide by 2		
		0x2: Divide by 4		
		0x3: Divide by 8		
1	TACH2_mode	Setting this bit to 1 selects the level sensitive input mode. Setting this bit to 0 selects TACH Count Mode for the input pin.	RW	0
0	TACH1_mode	Setting this bit to 1 selects the level sensitive input mode. Setting this bit to 0 selects TACH Count Mode for the input pin.	RW	0

OS_CONFIG_TEMP_RESOLUTION

Register Information				
Description	This register allows the user to configure the $\overline{OS}$ output pin and also the temperature sensor resolution.			
Offset	0x06			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:4	Temp_resolution	Depending of the state of bit 3 in this register these bits are the LSBs of the temperature measurement. If 8 bit resolution is selected then bit 7 only is the LSB of the temperature reading. If 11 bit resolution is selected then bits 7−4 are the LSBs of the temperature data (bit 7 being the most significant of the 4 bits).	RW	0x0
3	Temp_resolution_ control	Selects either an 8 bit or 11 bit temperature conversion.	RW	0
		0: Selects an 8 bit plus sign temperature conversion.		
		1: Selects an 11 bit plus sign temperature conversion.		
2	OS_mode_select	Selects the mode of operation for the $\overline{OS}$ pin.	RW	0
		0:		
		1:		
1	OS_polarity	Selects the polarity of the open drain $\overline{OS}$ pin.	RW	0
		0: Selects $\overline{OS}$ to be active low.		
		1: Selects $\overline{OS}$ to be active high.		
0	OS_status	This read only bit mirrors the state of the $\overline{RST\_OUT}/\overline{OS}$ pin when the $\overline{OS}$ pin is enabled.	RO	1

CONVERSION_RATE

Register Information				
Description	Register to control the conversion rate of the ADC input channels.			
Offset	0x07			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:1	Reserved		RO	0x00
0	Conv_rate		RW	0
		0: Sets the conversion rate to be ever 728 ms (typical).		
		1: Sets the NCT80 to operate in continuous conversion mode.		

CHANNEL_SELECT_REGISTER

Register Information					
Description		Allows the user to manually add/remove measurement channels from the ADC round robin loop.			
Offset		0x08			
Bitfield Details					
Field	**Name**	**Description**		**Access**	**Default**
7	Temp			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
6	IN6			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
5	IN5			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
4	IN4			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
3	IN3			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
2	IN2			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
1	IN1			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		
0	IN0			RW	0
		0:	This channel is included in the conversion loop.		
		1:	This channel is disabled and conversions are skipped. Value register will return 0 and it will not cause an interrupt to be generated.		

CONVERSION_RATE_PROGRAMMING

Register Information					
Description	Register to add further programmability to the conversion rate of the ADC input channels. Note Any non−zero value in this register over−rides setting as controlled from register 07h				
Offset	0x09				
Bitfield Details					
Field	**Name**	**Description**		**Access**	**Default**
7:3	Reserved			RO	0x00
2:0	Conv_rate	0x00	Use Conversion rate as setup from register 0x07 bit 0	RW	0x0
		0x01	Conversion rate = 1.2 ms		
		0x02	Conversion rate = 4.8 ms		
		0x03	Conversion rate = 9.6 ms		
		0x04	Conversion rate = 38 ms		
		0x05	Conversion rate = 77 ms		
		0x06	Conversion rate = 154 ms		
		0x07	Conversion rate = 614 ms		

IN0_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x20			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN0_Data		RO	0x0000

IN1_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x21			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN1_Data		RO	0x0000

IN2_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x22			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN2_Data		RO	0x0000

IN3_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x23			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN3_Data		RO	0x0000

IN4_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x24			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN4_Data		RO	0x0000

IN5_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x25			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN5_Data		RO	0x0000

IN6_READING

Register Information				
Description	This register stores the data returned on this input channel			
Offset	0x26			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:6	IN6_Data		RO	0x0000

TEMP_READING

Register Information				
Description	This register stores the data returned on the temperature channel			
Offset	0x27			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
15:4	Temp_Data		RO	0x0000

TACH1_READING

Register Information				
Description	This register stores the number of counts on the TACH1 input pin.			
Offset	0x28			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	TACH1_Data		RO	0x00

TACH2_READING

Register Information				
Description	This register stores the number of counts on the TACH2 input pin.			
Offset	0x29			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	TACH2_Data		RO	0x00

IN0_HIGH_LIMIT

Register Information				
Description	High limit register.			
Offset	0x2A			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN0_LOW_LIMIT

Register Information				
Description	Low limit register.			
Offset	0x2B			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

IN1_HIGH_LIMIT

Register Information				
Description	High limit register.			
Offset	0x2C			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN1_ LOW _LIMIT

Register Information				
Description		Low limit register.	Low limit register.	
Offset		0x2D	0x2D	
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

IN2_HIGH_LIMIT

Register Information				
Description		High limit register.		
Offset		0x2E		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN2_LOW_LIMIT

Register Information				
Description		Low limit register.		
Offset		0x2F		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

IN3_HIGH_LIMIT

Register Information				
Description		High limit register.		
Offset		0x30		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN3_LOW_LIMIT

Register Information				
Description		Low limit register.		
Offset		0x31		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

IN4_HIGH_LIMIT

Register Information				
Description		High limit register.		
Offset		0x32		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN4_LOW_LIMIT

Register Information				
Description		Low limit register.		
Offset		0x33		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

IN5_HIGH_LIMIT

Register Information				
Description		High limit register.		
Offset		0x34		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN5_LOW_LIMIT

Register Information				
Description		Low limit register.		
Offset		0x35		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

IN6_HIGH_LIMIT

Register Information				
Description		High limit register.		
Offset		0x36		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HIGH_LIMIT		RW	0x00

IN6_LOW_LIMIT

Register Information				
Description		Low limit register.		
Offset		0x37		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	LOW_LIMIT		RW	0x00

HOT_TEMP_HIGH_LIMIT

Register Information				
Description		Hot temperature limit		
Offset		0x38		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HOT_TEMP_HIGH_LIMIT		RW	0x55

HOT_TEMP_HYSTERESIS_LIMIT

Register Information				
Description		Hysteresis Temperature Limit (low)		
Offset		0x39		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HOT_TEMP_HYSTERESIS_LIMIT		RW	0x4B

OS_TEMP_HIGH_LIMIT

Register Information				
Description		Hot temperature limit		
Offset		0x3A		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HOT_TEMP_HIGH_LIMIT		RW	0x55

OS_TEMP_HYSTERESIS_LIMIT

Register Information				
Description		Hysteresis Temperature Limit (low)		
Offset		0x3B		
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	HOT_TEMP_HYSTERESIS_LIMIT		RW	0x4B

TACH1_COUNT_LIMIT

Register Information				
Description	TACH1 speed limit.			
Offset	0x3C			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	TACH1_COUNT_LIMIT		RW	0xFF

TACH2_COUNT_LIMIT

Register Information				
Description	TACH2 speed limit.			
Offset	0x3D			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	TACH2_COUNT_LIMIT		RW	0xFF

MANUFACTURERID

Register Information				
Description	Manufacturer ID register. 0x1A for ON Semiconductor.			
Offset	0x3E			
Bitfield Details				
Field	**Name**	**Description**	**Access**	**Default**
7:0	MANUFACTURER ID		RO	0x1A

Serial Bus Interface

Control of the NCT80 is carried out via the I^{2}C bus. The NCT80 is connected to this bus as a slave device, under the control of a master device. The NCT80 has a 7−bit serial bus address. The upper 4 bits of the device address are 0101. The lower 3 bits are set by pins 22, 23 and 24. Table 10 shows the 7−bit address for each of the pin states. The address pins are sampled continuously, so any changes made while power is on will result in the device address changing.

Table 10. I^{2}C ADDRESS OPTIONS

A2	A1	A0	Address
0	0	0	0x28
0	0	1	0x29
0	1	0	0x2A
0	1	1	0x2B
1	0	0	0x2C
1	0	1	0x2D
1	1	0	0x2E
1	1	1	0x2F

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high−to−low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7−bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low−to−high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. In the case of the NCT80, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions. To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, and then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register. This is illustrated in Figure 20. The device address is sent over the bus followed by R/W set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the NCT80's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the NCT80 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in Figure 16. A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data byte read from the data register. This is shown in Figure 18.
2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so Figure 16 can be omitted.

To read from a register it is necessary to first write the register address to the address pointer. The Byte Write protocol is used for this.

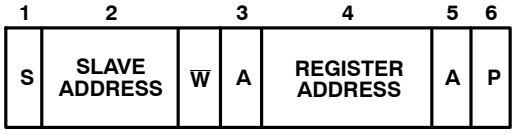


Figure 15. Byte Write Protocol

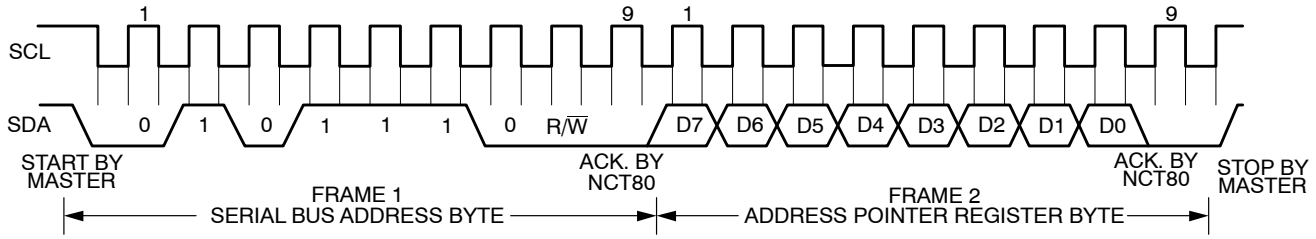


Figure 16. Writing to the Address Pointer

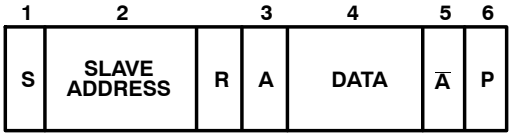


Figure 17. Read Byte Protocol

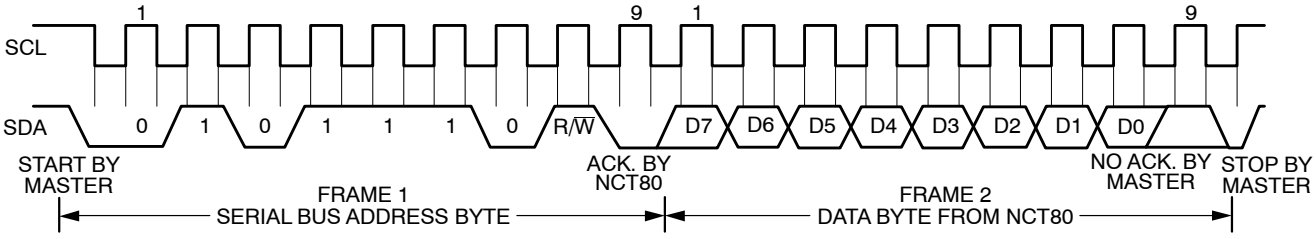


Figure 18. Reading a Byte from the NCT80

To write a byte to a particular register the following 3−byte sequence is used. The first byte is the 7−bit device address plus the Write bit. The second byte is the register address to be written to and the third byte is the data to be written.

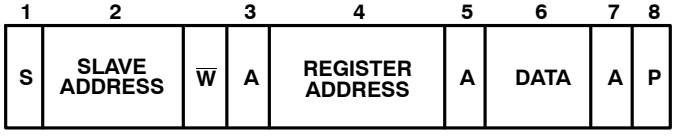


Figure 19. Write a Byte to a Register

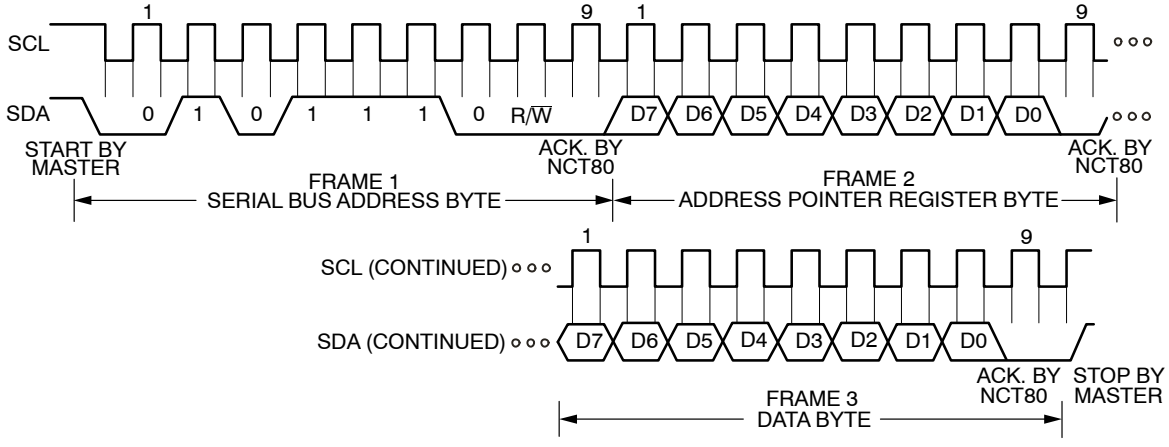
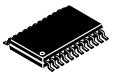


Figure 20. Writing a Byte to a Specified Address

ON Semiconductor is licensed by Philips Corporation to carry the I^2C Bus Protocol.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

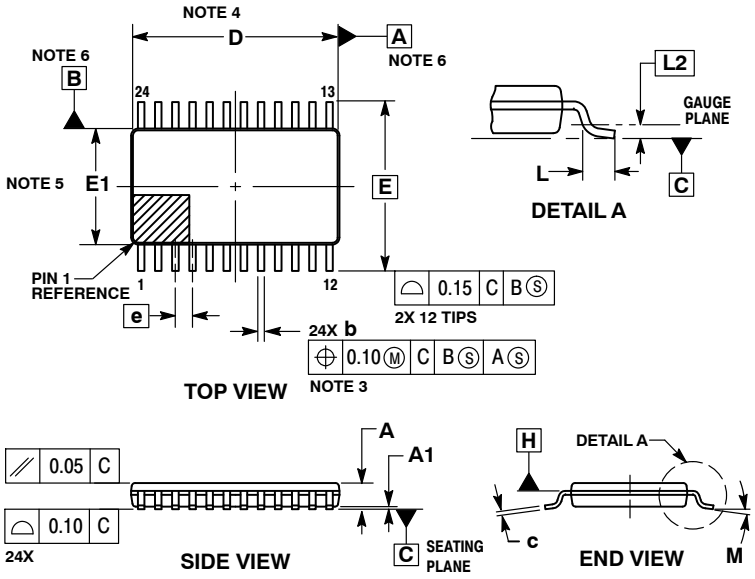
ON Semiconductor®



SCALE 1:1

TSSOP24 7.8x4.4, 0.65P
CASE 948H
ISSUE B

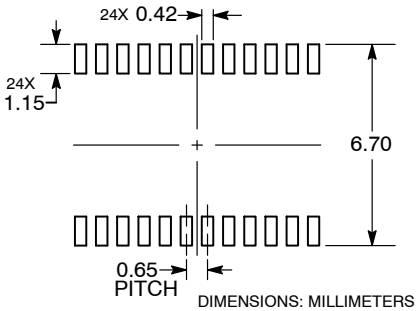
DATE 21 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

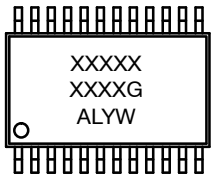
	MILLIMETERS	
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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