

*i*Coupler **EVAL-ADuM5211EBZ**, 150 mW *iso*Power Evaluation Board

FEATURES

*iso*Power integrated, isolated dc-to-dc converter
 Regulated 3.15 V or 5.25 V output
 Up to 150 mW output power
 20-lead SSOP package with 5 mm creepage
 High temperature operation: 105°C
 High common-mode transient immunity: >25 kV/μs

SUPPORTED *i*Coupler® MODELS

[ADuM5210](#)
[ADuM5211](#)
[ADuM5212](#)
[ADuM6210](#)
[ADuM6211](#)
[ADuM6212](#)

GENERAL DESCRIPTION

The [EVAL-ADuM5211EBZ](#) supports the [ADuM5210/ADuM5211/ADuM5212](#) and [ADuM6210/ADuM6211/ADuM6212](#) 150 mW isolated power modules. It provides a JEDEC standard SSOP20 pad layout as well as support for setting the desired output voltage, setting enable control and providing multiple positions for on-board loads and bypass capacitors.

*iso*Power devices employ high frequency, high power switching circuits to enable power transfer across chip scale, air core transformers. The evaluation board includes EMI mitigation recommendations from the [AN-0971 Application Note](#). With the included techniques, this PCB and power module is capable of meeting the requirements of CISPER22 Class A or Class B depending on the voltage and load range.

Complete specifications for the [ADuM5210/ADuM5211/ADuM5212](#) and [ADuM6210/ADuM6211/ADuM6212](#) are provided in the [ADuM5210/ADuM5211/ADuM5212](#) and [ADuM6210/ADuM6211/ADuM6212](#) data sheets, available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD

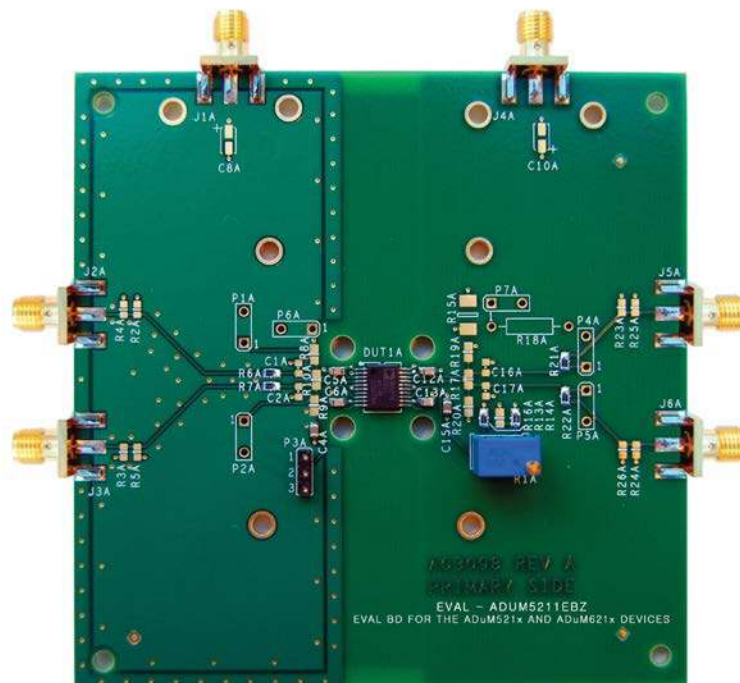


Figure 1. [EVAL-ADuM5211EBZ](#) Evaluation Board

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REVISION HISTORY

1/13—Revision 0: Initial Version

PCB EVALUATION GOALS

This board is intended to achieve three goals.

- It will allow a user of the [ADuM5210/ADuM5211/ADuM5212](#) or [ADuM6210/ADuM6211/ADuM6212](#) to exercise the functional capabilities of the power converter. These include evaluation of bypass, loading, power supply enable/disable control, and setting the adjustable output voltage level.
- All data channel configurations of the entire family can be exercised.
- This evaluation board demonstrates the EMI mitigation techniques required to make a low emissions design as set out in the [AN-0971 Application Note](#).

The [ADuM5210/ADuM5211/ADuM5212](#) and [ADuM6210/ADuM6211/ADuM6212](#) have a pin layout that is compatible with the [ADuM5010](#) and [ADuM6010](#). These two additional devices do not include data channels and consist of the *isoPower* module only. One PCB design supports all four families of parts. Many of the structures on the PCB that support the digital channels are not used for the [ADuM5010](#) and [ADuM6010](#) version of the PCB.

CONNECTORS

This evaluation system is used to examine a variety of different aspects of performance. Connections to power and instrumentation are critical to performing accurate measurements without creating artificial ringing, reflections, ripple, and EMI.

Two types of interconnect are provided: SMA edge connectors and through-hole signal ground pairs. Between these two options, both temporary and permanent connections to the board can easily be made. When coax connections are desired, SMA connectors are available for the V_{DDP} power input and V_{ISO} output as well as all four data I/O pins. These connectors were chosen because they are low profile and provide excellent mechanical connections to the PCB. Most lab equipment is geared toward use of BNC connectors, so adaptors will be required to use the on board connectors.

Power can be directly wired to the PCB via the P6A and P7A through-hole connectors. These provide a power ground pair with the power on the Pin 1 hole. These through holes are on 200mil centers, which match the pin spacing required for Tektronix active probes. These positions can be used for scope test points or direct wiring of power and ground.

In many cases, the data inputs will be derived from function generators through 50 Ω coax cables. The PCB includes positions to install termination resistors to ground near each connector. Two surface-mount pads are provided so that two 100 Ω resistors can be placed in parallel to create a 50 Ω termination with sufficient power dissipation capability to support a 5 V data stream.

PART CONFIGURATION STRUCTURES

The [ADuM5210/ADuM5211/ADuM5212](#) and [ADuM6210/ADuM6211/ADuM6212](#) have pins that must have set inputs for the IC to operate properly. The evaluation board allows all parts a full range of configuration options. On the primary side, the PDIS pin must either be tied low to enable the converter, or pulled high to disable the output power and put the part in a standby state. Connector P3A allows a jumper to be placed between Pin 1 and Pin 2 to disable the converter, or between Pin 2 and Pin 3 to enable the converter. The header can be removed if an external logic source controls the disable function and the signal can be fed directly into Position 2 of the header.

Control of the V_{ISO} voltage is accomplished through a voltage divider that's center node is attached to the V_{SEL} pin as shown in Figure 3. There are two options for setting the output voltage supported on this evaluation board. A 20 k Ω potentiometer is installed at R1A in series with a 16.5 k Ω resistor at Position R16A making a variable resistance to V_{ISO} of 16.5 k Ω to 36 k Ω . A 10 k Ω resistor to ground at Position R14A forms the lower leg of the voltage divider. This will give a range of adjustment of $V_{ISO} < 3.3$ V to > 5.0 V.

Alternatively, if a fixed output voltage is desired, R16A can be removed and a resistor can be installed in R13A that combined with the existing 10 k Ω resistance in R14A will form a fixed voltage divider to set V_{ISO} to a single voltage. Refer to the [ADuM5210/ADuM5211/ADuM5212](#) and [ADuM6210/ADuM6211/ADuM6212](#) data sheets for a selection of resistor values.

BYPASS ON THE PCB

Several positions and structures are provided to allow optimum bypass of the evaluation board. Provisions have been made for optional surface-mount bulk capacitors to be installed near the power connectors to compensate for long cables to the power supply or external load. Parallel bypass capacitors are installed near the [ADuM5210/ADuM5211/ADuM5212](#) or [ADuM6210/ADuM6211/ADuM6212](#) consisting of a 0.1 μ F and a 10 μ F capacitor for V_{DDP} and V_{ISO} . The 0.1 μ F capacitors can be moved to positions on the back side of the board if required.

The PCB also implements distributed capacitive bypass on the primary side of the PCB. This consists of power and ground fills on the top and bottom layers of the PCB on the V_{DDP} side of the board. This is one of the techniques discussed in the EMI Mitigation section. It has the extra benefit of providing added bypass on the primary side of the converter where the largest currents flow as well as RF shielding.

PROVISION FOR LOADING

V_{ISO} can be loaded three ways:

- An external load can be connected via the SMA connector.
- A fixed resistor can be installed at R18A.
- A surface-mount resistor can be installed at R15A.

DATA I/O

There are two data I/O pins on each side of the board. For example, examining Channel A on Side 1, Figure 3 shows the following structures, starting from each I/O connector:

- A position for a pull-down resistor or termination to be installed in R2A and R4A.
- A 0 Ω resistor at R6A connects the trace to the SMA connector and termination. This allows extra trace length and components to be removed when capacitance must be controlled.
- Two positions for connection of the trace to V_{DDP} or GND. R8A and C1A are available for a pull-up or pull-down resistor or for a capacitive load when the I/O is an output.
- There is the P1A test point, with a 200mil pitch. This is for hard wiring inputs or installing a Tektronix active probe header.
- Position R10A allows interconnection of Channel A and Channel B. Inputs on the same side can share a single off board connection, or an output signal can be wrapped back to an input.

The same set of structures is present on each channel, allowing a wide range of tests to be conducted with minimum configuration.

EMI MITIGATION

The PCB implements EMI mitigation techniques discussed in the [AN-0971 Application Note](#) to demonstrate the recommended board layout options for this device. These techniques include stitching capacitance and edge guarding.

Stitching Capacitance

Capacitance between the primary and secondary power and ground planes is the most effective way to reduce high frequency emissions from an *isoPower* device. Figure 2 shows how the inner layers of a PCB can create this stitching capacitance by overlapping inner layer metal to create an extremely low inductance capacitance. The green area shows the active coupling area.

Edge Guarding

Providing guard rings laced together with vias on each layer of the primary side reduces edge emissions from the PCB stack-up. This addresses emissions due to differential currents flowing in the ground planes from reaching the edge of the PCB where they could radiate. Figure 4 shows the top layer guard ring and the bottom layer ground fill as well as the regularly spaced vias in the guard ring that creates a cage type structure to reflect inter-plane emissions back into the PCB. Figure 5 shows the top layer power fill along with its vias to the Layer 3 power plane. This top layer power fill adds distributed capacitance as well as shielding for the layer below.

HIGH VOLTAGE TESTING

This PCB is designed in line with 2500 V basic insulation practices. High voltage testing beyond 2500 V is not recommended. Appropriate care must be taken when using this evaluation board at high voltages, and it should not be relied on for safety functions because it has not been hi-pot tested or certified for safety.

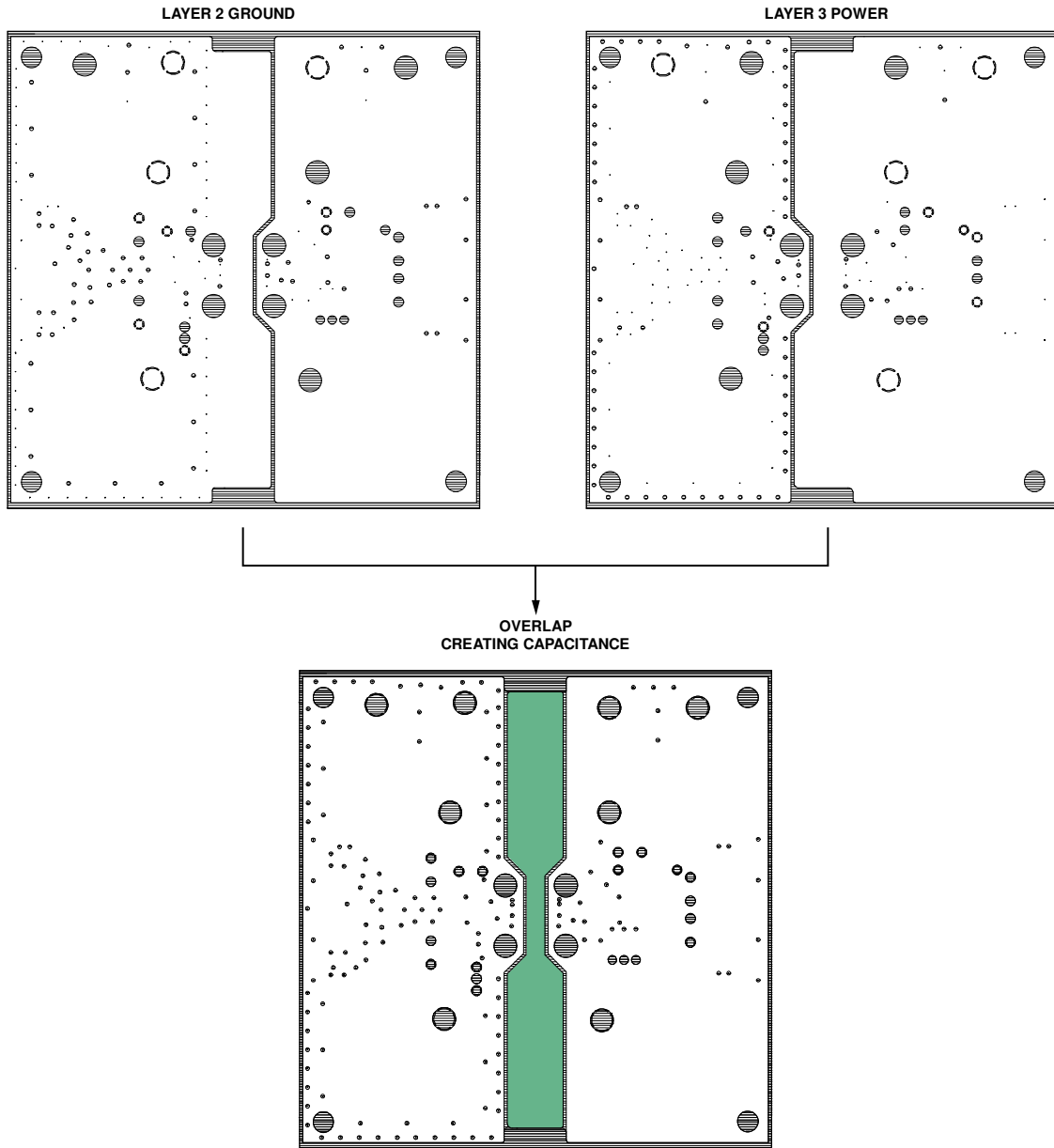


Figure 2. Ground and Power Planes Creating Stitching Capacitance

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EVALUATION BOARD SCHEMATICS AND ARTWORK

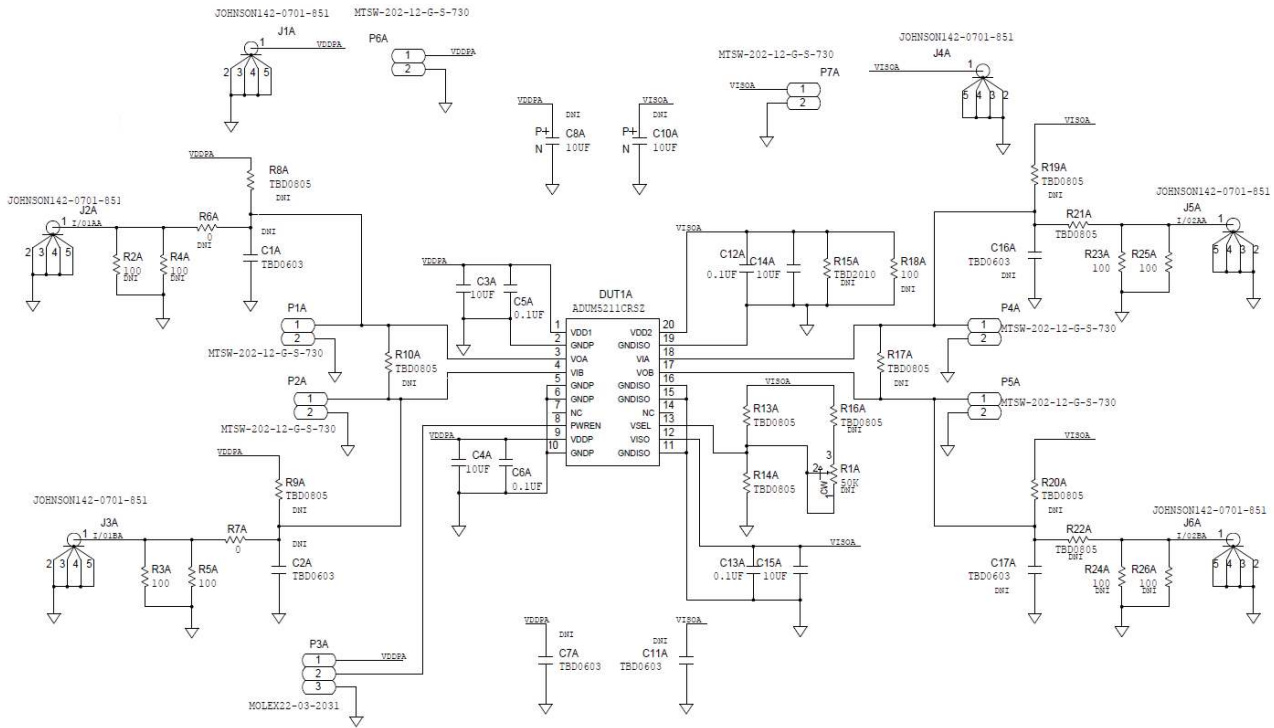
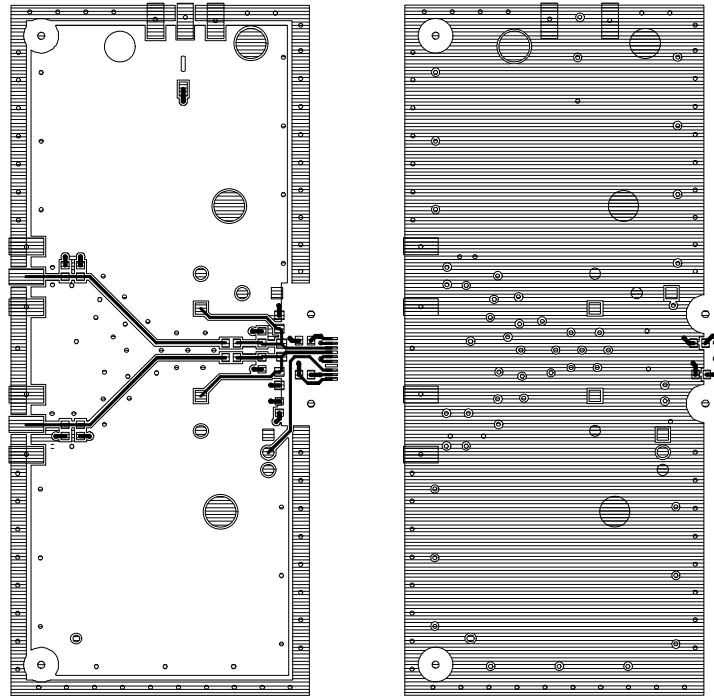


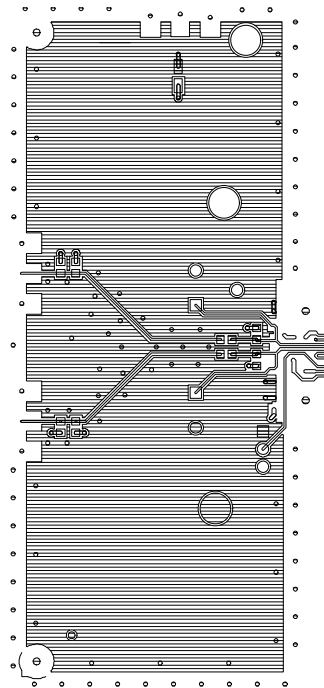
Figure 3. ADuM5210/ADuM5211/ADuM5212 or ADuM6210/ADuM6211/ADuM6212 Schematic

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Figure 4. Edge Guard on Primary Side Top and Bottom Layers



11070-005

Figure 5. Power Fill, Top Layer, Primary Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description
1	DUT1A	ADuM5211
4	C5A, C6A, C12A, C13A	0.1 μ F, 25 V, 10%, 0805
2	C4A, C15A	10 μ F, 6.3 V, 10%, 0805
4	R6A, R7A, R21A, R22A	0.0 Ω 1/16W
1	R14A	10 k Ω , 1/10 W, 1% 0805
1	R16A	16.5 k Ω , 1/10 W, 1%, 0805
1	R1A	20 k Ω resistor VAR 3/8 inch SQ top ADJ
1	P3A	3 pin 100 mil header
6	J1A to J6A	SMA edge connector, Johnson 142-0701-851



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

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