LV8127T

Bi-CMOS LSI

3-phase Bipolar PWM Drive Pre-Driver IC for Brushless Motor Drive

ON Semiconductor®

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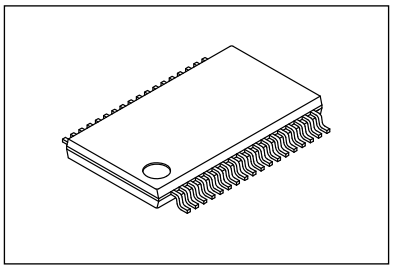
Overview

LV8127T is a three-phase bipolar PWM drive pre-driver IC for N-channel High-side and Low-side FETs. This IC is optimized for low cost, high-efficiency drive circuits in applications that use motors with high drive currents. It offers high supply voltage capability and a high degree of flexibility.



TSSOP36 (275mil)

Feature

- User programmable output current limit
- Built-in protection circuits for Over temperature (OTP), Under Voltage Lock Out (UVLO), Locked rotor (CSD)_and Output Current limit.
- Built-in Forward/Reverse direction control
- Built-in 5V regulator output
- Built-in 15V reference zener diode
- Hall IC input
- E-Brake function

Typical Applications

- Power Tool

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max	V_{CC} terminal	23	V
Supply voltage 2	VM max	VM terminal	190	V
Supply voltage 3	VG max	UH, VH and WH	210	V
DC Output current 1	I_O max1$_{DC}$	UL, VL and WL	50	mA
DC Output current 2	I_O max2$_{DC}$	UOUT, VOUT and WOUT, Source current	50	mA
DC Output current 3	I_O max3$_{DC}$	UOUT, VOUT and WOUT, Sink current	50	mA
RF pin input voltage	V_{RF} max		1	V
LVS pin input voltage	V_{LVS} max	The pins LVS1 and LVS2	V5+0.3	V
IN pin input voltage	V_{IN} max	The pins IN1, IN2 and IN3	V5+0.3	V
HSEL pin input voltage	V_{HSEL} max		V5+0.3	V
F/R pin input voltage	V_{FR} max		V5+0.3	V
EI^+ pin input voltage	V_{EI}+ max		V5+0.3	V
Allowable power dissipation	Pd max	*	1.1	W
Operation temperature	Topr	Ta	–30 to +100	°C
Storage temperature	Tstg		–55 to +150	°C

*When mounted on the specified printed circuit board (114.3 × 76.1 × 1.6mm), Glass epoxy

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}	V_{CC} terminal	12 to 18	V
Supply voltage 2	VM	VM terminal	18 to 185	V
Supply voltage 3	VG	The pins UH, VH and WH	V_{CC}+VM	V
5V constant output current	I_V5	V5 terminal	–30	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, VM = 48V, V_{CC} = 16V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}			4	5.5	mA
5V Regulator (V5 terminal)						
Output voltage	V5REG	I_O = –5mA	4.7	5	5.3	V
Line regulation	ΔV5REG1	V_{CC} = 12 to 20V		15	50	mV
Load regulation	ΔV5REG2	I_O = –5 to –30mA		10	70	mV
Gate Drive Outputs (UFG = VFG = WFG = 0V, UH = VH = WH = 15V when V_{CC} = 16V) *Note1						
Low Side Driver High Side On Resistance	LS_{RonH}	UL, VL and, WL I_{OH} = –10mA		25	35	Ω
Low Side Driver Low Side On Resistance	LS_{RonL}	UL, VL and, WL I_{OL} = 10mA		25	35	Ω
High Side Driver High Side On Resistance	HS_{RonH}	UOUT, VOUT and, WOUT I_{OH} = –10mA		25	35	Ω
High Side Driver Low Side On Resistance	HS_{RonL}	UOUT, VOUT and, WOUT I_{OH} = 10mA		10	15	Ω
High Side dead time1	Tdelay1	UOUT, VOUT and WOUT (see figure #X)	2.9	4	5.1	μS
Low Side dead time2	Tdelay2	UL, VL and WL (see figure #X)	3.4	4.7	6.1	μS
PWM Oscillator (PWM terminal)						
High level output voltage	V_{OH}(PWM)		2.75	3.0	3.25	V
Low level output voltage	V_{OL}(PWM)		1.0	1.1	1.2	V
External capacitor charge current	ICHG	VPWM = 2.1V	–55	–43	–30	μA
Oscillation frequency	f(PWM)	C = 1000pF	15.5	20	24.5	kHz
Amplitude	V(PWM)		1.65	1.9	2.15	Vp-p
Low Voltage Shutdown (LVSD)						
LVS1 threshold voltage	VLVS1		1.8	2.0	2.2	V
LVS2 Hysteresis driver On resistance	VLVS2L	ILVS2 = 5mA		15	30	Ω
Output leakage current	ILVS2leak	VLVS2 = 5V			10	μA
Output Current Control Voltage Input (EI^+ terminal)						
Gain (VEI+/VRF)	GDFSL0	V_{EI}+ < 1.27V(typ)		0		V/V
Gain (VEI+/VRF)	GDFSL1	1.27(typ) < V_{EI}+ < 3V(typ)	0.025	0.03	0.035	Times
Gain (VEI+/VRF)	GDFSL2	3.51(typ) ≥ V_{EI}+ ≥ 3V(typ)	0.08	0.095	0.116	Times
Reference Voltage Clamp	$V_{RF_{max}}$	V_{EI}+ ≥ 3.51V(typ)	90	105	120	mV
Control voltage input range	VSLEI		0		V5	V
Over Temperature Protection (OTP)						
OTP threshold	TSD	Design target value (junction temperature)	150	170		°C
Hysteresis	ΔTSD	Design target value (junction temperature)		30		°C

*Note1:Gate driver output Iopeak=640mA (t<20μ sec duty<7% VCC=16V)

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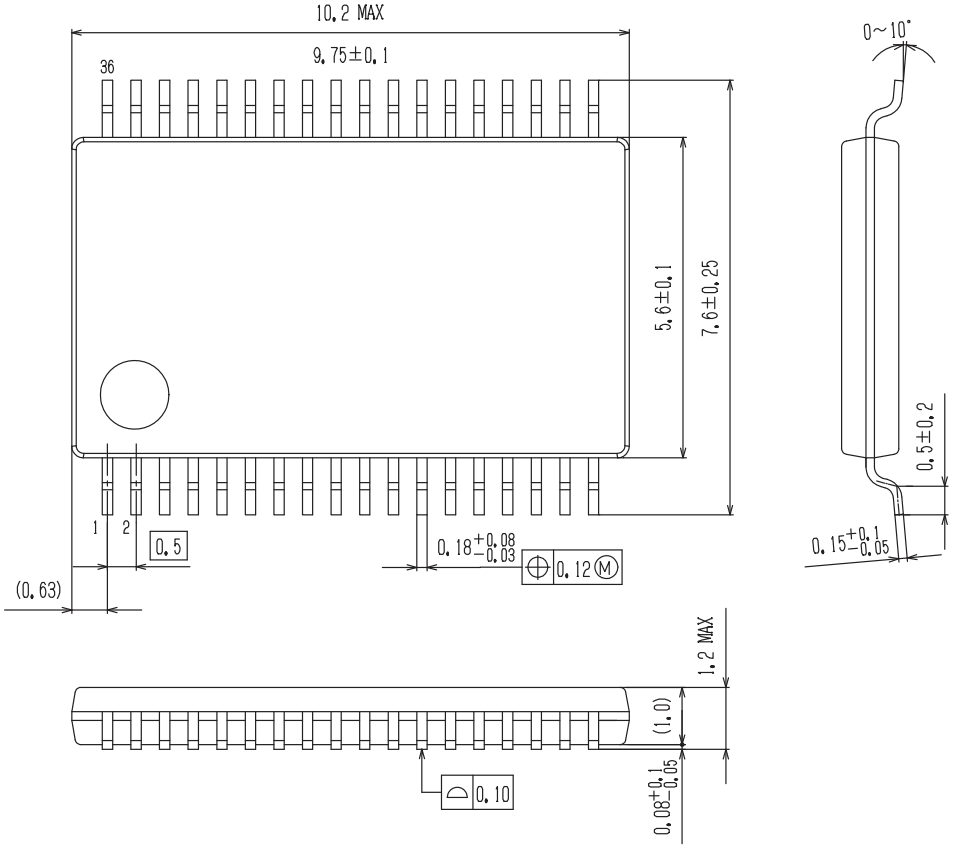
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Locked Rotor Detect Timer Reference Clock (CSD terminal)						
Oscillator High level output voltage	V_{OH}(CSD)		2.25	2.5	2.75	V
Oscillator Low level output voltage	V_{OL}(CSD)		0.85	1.0	1.2	V
External timing capacitor charge current	ICHG1	VCSD = 2.0V	–15	–11	–7	μA
External timing capacitor discharge current	ICHG2	VCSD = 2.0V	7	11	15	μA
Oscillation frequency	f(CSD)	C = 0.01μF	280	360	440	Hz
Oscillator amplitude	V(CSD)		1.3	1.5	1.7	Vp-p
START/BRAKE select input (SB terminal)						
START operation threshold voltage	V_{SBL}		0		2.5	V
BRAKE operation threshold voltage	V_{SBH}		5.0		V_{CC}	V
Hysteresis	ΔVSB		0.15	0.3	0.45	V
Hall Sensor Inputs IN1, IN2 and IN3						
High level input voltage	V_{IH}(IN)		4.0		V5	V
Low level input voltage	V_{IL}(IN)		0		1.0	V
Input open voltage	V_{IO}(IN)		V5–0.5		V5	V
Hysteresis	V_{IS}(IN)		0.8	1.0	1.4	V
High level input current	I_{IH}(IN)	V_{IN} = V5	–10	0	10	μA
Low level input current	I_{IL}(IN)	V_{IN} = 0V	–70	–50	–30	μA
E-Brake Control Input BR terminal						
High level input voltage	V_{IH}(BR)		4.0		V5	V
Low level input voltage	V_{IL}(BR)		0		1.0	V
Input open voltage	V_{IO}(BR)		V5–0.5		V5	V
Hysteresis	V_{IS}(BR)		0.8	1.0	1.4	V
High level input current	I_{IH}(BR)	VBR = V5	–10	0	10	μA
Low level input current	I_{IL}(BR)	VBR = 0V	–70	–50	–30	μA
E-Brake Duty Cycle Adjust BRSET terminal						
Input voltage1	VBRSET1	Output duty 100%	1.0	1.1	1.2	V
Input voltage2	VBRSET2	Output duty 0%	2.75	3.0	3.25	V
Direction Control F/R terminal						
High level input voltage	V_{IH}(FR)		4.0		V5	V
Low level input voltage	V_{IL}(FR)		0		1.0	V
Input open voltage	V_{IO}(FR)		V5–0.5		V5	V
Hysteresis	V_{IS}(FR)		0.8	1.0	1.4	V
High level input current	I_{IH}(FR)	VF/R = V5	–10	0	10	μA
Low level input current	I_{IL}(FR)	VF/R = 0V	–70	–50	–30	μA
Hall Select HSEL terminal – Selects angular spacing of sensors in the target motor						
High level input voltage	V_{IH}(HSL)		4.0		V5	V
Low level input voltage	V_{IL}(HSL)		0		1.0	V
Input open voltage	V_{IO}(HSL)		V5–0.5		V5	V
High level input current	I_{IH}(HSL)	VHSEL = V5	–10	0	10	μA
Low level input current	I_{IL}(HSL)	VHSEL = 0V	–70	–50	–30	μA
15V Reference Zener Diode (V15 terminal)						
Output voltage1	V_V15_1	Io = –100uA	15.8	17.2	18.2	V
Output voltage2	V_V15_2	Io = –1mA	15.8	17.8	19.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

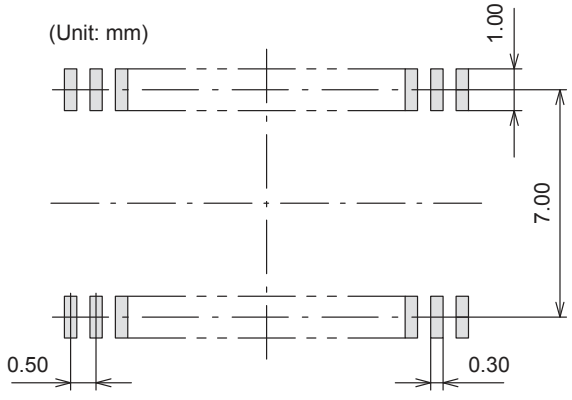
Package Dimensions

unit : mm

TSSOP36 5.6x9.75 / TSSOP36 (275 mil)
CASE 948BC
ISSUE A



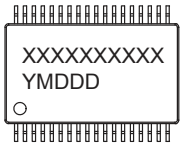
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

Fig.1

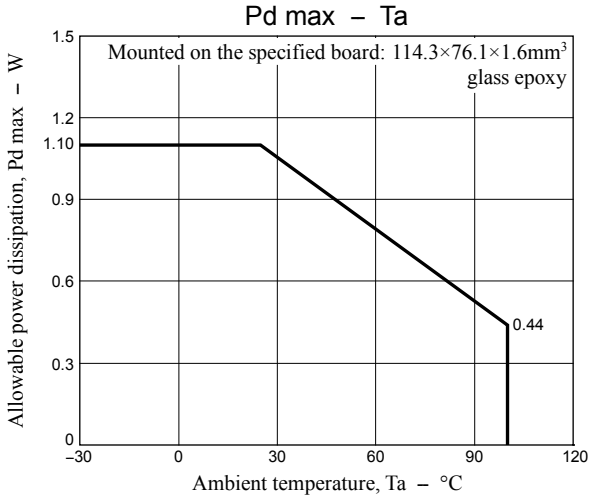
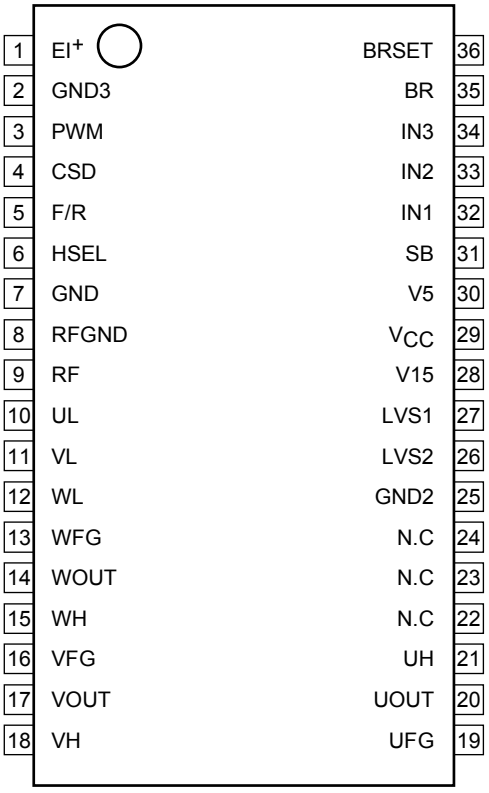


Fig2

Pin Assignment



Top view

Fig.3

Three-phase Logic Truth Table

These tables apply to the position sensor spacing of the motor, either 60 ° or 120°

(1) 120° (HSEL="H")

	F/R="L"			F/R="H"				
	IN1	IN2	IN3	IN1	IN2	IN3	Upper Gate	Lower Gate
1	H	L	H	L	H	L	VOUT	UL
2	H	L	L	L	H	H	WOUT	UL
3	H	H	L	L	L	H	WOUT	VL
4	L	H	L	H	L	H	UOUT	VL
5	L	H	H	H	L	L	UOUT	WL
6	L	L	H	H	H	L	VOUT	WL

(2) 60° (HSEL="L")

	F/R="L"			F/R="H"				
	IN1	IN2	IN3	IN1	IN2	IN3	Upper Gate	Lower Gate
1	H	H	H	L	L	L	VOUT	UL
2	L	H	H	H	L	L	WOUT	UL
3	L	L	H	H	H	L	WOUT	VL
4	L	L	L	H	H	H	UOUT	VL
5	H	L	L	L	H	H	UOUT	WL
6	H	H	L	L	L	H	VOUT	WL

Block Diagram

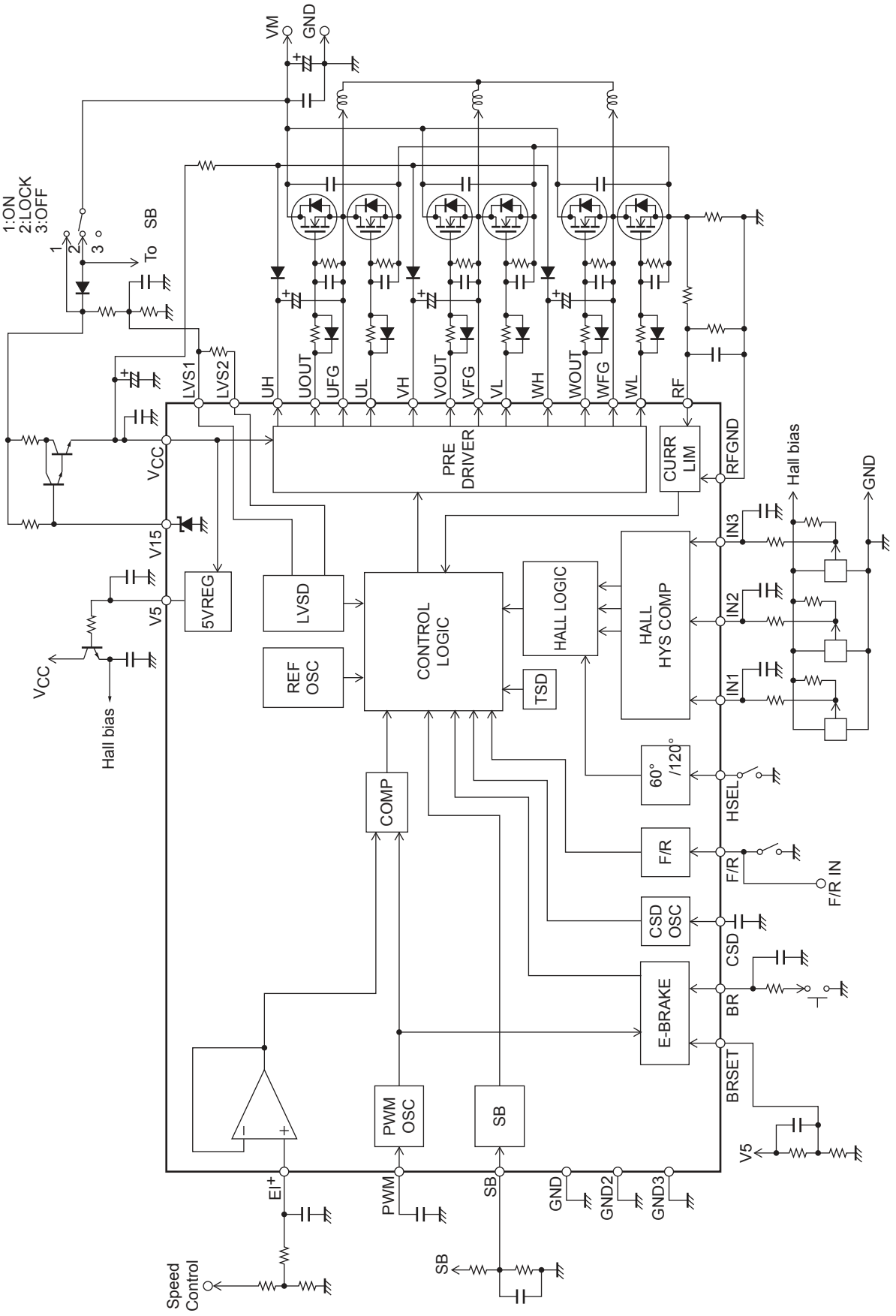
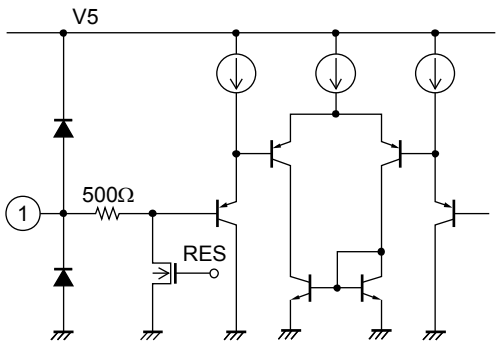
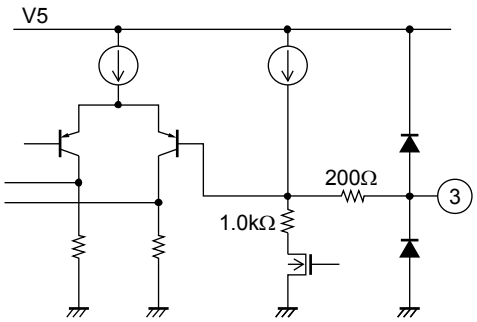
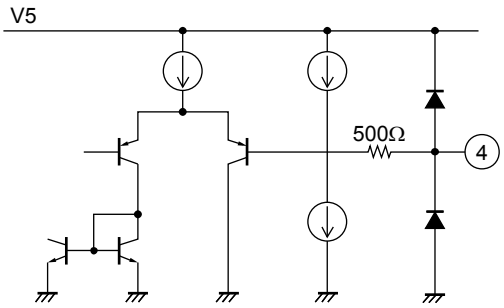
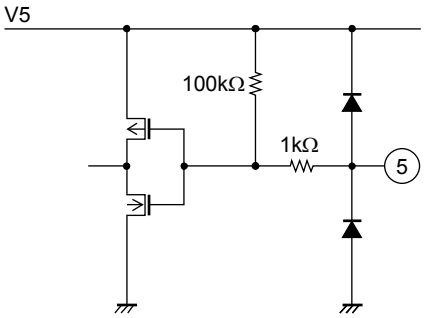
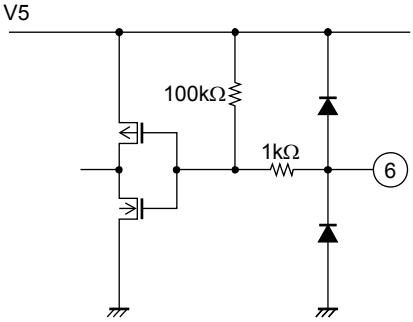


Fig.4

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	EI^+	Integral amplifier non-inverting input pin for voltage control. Used for analog torque control.	
2	GND3	Ground pin	Grounding pin
3	PWM	Set PWM oscillation frequency. Connect a capacitor between this pin and GND.	
4	CSD	Sets the detection time of Locked Rotor protection circuit. Connect a capacitor between this pin and GND.	
5	F/R	Direction (Forward/Reverse) control pin. Forward = 1, Reverse = 0 Internal pull-up resistor	
6	HSEL	Selects the position sensor spacing. (either 120° of 60°) HSEL = "H" for 120° HSEL = "L" for 60° Internal pull-up resistor	
7	GND	Ground pin	Grounding pin

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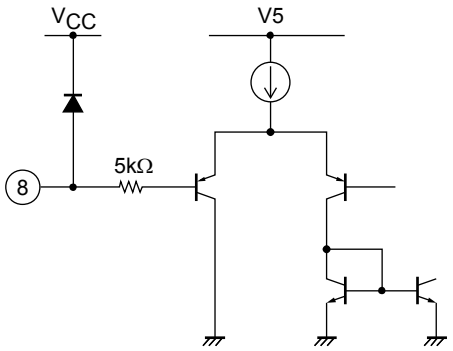
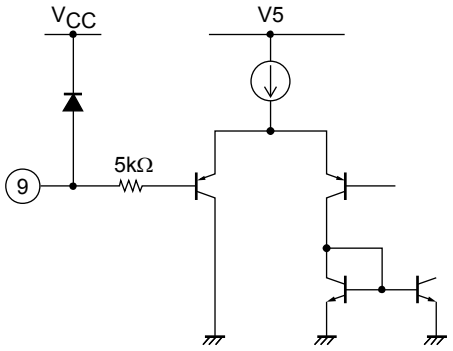
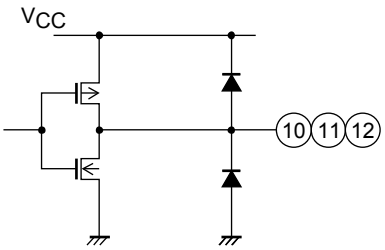
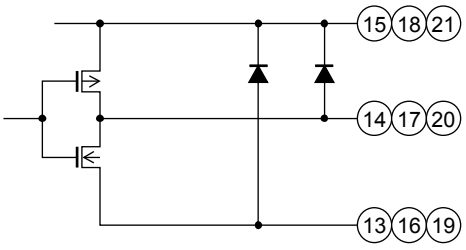
Pin No.	Pin name	Function	Equivalent circuit
8	RFGND	Current sensing Kelvin reference pin. This pin is connected to the GND side of the current sense resistor. This pin should be routed with RF to eliminate voltage drops in the sensing circuit due to PCB trace resistance. A dedicated trace should be used between this pin and the high side of the sense resistor.	
9	RF	Current Sensing Kelvin input pin. This pin is connected to the external current sense resistor and should be routed closely with RFGND to eliminate voltage drops in the sensing circuit due to PCB trace resistance. A dedicated trace should be used between this pin and the high side of the sense resistor.	
10 11 12	VL UL WL	. Low side FET drive pins for the three phases. Duty cycle driven.	
13 16 19	WFG VFG UFG	Motor phase voltage monitor pins. Used by the IC to determine the state of each switch node.	
14 17 20	WOUT VOUT UOUT	High side FET drive pins for the three phases.	
15 18 21	WH VH UH	Drive boost pins for the three phases. Used as the high side gate voltage source. Attached to a simple diode-capacitor boost circuit.	
25	GND2	Ground pin	Ground pin

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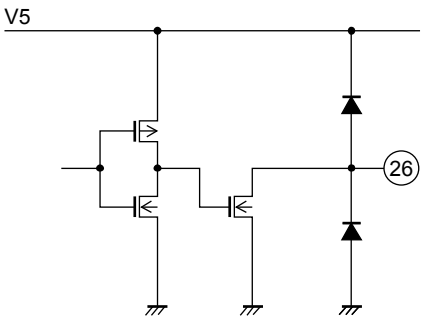
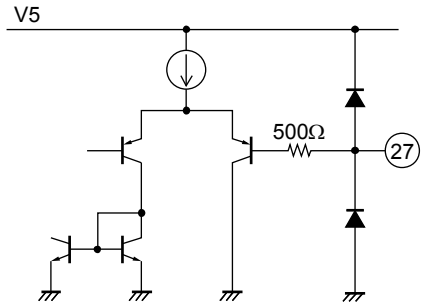
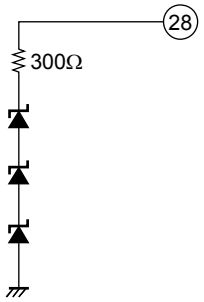
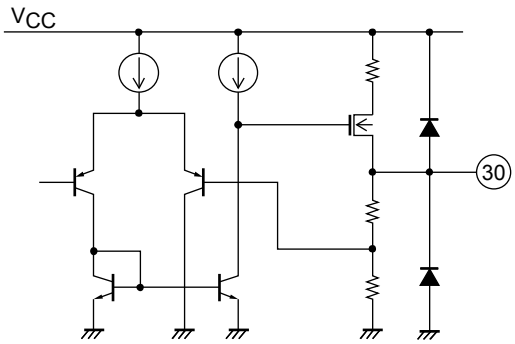
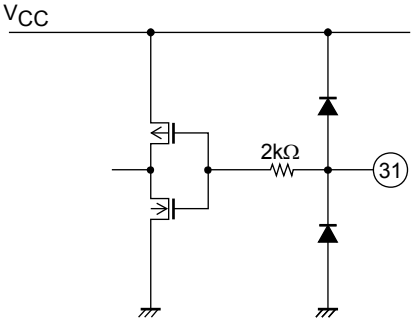
Pin No.	Pin name	Function	Equivalent circuit
26	LVS2	Open drain pull-down to add hysteresis to low supply voltage protection (LVSD) comparator. External resistor value determines hysteresis.	
27	LVS1	Low supply voltage protection (LVSD) comparator input. External resistor divider sets the actual falling edge threshold for low supply voltage protection (LVSD).	
28	VI5	Reference zener diode (15V nominal). Used with an external pull-up as a reference for a 15V BJT emitter follower-based regulator. Typically a diode drop above 15V to allow 15V to appear at the BJT Emitter.	
29	V_{CC}	Power supply pin. Connect a capacitor between this pin and GND for stabilization.	
30	V5	Stabilizing pin for 5V regulator. Connect a capacitor between this pin and GND for stabilization. (about 0.1μF)	
31	SB	Logic Input for Shorted Braking SB = 0V for normal operation. SB >= 5V (nominal)for Shorted Braking assertion	

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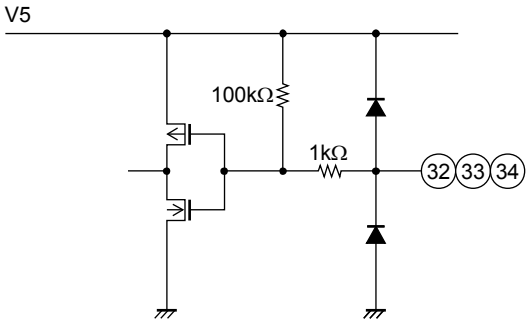
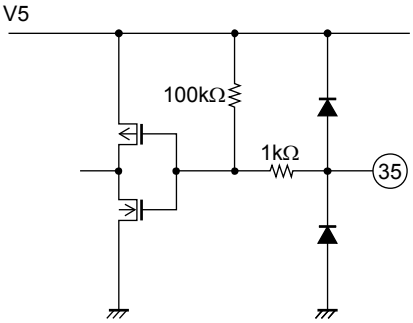
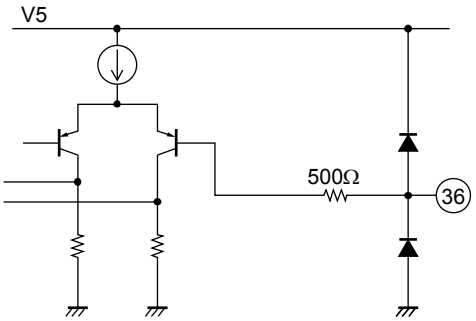
Pin No.	Pin name	Function	Equivalent circuit
32 33 34	IN1 IN2 IN3	Hall input pin Internal pull-up resistor. Connect a capacitor between this pin and GND for signal noise reduction.	
35	BR	Logic input for E-BRAKE control. Internal pull-up resistor. (controls the regenerative brake function) When the BR pin is open (high) then the motor is allowed to rotate without braking. When the BR pin is pulled low, braking is active.	
36	BRSET	Analog control voltage input for E-BRAKE adjustment. Controls the duty cycle of the brake circuit. A lower voltage on BRSET will increase the duty cycle of the brake circuit.	
22 23 24	NC NC NC	The NC pins have no internal connections and can be used for layout purposes.	

Hall input – Drive output Timing Chart (3-phase Hall Input Phase Difference : 120°)

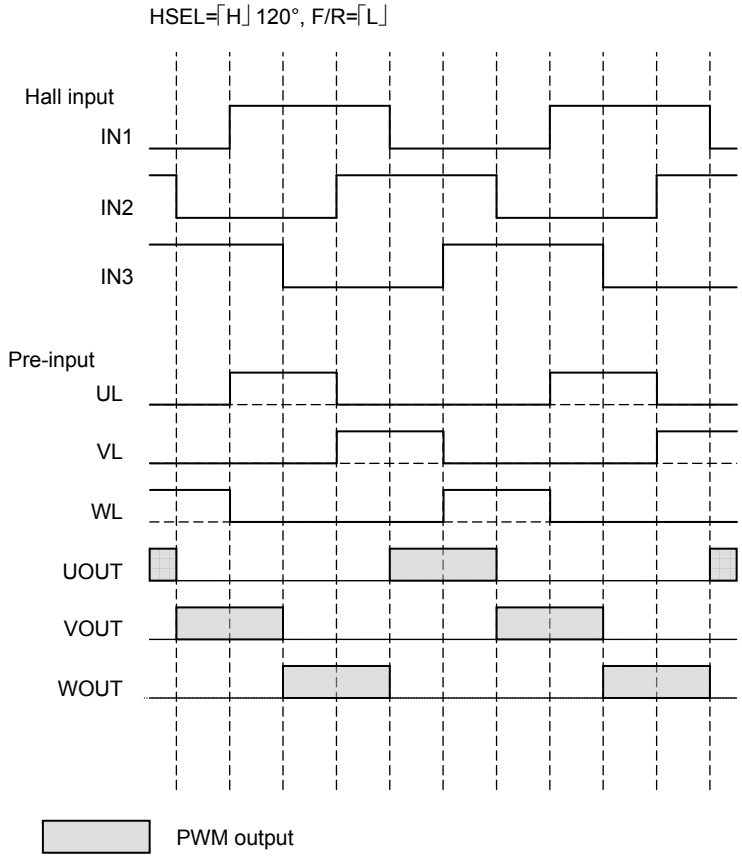


Fig.5

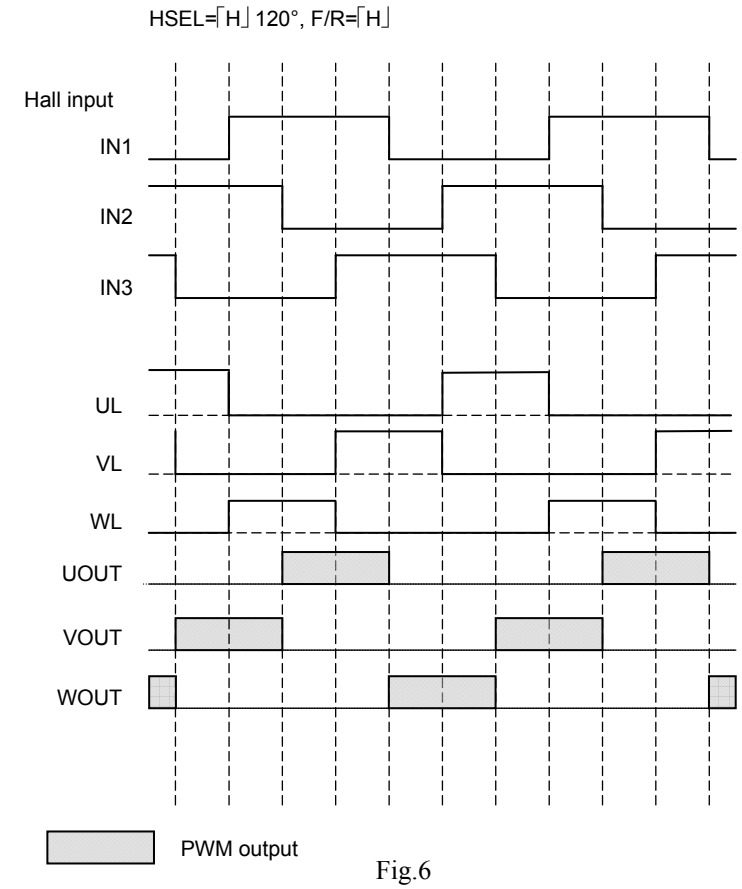


Fig.6

Hall input - Drive output Timing Chart (3-phase Hall Input Phase Difference : 60°)

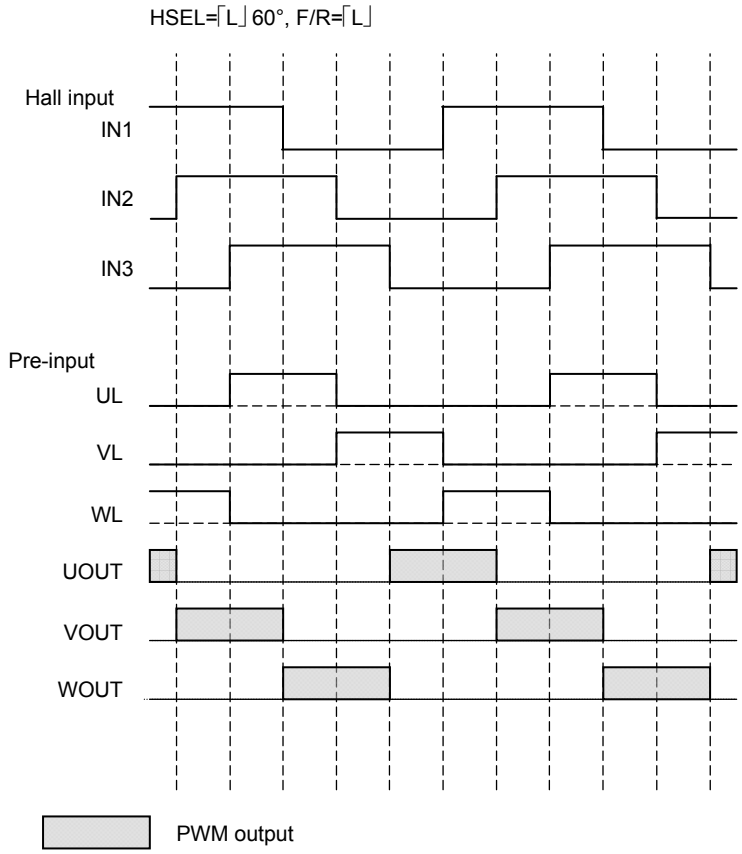


Fig.7

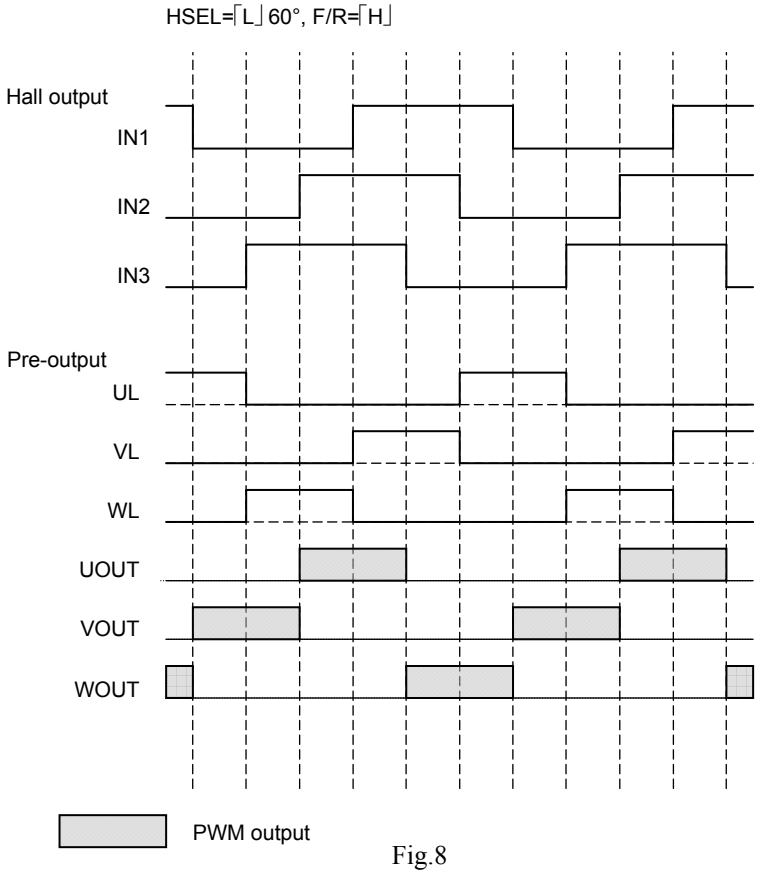


Fig.8

LV8127 Operation

The LV8127T is a self-contained motor driver for three phase Brushless DC (BLDC) motors using external N-Channel FET's for the power driver stage. It supports three half-bridge FET configurations including the upper and lower FET drives for all six FET's. This part controls motor current as a function of the control voltage applied at the input. It has various protection features built in, including Over Temperature (OTP), Locked Rotor(CSD) and Low Voltage Shutdown (LVSD).

Position sensing uses external Hall Effect sensors, either motor mounted or from an external circuit. These sense inputs determine which pair of output drivers should be active, with two bridges active and one inactive for each of three physical segments of rotation. Two sections active will drive a motor in a particular direction and sequencing all three phases will generate continuous rotation. Direction of rotation is accomplished by changing the sequence of the three drive phases.

Effective coil current is controlled with PWM drive of the NFET's in a linear mode for best efficiency. The part has built-in boost circuits for each bridge to generate adequate drive amplitude for upper NFETs.

The PWM reference is a sawtooth wave generated on chip. The PWM frequency can be set with a capacitor on the PWM pin. The PWM duty cycle is determined by the input control voltage at EI+, which is used to set the motor current. The modulator has a piecewise linear variable gain with low gain (0.03V/V) below 3V at EI+ and a higher gain (0.1V/V) as the input voltage exceeds 3V. Above 3.5V the gain is dropped to zero to eliminate any further increase in Duty Cycle.

Motor current is monitored as a small voltage generated across an external resistor in the common H-Bridge lower leg. This voltage is sensed differentially with both leads treated as Kelvin leads and brought inside the LV8127T to an internal amplifier.

PWM output is then generated by combining the PWM reference waveform, the modulation input and the current (error) information to generate a varying duty cycle. This varying width pulse train is applied to the active pair of H-bridges to generate a varying current and thus a rotating flux field to turn the rotor. The strength of the flux field is proportional to the duty cycle.

Two types of braking are supplied. Both would be considered Dynamic Braking, the difference between the two being whether or not regeneration is utilized.

Shorted Braking, also called Motor Plugging, occurs in a motor when the field windings are intentionally shorted such that each coil sees a very low impedance termination. Usually both ends are grounded or shunted with a shorting bar. This produces very high winding currents if the rotor is moving through a magnetic field such as exists in the PM motors in common use. This high current in turn generates a large force in the opposing direction that is manifested as an opposing torque, or braking effect. This type of braking is most effective when the rotor is turning at high speed and least effective at low speeds. This controller generates Shorted Braking action by turning on the lower legs of all three Half Bridges and turning off all upper legs. This 'shorts' all windings to ground and allows high circulating currents in each winding until the rotor stops. When stopped the windings no longer have current and the power consumed is minimized.

Shorted Braking or Plugging does put high electrical stresses on the windings and should be used to stop a rotor, not to slow or control speed.

Regenerative braking can also be used with this controller, called E-Brake in this document. In regenerative braking the PWM signal remains active and is reduced to slow the motor. If the motor is being externally driven by another device or simply by an inertial load it is considered to be in an over-run state where the rotation is generating more energy than the drive section is supplying. In this case the FET structure will sink energy rather than source energy. Current can then flow from the motor to the power supply or battery regenerating energy from the kinetic energy of the mechanical system. This feature can come into play if the motor were driving a vehicle such as a bicycle.

Regenerative braking is excellent for slowing or controlling speed as it recovers energy and is more efficient. Care must be taken to ensure the power source is capable of sinking current as well as sourcing current.

Protection feature sensor information is derived from the drive inputs such as motor current and position sensing and affects the operation by contributing to the control block. Die temperature is monitored and also affects overall control.

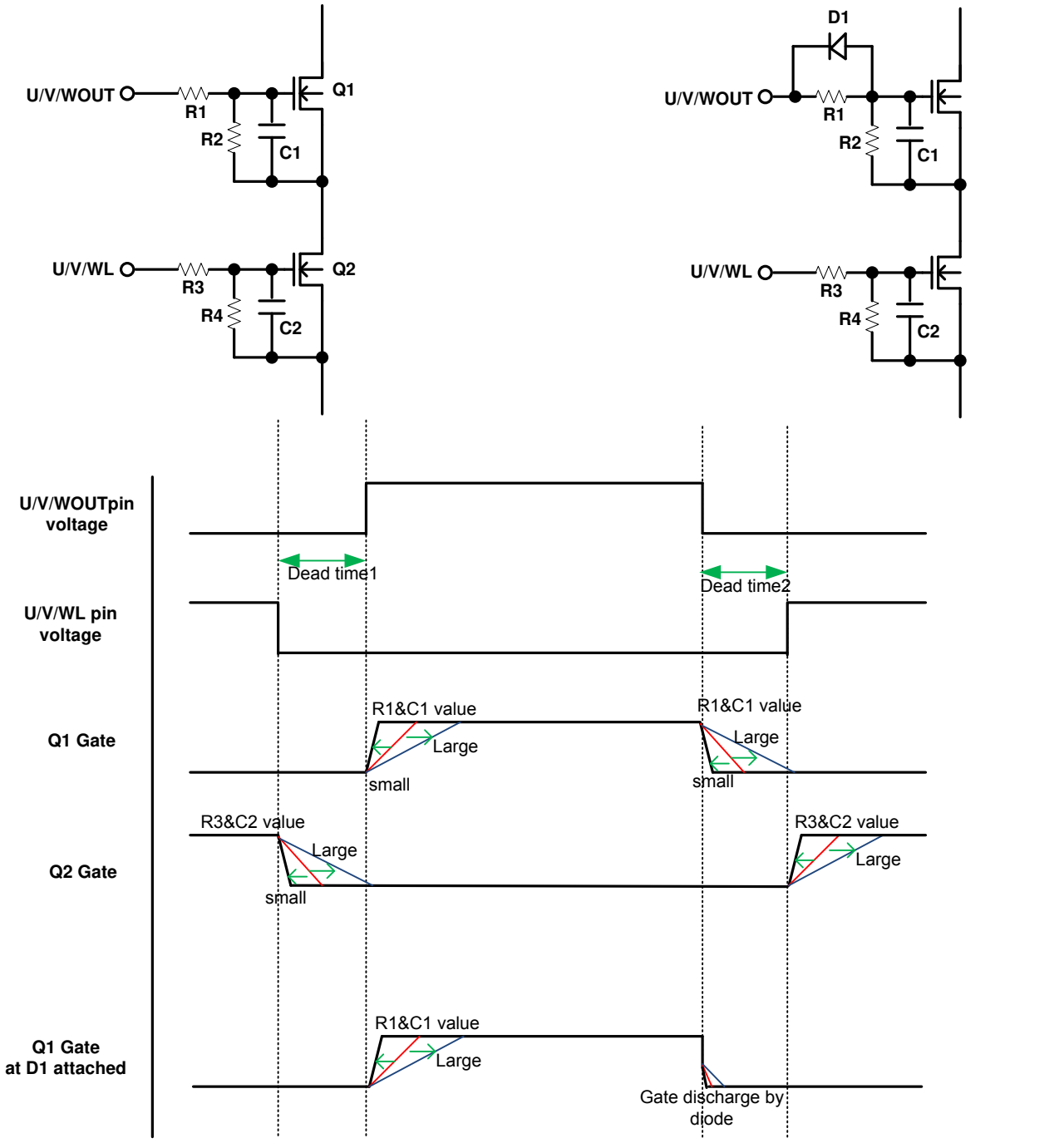


Fig.9

1. Cycle-by-cycle Current Limit

Current limit is detected as a voltage difference across the sense resistor greater than the internal reference of 0.1V. If the current desired is quite high or the sense resistor is large the voltage across the sense resistor can be scaled down with an external resistor divider. A small cap should be placed across the sense resistor for noise suppression.

When current limit is detected the information is sent to the control logic which reduces the duty cycle to reduce the current.

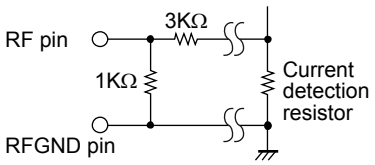


Fig.10

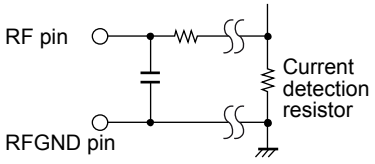


Fig.11

2. PWM Oscillator Circuit

The PWM frequency is determined by the value of the capacitor C connected to the PWM terminal.

$$f_{PWM} = 1/(50000 \times C)$$

A 1000pF capacitor would yield about 20kHz

The power loss in the output stage will increase when the PWM frequency is too high due to switching losses during transitions. When the PWM frequency is too low, the switching will cause acoustic noise in the motor. The Recommended PWM frequency is between 20kHz and 40kHz. To prevent acoustic, electrical, commutation noise and other adverse effects, route the GND terminal of the capacitor as close as possible to the GND terminal of the IC.

3. Control Method

This IC adopts the current feedback method which reduces output current ripple that would cause acoustic noise in the motor. The current control voltage is applied to an amplifier with gain characteristic as shown below.

The user applies a current control voltage (1.3V to 3.6V) to the EI^+ pin.

GAIN of control circuit is TYP = 0.03V/V when the voltage on the terminal EI^+ terminal is less than 3V and TYP = 0.1V/V when it is higher.).

This generates the reference voltage against which the current feedback voltage applied to the RF pin is compared.

Current Control Function

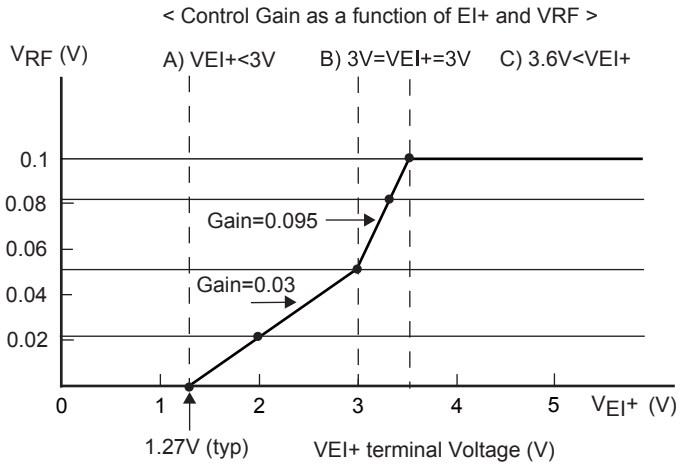


Fig.12

A) VEI+ < 3V

VRF = (VEI+ – 1.27) × GDFSL1 (V)

Driving gain: GDFSL1 = 0.03 (times)

I = VRF/Rf (A)

Rf(Ω):current sense resistor value

Example(TYP model)

When the sense resistor is 10m Ω,

VEI+ = 2V

VRF = (2 – 1.27) × 0.03 = 0.0219 (V)

I = VRF/Rf = 0.0219/0.01 = 2.19 (A)

VEI+ = 2.8V

VRF = (2.8 – 1.27) × 0.03 = 0.0459 (V)

I = VRF/Rf = 0.0459/0.01 = 4.59 (A)

B) 3V ≤ VEI+≤3.6V

VRF = (VEI+ – 3)×GDFSL2+0.0519 (V)

Driving gain:GDFSL2 = 0.095 (times)

I = VRF/Rf (A)

Rf (Ω) : sense resistor

Example (TYP model)

When the sense resistor is 10m Ω

VEI+ = 3V

VRF = (3 – 3) × 0.095 + 0.0519 = 0.0519 (V)

I = VRF/Rf = 0.0519/0.01 = 5.19 (A)

VEI+ = 3.3V

VRF = (3.3 – 3) × 0.095 + 0.0519 = 0.0804 (V)

I = VRF/Rf = 0.0804/0.01 = 8.04 (A)

VEI+ = 3.5V

VRF = (3.5 – 3) × 0.095 + 0.0519 = 0.10415 (V)

I = VRF/Rf = 0.10415/0.01 = 10.415 (A)

C) 3.6V < VE+
VRF = 0.105 (V) (fixed)
I = VRF/Rf (A)
Rf(Ω):sense resistor

Example (TYP model)
When the sense resistor is 10m Ω

VRF = 0.105 (V) (fixed)
I = VRF/Rf = 0.105/0.01 = 10.5 (A)

4. Bootstrap Circuit

The bootstrap circuit generates a boost voltage used by the controller to drive the upper FET's into enhancement. The gate voltage needed on the upper FET gates is higher than the operating voltage at Vcc requiring this boost.
The boost voltage is generated by pulling down the phase node at xFG when the lower FET is on. This charges the Boost Capacitor through the external boost diode.

When the lower FET is released the phase node at xFG rises and the charged capacitor supplies the xH boost supply pin with a voltage above the upper FET threshold voltage. The xH boost pin voltage is then used as the source for the upper FET gate drive voltage at xOUT. When the motor is running at less than 100% duty cycle, the bootstrap cap is charged during every PWM cycle.

When the motor is running at 100% duty cycle, the bootstrap capacitor is charged at every commutation event, which corresponds to the time required for 120 electrical degrees of motor rotation.

100% Duty Cycle will most likely occur at light loads and low supply voltage, where speed will be low and the commanded current cannot be achieved.

Calculation of required bootstrap capacitor value for 100% duty cycle support (refer to figure 13) :

Assume minimum motor speed of 15,000 RPM and a 4-pole motor.

Size of the Bootstrap Capacitor = (Discharge current × Time of electrical angle of 120 degrees) divided by (allowable boost voltage drop)
Total Current Draw -> (Current Drawn in the gate drive Circuit) + (driving current to charge the external FET)
*Average Drive Current of external MOSFET is negligible
Current Draw in the Circuit : Constant current in the circuit=180μA,
load resistor in the circuit=28k Ω
Boost voltage=12V
Therefore
Total Current Draw =180μA +(Boost voltage÷28k)=180μA+(12÷28k)=609μA

$$\text{Time of electric angle of 120 degree} = \frac{60 \times 2}{\text{Rotational speed} \times \text{Pole} \times 3} = \frac{60 \times 2}{15000 \times 4 \times 3} = 667\ \mu s$$

This equation holds for motors with either 120 degree or 60 degree sensor positioning.
In order to limit the boot voltage drop to a recommended value of 2V under worst-case conditions,
Bootstrap capacitor value = (609μ×667μ) ÷2=0.2μF

Due to variations of Capacitor Value Distribution and variations over the Bias voltage, Temperature and Current it is recommended to multiply the above result by 10.

Bootstrap capacitor value=0.2μF×10=2.0μF → 2.2μF

Recommended Capacitor working voltage ≥ 25V
A capacitor which has good temperature characteristics is also recommended.

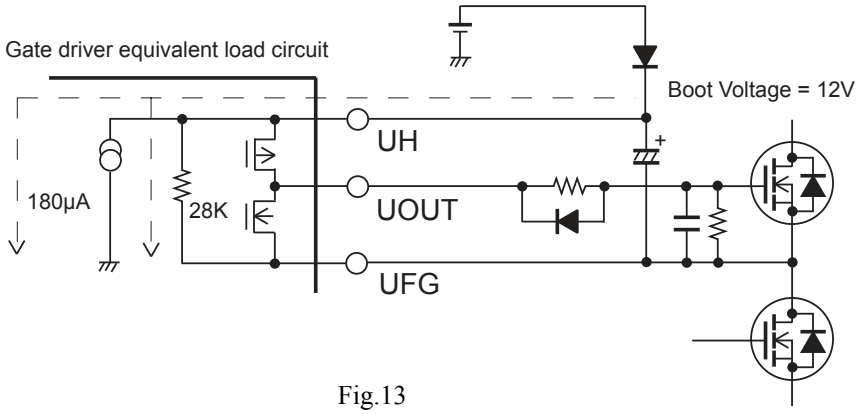


Fig.13

5. **Position Input Signal (Hall Effect sensors)**

Typically the position input signal is generated by a Hall Effect sensor at the rotor. These signals are usually supplied as open-drain outputs (but may also be supplied via an external buffer).

Although the Hall output often has an internal pullup resistor of around 100K it is common practice to add an external pullup of a lower value at the controller to reduce noise effects.

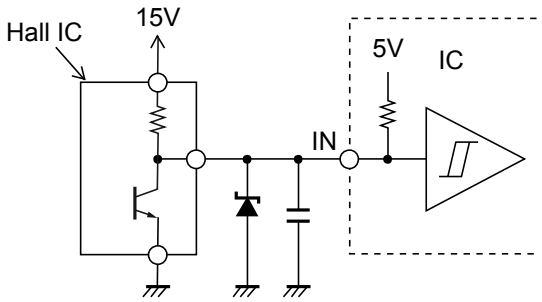


Fig.14

If the Hall Effect output is supplied by a voltage source above 5V a zener clamp or voltage divider is used to reduce the signal level for controller compatibility. Although the controller input is a Schmitt inverter with around 1.0V of hysteresis a capacitor is sometimes added for more noise immunity.

If all Hall Effect sensors are high at the same time all output drives are turned off as it is a clear error condition.

6. Low Voltage Shutdown circuit

The voltage applied to the terminal LVS1 is monitored by the low voltage shutdown circuit. LVS1 is compared internally with a 2V reference and considered to be a low input voltage condition if below 2V. All outputs will be turned off while this state exists.

LVS1 is the comparator non-inverting input and LVS2 is the comparator output. This allows an external resistive network to introduce the amount of hysteresis desired.

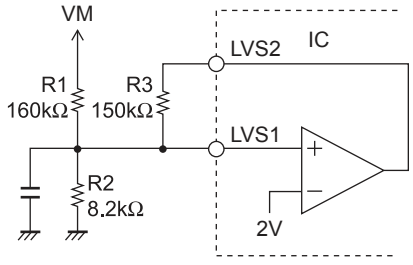


Fig.15

If this circuit operation is not desired the LVS1 input should have a voltage attached such that: 2V < LVS1 <5V
Leaving LVS1 open is always detected as an under voltage state.

The upper and lower hysteresis levels are calculated as:

Detection voltage ≈ (2.0/R2) × (R1 + R2)
Release voltage ≈ (2.0/RX) × (R1 + RX) * RX = (R2 × R3)/(R2 + R3)
If, for example, R1 = 160kΩ, R2 = 8.2kΩ and R3 = 150kΩ,

Then the detection voltage is about 41.0V and the release voltage is about 43.2V with a hysteresis loop of about 2.2V

There is no hard internal threshold at which logic is shutdown as that decision should be a part of the LV shutdown consideration.

In the event Vcc drops below the specified 12V minimum recommended operation it is possible to maintain logic operation at lower voltages down to around 10V, but this level is in no way guaranteed nor tested in manufacturing and is not recommended for normal operation.

7. SB (Start/Brake) circuit

This pin is used to enable the motor driver.

- When the terminal SB is connected with GND → Normal operation mode.
- When the terminal SB is set above 5V → Shorted Brake mode

The output of UL/VL/WL is set to "high" in the Shorted Brake mode. All the lower output MOS-FETs are turned on. (Note that even in the Shorted Brake mode, the motor will 'coast' if BR is 'high', and will brake if BR is 'low').

8. Power Supply Stabilization

Since this IC has a switching drive system, noise is easily generated in the power line.
Therefore connect a capacitor with sufficient capacitance between the terminal V_{CC} and GND for stabilization.
When a diode is to be inserted on the power line to prevent damage from reverse connection of power supply, it is necessary to choose a large diode size because noise is easily generated on the power line.

9. Stabilization of the regulator output voltage

A capacitor of 0.1μF or more should be connected between the terminal V5 (5V : control circuit power supply) and GND. The GND terminal of the capacitor should be as close to the ground terminal of the IC as possible.
The V5 terminal can be used to supply external loads of up to 30mA. However, if a large load current is applied, it should be confirmed that the temperature rise of the IC is not excessive.

10. Direction control: Forward/Reverse Operation (F/R)

If the direction is changed while the motor is rotating, measures to prevent the shoot-through current in the output stage are used.
However, a current of more than the current limit value may flow to the output transistors because of the large motor BEMF.
Power FETs that can survive this large current must be chosen if it is expected to change direction while the motor is rotating.

11. Locked Rotor protection (CSD)

To protect the motor and the IC in the locked rotor condition this IC has built-in locked rotor protection. If the Hall input signal is not switched for a given length of time in the motor drive state, the outputs on the ON side (UOUT, VOUT and WOUT) are turned off. The time is set by the value of capacitor connected to the CSD terminal.

Set time (s) = 33 × C (μF)

When the capacitor of 0.01μF is connected, the protection time becomes about 0.3 seconds.
The set time must be adequate for the motor start-up time. This function generates the initial reset pulse, the logic circuit goes into a reset and the speed cannot be controlled until this time expires.
Therefore, if the locked rotor protection circuit is not used connect a resistor of about 150kΩ and a capacitor of about 4700pF in parallel between the terminal CSD and GND.
To release the state of the locked rotor protection, either of the following operation is necessary.

- EI^+ input is reduced to 1.1V or less.
- The power supply is removed and re-applied.

12. Switching function of Hall input phase (60°/120°)

The switching of the three Hall input phase difference (between 120° and 60°) can be performed by the terminal HSEL.

- HSEL = "High" : 120°
- HSEL = "Low" : 60°

13. E-Brake Function (BR and BRSET)

When the BR pin is set low the IC enters the E-Brake mode. The lower MOSFET's short the motor coils in phase as defined by the voltage on the BRSET pin.
(Shorted Brake: all the output low-side MOS-FET are turned on.) The braking strength is continuously adjustable by supplying a PWM drive signal to the low-side FETs.

The Duty cycle is set by the voltage at the BRSET pin over a range of 1.1V (100%) to 3.0V (0%).(see Fig.16,17)
Figure a) shows normal motor rotation. In this case, it drives from upper side of OUT_U to lower side of OUT_V.
Figure b) shows the Shorted Brake mode. The current recirculates in the low-side FET.
Figure c) shows the All off mode. The current flows through the body diode of the high-side FET of OUT_V to VM.

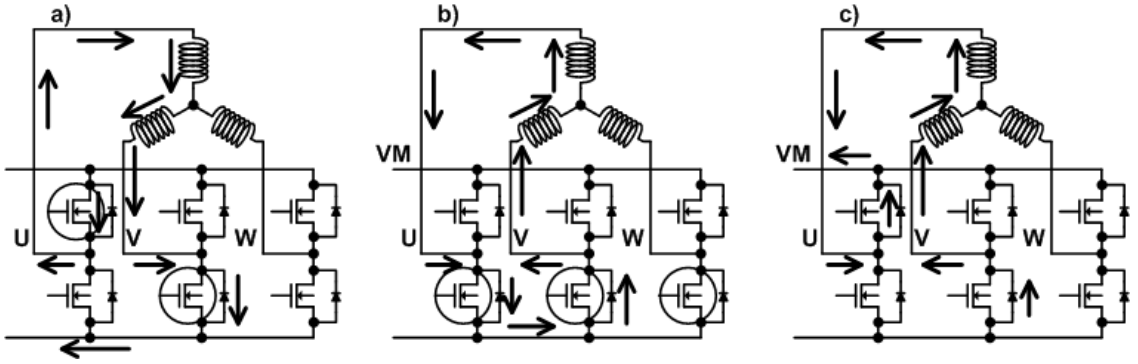


Fig.16

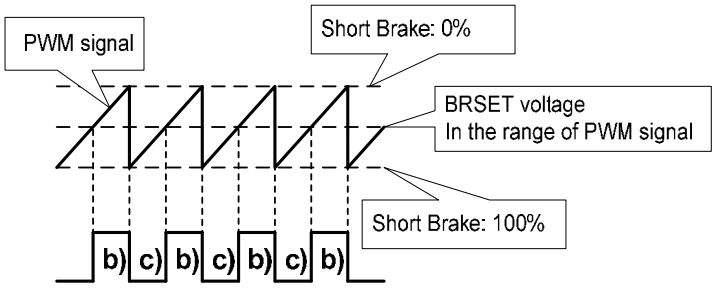


Fig.17

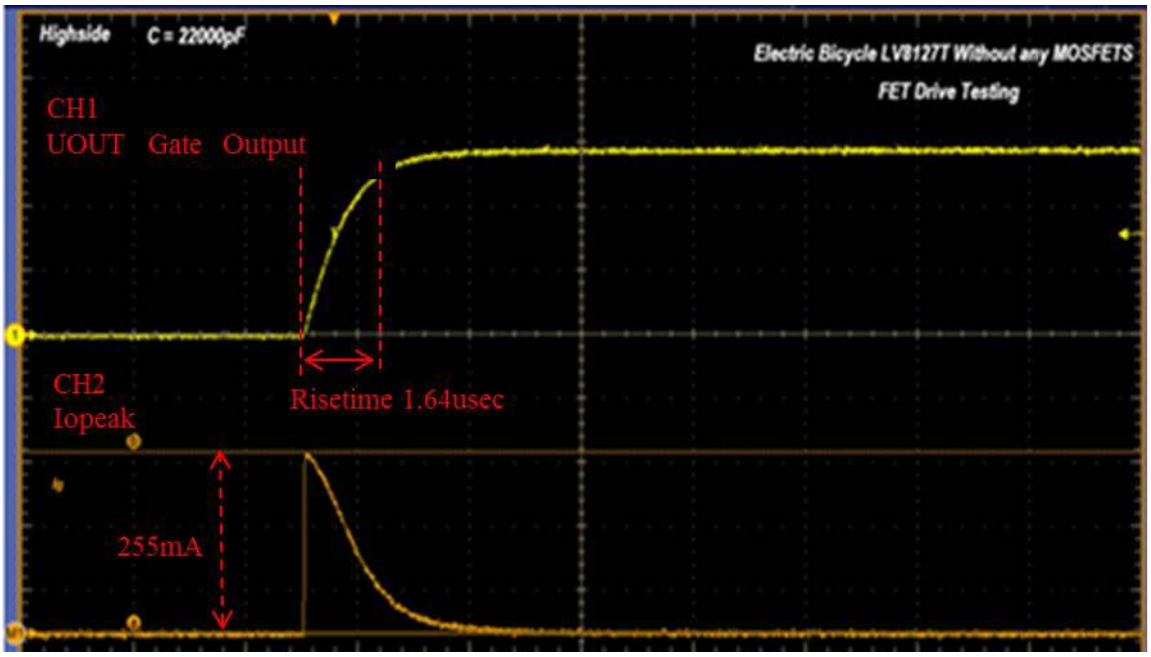
14. Gate driver current calculation example:

Gate drive is a function of internal FET Rds and Vcc as this voltage is applied to the Gate relative to the external FET source. For the lower FET drive the circuit is simple. For the upper FET drive Vcc is added to the output voltage at U,V,W output nodes by the boost voltage action.

Ipeak is then simply Ipeak = Vcc/Rds.

An example: The typical upper internal drive is 58Ω, including the FET Rds. If Vcc = 14.9V, Ipeak = Vcc/Rds = 14.9V/58Ω = 255mA

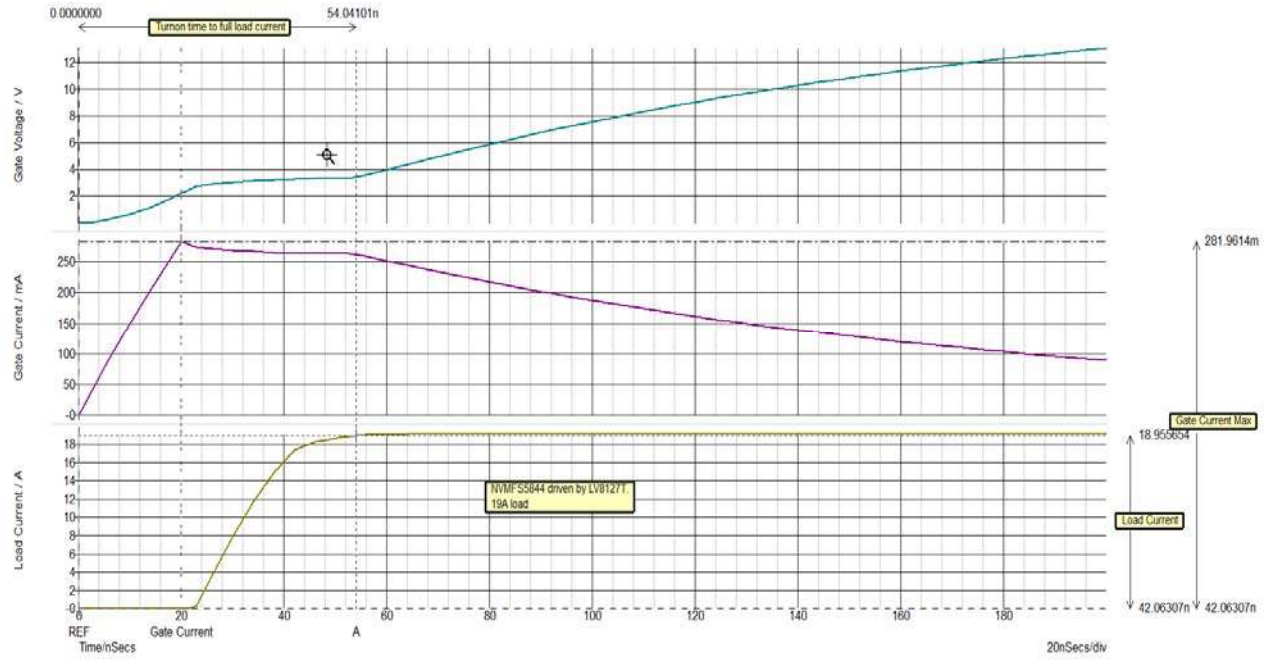
Illustration of a FET driver output loaded with a single heavy capacitance showing the peak value.

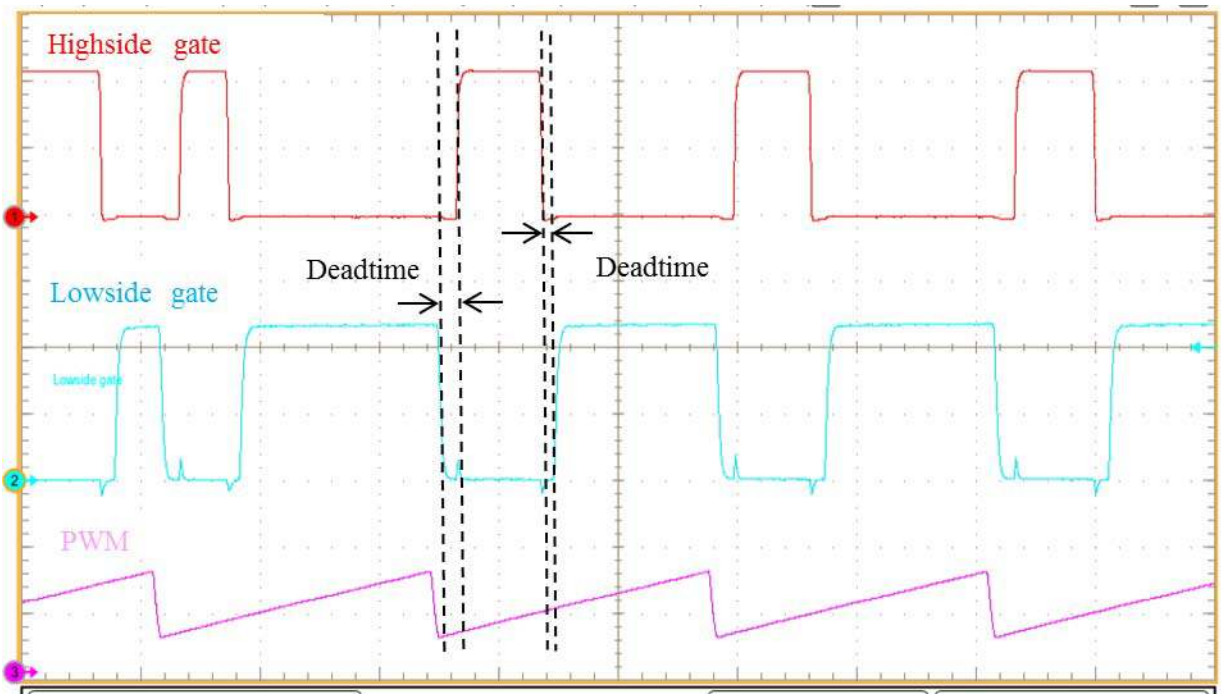


CH1	5V/div
CH2	90mA/div
Time	2.5μsec/div

Illustration below shows typical output phase FET turn-on for an NVMFS5844 driven into a 19A resistive load by the LV8127T.

Gate Drive current reaches 281 mA while Drain transitions from zero to 19A





Waveform of Synchronous rectification (Diode Emulation).

During a PWM switching cycle the low side power FET is turned on during the PWM off cycle to shunt motor energy back to the supply. Without this action the energy is forced through the FET body diode and is dissipated rather than recovered. Note the high side gate drive is aligned with the beginning of each PWM cycle. The low side switch is active during the PWM off time. A small deadtime is inserted between the gate turn-ons to eliminate possible destructive current shoot-through.

Layout and circuit design considerations

Output drive Circuit –

- Short recovery time diodes should be used in the FET gate drive circuits to reduce/eliminate short shoot-through current spikes. HF ringing across the bridge pairs can be effectively suppressed with a 0.1 uF cap mounted immediately beside the FETs as shown in the application schematic of Fig.4.
- The gate conditioning resistors and capacitor in the application schematic allow the gate drive to be customized for a specific application by controlling gate transition slew rates. This allows the user to optimize the tradeoff between noise and efficiency according to the application.
- Notice the effects of the various FET drive components in the diagram of Fig.9. These networks allow considerable adjustment of FET rise and fall times to eliminate Ringing, harmonic content and power losses.
- Notice the effects of the gate discharge diode D1 in the diagram of Fig.9.

The accuracy of the current limit value is assured by Kelvin connection of the RFGND and RF sense terminals to the current sense resistor. When a current sense resistor with very small resistance value is used, the PCB trace resistance value for each phase should be matched. When the trace resistance for each phase is different, the current limit value changes at every change of phase. Therefore, motor vibration and noise may occur.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8127T-TLM-H	TSSOP36 (275mil) (Pb-Free / Halogen Free)	1000 / Tape & Reel
LV8127T-MPB-H	TSSOP36 (275mil) (Pb-Free / Halogen Free)	48 / Fan-Fold