User manual

Document information

Information	Content								
Keywords	OM13320 Fm+ development kit, OM13260 Fm+ I2C bus development board, OM13303 GPIO target board								
Abstract	Installation guide and User Manual for the OM13541 34-bit GPIO Daughter Card that connects to OM13260 Fm+ I2C bus development board. This daughter board makes it easy to test and design with the PCAL6534, an ultra- low voltage translating 34-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I2C-bus interface. This daughter board, along with the Fm+ Development board, provides an easy to use evaluation platform.								



Revision history

Rev	Date	Description
v.1	20190801	Initial version

1 Introduction

The PCAL6534 34-bit GPIO evaluation board allows bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V on SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V on I/O ports with active low reset input control and open-drain active low interrupt output indicator (red LED) plus one hardware address input setting to select one of four different slave addresses. A graphical interface allows the user to easily explore the different functions of the I/O expander.

The IC communicates to the host via the industry standard I^2 C-bus/SMBus port. The evaluation software runs under Microsoft Windows PC platform.

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2 Features of the OM13541 34-bit GPIO daughter board

- Direct connection to OM13260 Fm+ I²C-bus Development board
- Easy to use GUI-based software demonstrates the capabilities of the PCAL6534
- Jumper configuration for most features of PCAL6534
- Flexible power supply configuration: 3.3 V, 5 V or external supply
- Direct connection to OM13303 GPIO Target board for I/O visualization
- · Convenient test points for easy scope measurements and signal access
- Jumper configuration of device I²C address
- LED indicators for power and INT
- No external power supply required and obtains +5 V power from PC USB port

3 Hardware description

3.1 Power supply jumpers

The power supply selection for the OM13541 is very flexible and allows for detailed analysis and evaluation of 34-bit GPIO device. J13 selects +5V_PWR supply from either the tester connector J1 (pins 4 and 6, +5V_TSTR) or the Fm+ board connector J11 (pins 7 and 12, +5V). J7 selects VDDP (U1 pin A6) supply from either +5V_PWR or +3V3 (J11 pins 8 and 11) and J2 selects VDDI (U1 pin A1) supply from either +3V3 (J11 pins 8 and 11) or +5V_PWR. If external power operation is desired from TP2 (VDDP-IN) and TP3 (VDDI), no jumper is required on J7 and J2. The D2 green LED is lit when VDDP is available.

3.2 SCL and SDA jumpers

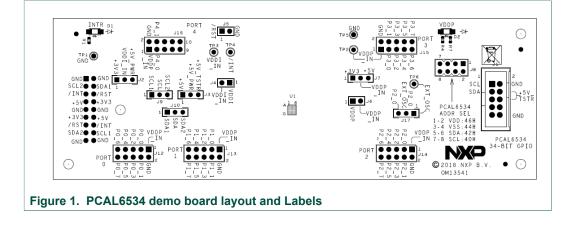
The I^2C -bus signals SDA and SCL supplied to the device under test can be sourced from either the Fm+ board via J11 or the tester via J1. Jumpers J10 and J9 select the I^2C bus 1 or bus 2 signals from the Fm+ board, shorting pins 1 to 2 to select I^2C bus 1 while shorting pins 2 to 3 to select I^2C bus 2.

3.3 Device reset, interrupt and address pin selection

- **Reset** (U1, pin A5), the device is resetting when shorting pin 1 to 2 on jumper J5
- Interrupt (U1, pin B1), open-drain interrupt (INT) output is activated and D1 red LED is lit when any input state differs from its corresponding Input Port register state, TP4 can be used to monitor the INT pin 32.
- Address input (U1, pin A4), jumper J8 is used to select device address as shorting pins 1 to 2 (VDD, address is 46h), shorting pins 3 to 4 (VSS, address is 44h), shorting pins 5 to 6 (SDA, address is 42h), shorting pins 7 to 8 (SCL, address is 40h).

3.4 Board layout viewer

Figure 1 shows all jumper locations and labels on PCB.



3.5 Connector pinouts

• **J1** (10-pin male tester connector) is connected to master which is driving either I²Cbus for PCAL6534. This is easily achieved with third party development tools from Total Phase (<u>http://www.totalphase.com</u>). There are two tools called Aardvark and Beagle that direct connect to this board through J1.

J1 Pin #	Function	Board connection
1	SCL	U1 pin A3 (PCAL6534)
2,10	GND	Ground
3	SDA	U1 pin A2 (PCAL6544)
4, 6	+5V_TSTR	J13 pin 3
5	SDOUT (MISO)	NC
7	SCLK	NC
8	SDIN (MOSI)	NC
9	/CS (SS)	NC

Table 1. J1 10-pin tester connector

Note: Since SDA and SCL are both connected to the device (U1) under test, the Aardvark and the Fm+ Development board cannot be used simultaneously. The Beagle, a bus sniffer, does not have any issues.

 J11 (18-pin female connector) can connect directly to the OM13260 Fm+ Development board. This connector provides power, I²C signals and other ancillary signals.

J11 Pin #	Function	Board connection
1, 2, 9, 10, 17, 18	GND	Ground
3	SCL2	SCL Bus 2 to J9 pin 3
4	SDA1	SDA Bus 1 to J10 pin 1
5, 14	INT	Interrupt to U1 pin B1, LED (D1) and TP4 (test point 4)
6, 13	RESET	U1 pin A5 and J5 pin 1
7, 12	+5V	J3 pin 1
8, 11	+3V3	J2 pin 1 and J7 pin 1
15	SDA2	SDA Bus 2 to J10 pin 3
16	SCL1	SCL Bus 1 to J9 pin 1

Table 2. J11 18-pin Fm+ board connector

Note: The connector on the Fm+ board is a male, shrouded 14 pin types, while the connector on this 34-bit GPIO board is an 18-pin female. The reason lies with the shroud around the 14-pin connector. To ensure correct mating of the female with the male, two pin positions on both female sides are grounded.

• J12, J13, J14, J15, J16 (10-pin male connector) is connected to GPIO target board (OM13303) which consists of eight LEDs and eight switches and connects directly to this 34-bit GPIO board through J12 (I/O of port 0), J13 (I/O of port 1), J14 (I/O of port 2), J15 (I/O of port 3), J16 (I/O of port 4). These switches and LEDs on GPIO target board permit easy exercise of the I/O functionality of the device under test. The LEDs light red when the voltage on that channel is below VDDP x 0.3V and LEDs light green

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when the voltage is above VDDP x 0.7V. The LEDs remain off when the voltage is between those two levels.

Table 3. J12, J13, J	able 3. J12, J13, J14, J15, J16 10-pin GPIO target board connector									
J[12:16] pin #	Function Board connection									
1	VDDP_IN	J7 pin 2 and TP2 (test point 2) and by J6 to VDDP (U1 pin A6)								
2	GND	Ground								
3	P[0:4]_0 (I/O 0)	U1 pin C1, D3, E3, E6, B5								
4	P[0:4]_1 (I/O 1)	U1 pin B2, F1, F4, E4, B4								
5	P[0:4]_2 (I/O 2)	U1 pin B3, E2, G5, D5								
6	P[0:4]_3 (I/O 3)	U1 pin D1, G1, G5, D6								
7	P[0:4]_4 (I/O 4)	U1 pin C2, G2, G6, D4								
8	P[0:4]_5 (I/O 5)	U1 pin C3, F2, F6, C5								
9	P[0:4]_6 (I/O 6)	U1 pin E1, G3, F5, C6								
10	P[0:4]_7 (I/O 7)	U1 pin D2, F3, E5, C4								

3.6 All jumpers default setting and test points

Figure 2 shows the PCAL6534 demo board.

- D1 (red LED) is connected to interrupt output (U1 pin B1), it is ON when INT is asserted
- TP4 (INT) is connected to interrupt output (U1 pin B1) for probing use.
- TP1 and TP5 are GND test points for probing use.
- TP6 (EXT_OSC) is external clock input through J17 (1-2) to P2_0 (pin E3) for debouncer circuit use
- TP2 (VDDP IN) and TP3 (VDDI) are connected to external power inputs.
- All jumpers default settings and functions are shown in Table 4.

Table 4. All jumpers setting for test and evaluation

Jumper	Default setting	Comment
J7 (3-pin)	2-3 (VDDP_IN = +5V_ PWR)	This jumper is used to select VDDP for U1 device (pin A6) 1-2: select +3V3 2-3: select +5V_PWR
J2 (3-pin)	1-2 (VDDI_IN = +3V3)	This jumper is used to select VDDI for U1device VDDI (pin A1) 1-2: select +3V3 (from Fm+ development board) 2-3: select +5V_PWR
J3 (3-pin)	1-2 (+5V = +5V_PWR)	This jumper is used to select +5V_PWR source 1-2: select +5V from Fm+ development board 2-3: select +5V_TSTR from tester (beagle) board
J4 (2-pin)	Short	Short: connect VDDI to U1 device VDDI (pin A1) Open: connect current meter to measure the IDDI on U1 device
J5 (2-pin)	Open	Short: force /RESET (U1 pin A5) to GND Open: 10K pull-up /RESET (U1 pin A5) to VDDI
J6 (2-pin)	Short	Short: connect VDDP_IN to U1 device VDDP (pin A6) Open: connect current meter to measure the IDDP on U1 device

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Jumper	Default setting	Comment					
J8 (4x2-pin)	1-2 (VDDI)*note1	This 4x2 jumper is used to select input value for ADDR (U1 pin A4) 1-2: select VDDI (address is 0x46 for PCAL6534) 3-4: select VSS (address is 0x44 for PCAL6534) 5-6: select SDA (address is 0x42 for PCAL6534) 7-8: select SCL (address is 0x40 for PCAL6534)					
J9 (3-pin)	1-2 (SCL = SCL1)	This jumper is used to select SCL source for U1 device (pin A3) 1-2: select SCL1 (bus 1 from Fm+ development board) 2-3: select SCL2 (bus 2 from Fm+ development board)					
J10 (3-pin)	1-2 (SDA = SDA1)	This jumper is used to select SDA source for U1 device (pin A2) 1-2: select SDA1 (bus 1 from Fm+ development board) 2-3: select SDA2 (bus 2 from Fm+ development board)					
J11 (18-pin)	Connect Fm+ development board	This 18-pin female connect to PORT A/B/C/D (14-pin male) on Fm+ development board (OM13260) for power supply, I2C-bus and control signals to test					
J12-J16 (10-pin)	Connect to GPIO Target board	This 10-pin male connect to GPIO target board (OM13303) for input/ output pins test					
J17 (3-pin)	2-3 (P2_0)	This jumper is used to select function either P2_0 or EXT_OSC for U1 device (pin E3) 1-2: select external oscillator (EXT_OSC) input for debounce circuit use 2-3: select P2_0 input as normal operation					
1. Default PCAL653	34 slave address is set to 0	x46 (ADDR = VDD)					

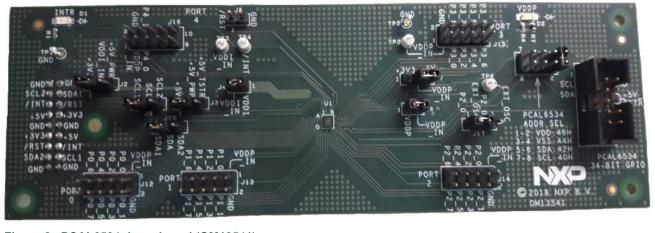
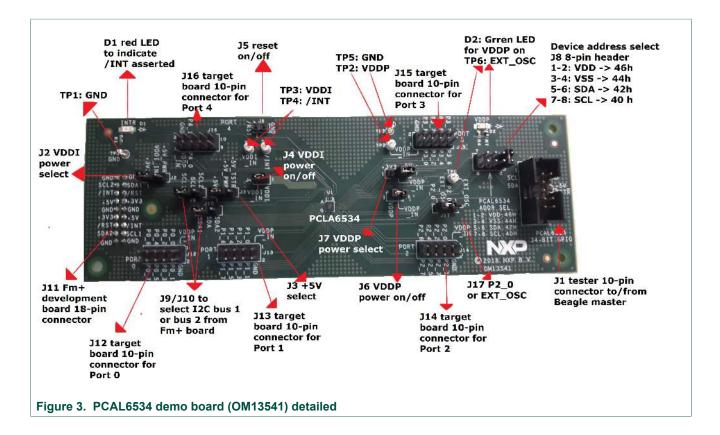


Figure 2. PCAL6534 demo board (OM13541)

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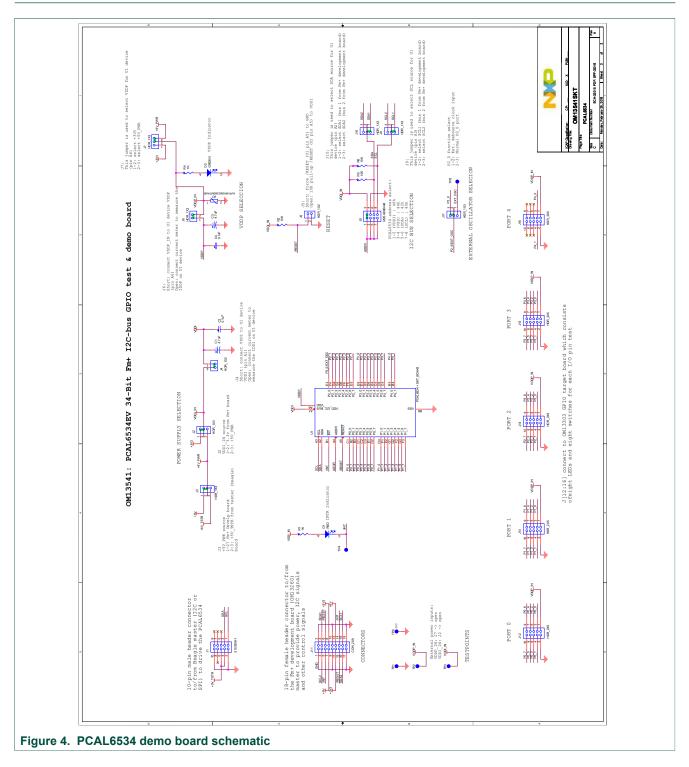


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4 Schematic



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5 Installation

5.1 PCAL6534 demo board, Fm+ development board, GPIO target board

The OM13541 PCAL6534 34-bit GPIO demo board is a daughter card to the OM13260 Fm+ I2C bus development board, which is part of the Fm+ development board kit (OM13320); three I/O ports (8-bit × 3) on PCAL6534 are connected to the GPIO target board for I/O visualization. You may download the software, user manual, and find ordering information at the NXP web site:

https://www.nxp.com/products/analog/interfaces/ic-bus/ic-led-controllers/ic-fm-plusdevelopment-board:OM13320

5.2 OM13541 connection to Fm+ I²C-bus development board

The OM13260 Fm+ I²C-bus development board should be disconnected from your PC before mounting the OM13541 board with GPIO target board on to it. The OM13541 board has an 18-pin female connector (J11) that connects to CN4 14-pin male connector on the Fm+ development board (OM13260) as shown in <u>Figure 5</u>. Five GPIO Target boards (OM13303) through ribbon cables connect to 10-pin male connectors (J12, J13, J14, J15, J16) on OM13541 PCAL6534 34-bit GPIO demo board for 8-bit I/O port0, port1, port2, port3 and port4.

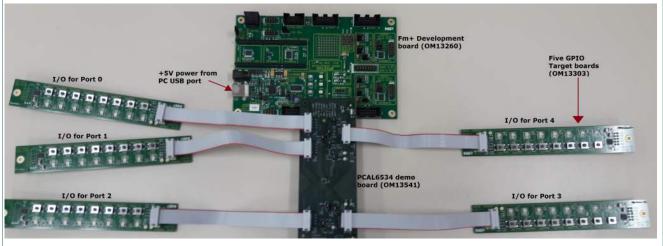


Figure 5. PCAL6534 demo board (OM13541) mounting to the Fm+ development board (OM13260) and connecting to five GPIO target boards (OM13303)

6 PCAL6534 evaluation steps with Fm+ development board

NXP Fm+ Evaluation Board - 0 × File Device Options Window Help 3V3 ↑ 5V PORT A PCA9672 8ch GPIO PORT B I2C BUS 2 PULL UP I2C BUS 2 LPC -RESISTORS XPRESSO | 1 PCA9665 BUS PCA9955 16ch LED CONTROLLER PORT E Parallel Port 3V3 1 5V I2C BUS 1 PULL UP LPC1343 I2C BUS 1 RESISTORS MCU PCA9672 8ch GPIO PORT D PORT C USB-I2C Hardware Detected I2C: 1000 kHz SPI: 1 MHz Transmission successful

The PCAL6534 is controlled by the Fm+ development board GUI in Expert mode as shown in <u>Figure 6</u> and <u>Figure 7</u>.

Figure 6. Select the Expert Mode from Fm+ development board GUI (1 of 2)

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		Device	Options	- [I ² C Experi Window	Help	_					•
lsg #	Start	Address	R/W	Data				Stop?	Additional	Notes	
2								 	Delay		- 11
1	ST ST										
2	ST										- 2
4	ST										-
5	ST										
6	ST										
7	ST										1
8	ST										
Ser	nd Mess	sage	Se	end All	Send Sequence		Send Continuously				
	nd Mess we Msg.			end All	Send Sequence		Send Continuously				

Figure 7. Select the Expert Mode from Fm+ development board GUI (2 of 2)

Connect the hardware as described in <u>Section 5.2</u>. All jumpers are in default setting and device address is set to 0x46h on J8 (set ADDR = VDDI) for PCAL6534 demo board. When you have correctly installed the software and the demonstration board hardware is connected and recognized by the computer, start the Fm+ development board software. As shown in Figure 7, when the demonstration board hardware is correctly connected to the USB port and the computer recognizes it, the message "USB-I2C Hardware Detected" is displayed on the bottom of the window.

6.1 PCAL6534 output shifting pattern demo for all five ports

- 1. From the 'Device' drop-down menus select 'Expert Mode' as shown in Figure 7.
- 2. Copy the "output shifting pattern on all five ports" text file as shown below. From the 'File' drop-down menus select 'Open', and from the "open data file" window to select the "output shifting pattern on all five ports" text file.

Expert Mode Data File

46,Write,Yes,200,0F,00,00,00,00,00,Comments: set all GPIOs as output ports 46,Write,Yes,200,05,FF,FF,FF,FF,FF,Comments: write registers 04,05,06 to set all output ports to 1s

46,Write,Yes,200,05,FE,FE,FE,FE,FE,Comments: set bit0 to 0 in all five ports 46,Write,Yes,200,05,FD,FD,FD,FD,FD,Comments: set bit1 to 0 in all five ports

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46,Write,Yes,200,05,FB,FB,FB,FB,Comments: set bit2 to 0 in Ports 0 to 3 46,Write,Yes,200,05,F7,F7,F7,F7,Comments: set bit3 to 0 in Ports 0 to 3 46,Write,Yes,200,05,EF,EF,EF,EF,Comments: set bit4 to 0 in Ports 0 to 3 46,Write,Yes,200,05,DF,DF,DF,DF,Comments: set bit5 to 0 in Ports 0 to 3 46,Write,Yes,200,05,BF,BF,BF,BF,Comments: set bit5 to 0 in Ports 0 to 3 46,Write,Yes,200,05,F7,F7,F7,F7,Comments: set bit6 to 0 in Ports 0 to 3 46,Write,Yes,200,05,7F,7F,7F,7F,Comments: set bit7 to 0 in Ports 0 to 3 Sequence:01,02,03,04,05,06,07,08,09,10

- 3. After opening the "output shifting pattern on all five ports" text file, the "NXP Fm+ Board GUI" in Expert mode screen is displayed as shown in <u>Figure 8</u>.
- 4. Click the 'Send All' button; all the valid messages on the screen are sent in the order of the row number (Msg #). This action is performed once.

· · · · · · · · · · · · · · · · · · ·			Carl State States	s Window H					. 6
Msg #	Start	Address	R/W	Data			Stop?	Additional Delay	Notes
1	ST	46	Write	0F,00,00,00,0	0,00		Yes	200	set all GPIOs as output ports
2	ST	46	Write	05,FF,FF,FF,FF,F	F,FF		Yes	200	write registers 05-09 to set all
3	ST	46	Write	05,FE,FE,FE,F	E,FE		Yes	200	set bit0 to 0 in all five portS
4	ST	46	Write	05,FD,FD,FD,	FD,FD		Yes	200	set bit1 to 0 in all five ports
5	ST	46	Write	05,FB,FB,FB,FB,F	B,FE		Yes	200	set bit2 to 0 in all 0-3 ports & bit 0/1
6	ST	46	Write	05,F7,F7,F7,F7,F	7,FD		Yes	200	set bit3 to 0 in all 0-3 ports & bit 0/1
7	ST	46	Write	05,EF,EF,EF,EF,E	F,FE		Yes	200	set bit4 to 0 in all 0-3 ports & bit 0/1
8	ST	46	Write	05,DF,DF,DF,	DF,FD		Yes	200	set bit5 to 0 in all 0-3 ports & bit 0/1
9	ST	46	Write	05,BF,BF,BF,BF,B	F,FE		Yes	200	set bit6 to 0 in all 0-3 ports & bit 0/1
10	ST	46	Write	05,7F,7F,7F,7	F,FD		Yes	200	set bit7 to 0 in all 0-3 ports & bit 0/1
11	ST	46	Write	05,FF,FF,FF,F	F,FF		Yes	200	write registers 05-09 to set all
12	ST	46	Write	05,00,00,00,0	0,00		Yes	200	write registers 05-09 to set all
13	ST	00	Write	06			Yes	0	SW reset
	od More	sage	S	end All	Send Sequence	Send Continuously			
	ve Msg.	= 1	Sendir	ng Msg # 13	01,02,03,04,05,06,07	09 00 10 11 12 12			

Figure 8. Message data in Expert mode to demo "output shifting pattern on all five ports"

6.2 PCAL6534 registers are controlled by Fm+ board GUI

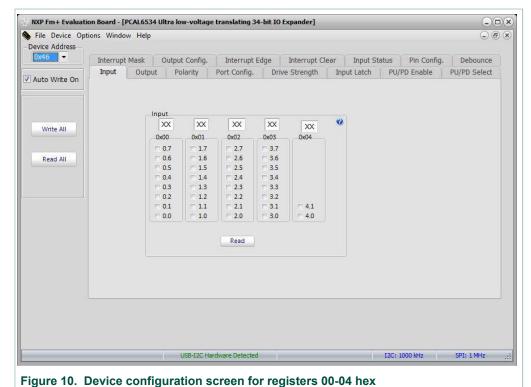
1. Select 34-bit PCAL6534 from I/O Expanders as shown in Figure 9.

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File	e Edit	Device	Options 1	Window He	lp							
	الما 🕙	Į/O	Expanders		•	4-bit I/0) Expanders	- 1				
lsq #	Start	LED	Blinkers and	d Dimmers	•	<u>8</u> -bit I/0) Expanders	-) i		Stop?	Additional	Notes
		Mas	ter Selector	(2-to-1 dem	ux) 🕨	16-bit I	O Expanders	- >			Delay	
1	ST	Mul	tiplexers/Sw	vitches		24-bit I/	O Expanders	- +		Yes	200	set all GPIOs as output ports
2	ST	_	-volatile Re			_	O Expanders		PCAL6534	Yes	200	write registers 05-09 to set all
3	ST			-		a management	Concerning and the second second	+1	PCAL0554	Yes	200	set bit0 to 0 in all five portS
4	ST	- 70°	Time Clock			4 <u>0</u> -bit 1/	O Expanders	1		Yes	200	set bit1 to 0 in all five ports
5	ST	The	rmal Manag	jement	· • • •					Yes	200	set bit2 to 0 in all 0-3 ports & bit 0/1
6	ST	Expe	ert Mode							Yes	200	set bit3 to 0 in all 0-3 ports & bit 0/1
7	ST	SPI	Devices		- F					Yes	200	set bit4 to 0 in all 0-3 ports & bit 0/1
8	ST									Yes	200	set bit5 to 0 in all 0-3 ports & bit 0/1
9	ST	46	Write 05	5,BF,BF,BF,BF	,FE					Yes	200	set bit6 to 0 in all 0-3 ports & bit 0/1
10	ST	46		5,7F,7F,7F,7F						Yes	200	set bit7 to 0 in all 0-3 ports & bit 0/1
11	ST	46		5,FF,FF,FF,FF,FF						Yes	200	write registers 05-09 to set all
12	ST	46	Write 05	5,00,00,00,00	,00					Yes	200	write registers 05-09 to set all
13	ST	00	Write 06	5						Yes	0	SW reset
C -1			Senc	4.41	Cand Co		Sand Castin	i Osurah	2			
Sei	nd Mess				Send Se		Send Contin		9			
	ve Msq.	= 1	Sending 1	Msg # 13	01,02,03,04	1,05,06,07	,08,09,10,11,12	,13				
	reriogr						re Detected					

Figure 9. Device selection screen for PCAL6534

2. Input registers read are shown in Figure 10.



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Device Address 0x46	Television	March C.				ease W	Table and C		Tana A Cha	V N	Dia Carlo	V Debause
	Interrupt	1	Dutput C		Interrupt	-	Interrupt C		Input Sta		Pin Config.	Debounce
Auto Write On	Input	Output	Pola	rity	Port Config.	Driv	e Strength	Inp	ut Latch	PU/F	PD Enable	PU/PD Select
		Out		rr.			0.0	0				
Write All		1.	FF	FF	FF	FF	03					
		_0x(0x06	0x07	0x08	0x09					
		▼ (✓ 1.7 ✓ 1.6	✓ 2.7 ✓ 2.6	▼ 3.7 ▼ 3.6						
Read All		V (▼ 1.5	✓ 2.5	▼ 3.0						
		70		▼ 1.4	₹ 2.4	₹ 3.4						
		V		▼ 1.3	₹ 2.3	▼ 3.3						
		V ().2	▼ 1.2	♥ 2.2	₹ 3.2						
		V (✓ 1.1	♥ 2.1	₹ 3.1	▼ 4.1					
		V (0.0	✓ 1.0	₹ 2.0	▼ 3.0	▼ 4.0					
					Write							
					Read							
					Consumation of the owner							

Figure 11. Device configuration screen for registers 05-09 hex

4. Polarity registers read or write are shown in Figure 12.

0x46 🔻	Interrupt	Mack	Outo	ut Config.	Interrupt I	dae	Interrupt Cl	ear	Input Sta	tus Pin (Config.	Debounce
	Input	Outpu	and the second second	Polarity	Port Config.	-	Strength		out Latch	PU/PD Ena		PU/PD Select
Auto Write On			Polarity									
Write All			00	00	00	00	00	0				
WITE AU			0x0A	0x0B	0x0C	0x0D	0x0E	3				
			0.7	□ 1.7	E 2.7	□ 3.7						
Read All			0.6	1.6	2.6	3.6						
			0.5	1.5	E 2.5	□ 3.5 □ 3.4						
			0.3	□ 1.3	2.4	3.3						
			0.2	□ 1.2	□ 2.2	□ 3.2						
			0.1	E 1.1	□ 2.1	3.1	□ 4.1					
			0.0	1.0	2.0	3.0	4.0					
					Write							
					Read							

5. Port Configuration registers read or write are shown in Figure 13.

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0x46 🔻	Interrupt	Mask	Output	Config.	Interrupt E	dae	Interrupt C	lear	Input Sta	atus	Pin Config.	Debounce	
	Input	Output		larity	Port Config.		e Strength		out Latch		PD Enable	PU/PD Select	
Auto Write On		1				11					10.2500/2800/08 08		
			figurat		Lee.	Lee.	0.0						
Write All		1.	FF	FF	FF	FF	03	0					
			(0F	0x10	0x11	_0x12	0x13						
			0.7	▼ 1.7	▼ 2.7	♥ 3.7							
Read All			0.6	▼ 1.6	₹ 2.6	♥ 3.6							
			0.5	♥ 1.5	♥ 2.5	▼ 3.5							
			0.4	▼ 1.4	₹ 2.4	♥ 3.4							
			0.3	♥ 1.3	₹ 2.3	♥ 3.3							
			0.2	▼ 1.2 ▼ 1.1	✓ 2.2 ✓ 2.1	✓ 3.2 ✓ 3.1							
			0.0	▼ 1.1	▼ 2.0	▼ 3.0							
			0.0	¥ 1.0		v 5.0	V 4.0						
					Write								
					Read								

Figure 13. Device configuration screen for registers 0F-13 hex

6. Drive strength registers read or write are shown in Figure 14.

0x46 🔻	Interrupt Mask	Output Config.	Interrupt Edge	e Interrupt Clea	ar Input Status	Pin Config. Debounce
Auto Write On	Input Output		Port Config.	Drive Strength	11	PD Enable PU/PD Select
	-Output Drive Str	ength (0x30 - 0x3	38)			
Write All	FF FF	FF FF	FF FF	FF FF	FF	0
	0.7 1.00 💌	1.7 1.00 💌	2.7 1.00 💌	3.7 1.00 💌		
Read All	0.6 1.00 💌	1.6 1.00 💌	2.6 1.00 💌	3.6 1.00 💌		
	0.5 1.00 💌	1.5 1.00 🚬	2.5 1.00 💌	3.5 1.00 💌		
	0.4 1.00 💌	1.4 1.00 💌	2.4 1.00 💌	3.4 1.00 💌		
	0.3 1.00 💌	1.3 1.00 💌	2.3 1.00 💌	3.3 1.00 💌	4.3 1.00 💌	
	0.2 1.00	1.2 1.00 💌	2.2 1.00 💌	3.2 1.00 -	4.2 1.00 💌	
	0.1 1.00 💌	1.1 1.00 💌	2.1 1.00 💌	3.1 1.00 💌	4.1 1.00 🗾	
	0.0 1.00 💌	1.0 1.00 💌	2.0 1.00 🚬	3.0 1.00 -	4.0 1.00	
	on successful	USB-I2C Ha				1000 kHz SPI: 1 MHz

7. Input latch registers read or write are shown in Figure 15.

PCAL6534 demonstration board OM13541

Interrupt Input	Mask Output		Config.	Interrupt	Edao						
Input	Output					Interrupt C	2 · · · ·	Input Sta		Pin Config.	Debounce
	output	Pol	larity	Port Config.	Driv	e Strength	Inp	ut Latch	PU/	PD Enable	PU/PD Select
	10.000	and the second		00	00	00	2				
	1		1				0				
						UX3E					
	E	0.3	□ 1.3	2.3	□ 3.3						
			□ 1.2	2.2	3.2						
		0.0	1.0	2.0	3.0	4.0					
				Write							
				Read							
			Input Lat(00 0x3A 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0	0x3A 0x3B 0.7 1.7 0.6 1.6 0.5 1.5 0.4 1.4 0.3 1.3 0.2 1.2 0.1 1.1	00 00 00 0x3A 0x3B 0x3C 0.7 1.7 2.7 0.6 1.6 2.6 0.5 1.5 2.5 0.4 1.4 2.4 0.3 1.3 2.3 0.1 1.1 2.1 0.0 1.0 2.0	00 00 00 00 00 0x3A 0x3B 0x3C 0x3D 0x3D 0.7 1.7 2.7 3.7 0.6 1.6 2.6 3.6 0.5 1.5 2.5 3.5 0.4 1.4 2.4 3.4 0.3 1.3 2.3 3.3 0.2 1.2 2.2 3.2 0.1 1.1 2.0 3.0	00 00 00 00 00 00 0x3A 0x3B 0x3C 0x3D 0x3E 0.7 1.7 2.7 3.7 0.6 1.6 2.6 3.6 0.5 1.5 2.5 3.5 0.4 1.4 2.4 3.4 0.3 1.3 2.3 3.3 0.2 1.2 2.2 3.2 0.1 1.1 2.0 3.0 4.0	00 00 00 00 00 00 00 0x3A 0x3B 0x3C 0x3C 0x3D 0x3E 0.7 1.7 2.7 3.7 0.6 1.6 2.6 3.6 0.5 1.5 2.5 3.5 0.4 1.4 2.4 3.4 0.3 1.3 2.3 3.3 0.2 1.2 3.1 0.2 1.2 7.2 3.1 4.1 0.0 1.0 2.0 3.0 4.0	00 00<	00 00 00 00 00 00 0x3A 0x3B 0x3C 0x3D 0x3E 0.7 1.7 2.7 3.7 0.6 1.6 2.6 3.6 0.3 1.3 2.5 3.2 0.1 1.1 2.1 3.1 0.0 1.0 2.0 3.0 4.0	00 00 00 00 00 00 00 0x3A 0x3B 0x3C 0x3D 0x3E 0x3E 0.7 1.7 2.7 3.7 0.6 0.6 1.6 2.6 3.6 0.6 1.6 2.6 3.5 3.5 0.4 1.4 2.4 3.4 0.3 1.3 2.3 3.3 0.2 1.2 1.2 1.2 0.1 1.1 2.1 3.1 4.1 0.0 4.0

Figure 15. Device configuration screen for registers 3A-3E hex

8. PU/PD Enable registers read or write are shown in Figure 16.

0x46 🔻	Interrupt	Mask	Outpu	t Config.	Interrupt	Edae	Interrupt Cl	ear	Input Status	Pin Config.	Debounce	
Z Auto Write On	Input	Output		olarity	Port Config.		e Strength		11	U/PD Enable	PU/PD Select	
		-PU	/PD En	and the second se	00	00	00					
Write All			00 x3F 0.7	00 0x40 1.7	00 0x41 2.7	00 0x42 3.7	00 0x43	0				
Read All			0.6 0.5 0.4	□ 1.6 □ 1.5 □ 1.4	2.6 2.5 2.4	□ 3.6 □ 3.5 □ 3.4						
		1	0.3 0.2 0.1 0.0	1.3 1.2 1.1 1.0	2.3 2.2 2.1 2.0	3.3 3.2 3.1 3.0	□ 4.1 □ 4.0					
			0.0	1.0	Write Read		4.0					

9. PU/PD select registers read or write are shown in Figure 17.

PCAL6534 demonstration board OM13541

Device Address 0x46 v									
	Interrupt		Dutput Conf		-	Interrupt Cl			
Auto Write On	Input	Output	Polarity	Port Config	. Dri	ve Strength	Input Latch	PU/PD Enable	PU/PD Select
		-PU/	PD Selection	1					
				F FF	FF	03		0	
Write All		-0x4	14 Ox4		0x47	0x48			
		V ().7 🗸 1	1.7 2.7	₹ 3.7				
Read All		▼ (▼ 3.6				
		V (▼ 3.5				
		V (✓ 3.4				
		V (V (▼ 3.3 ▼ 3.2				
		V (✓ 3.2				
		V (▼ 3.0				
				Write					
				Read					
				Fread	a l				

Figure 17. Device configuration screen for registers 44-48 hex

10. Interrupt mask registers read or write are shown in Figure 18.

0x46 🔻	Input Outpu	ut F	olarity	Port Config.	Driv	e Strength	Inp	ut Latch	PU/PD Enable	PU/PD Select
Auto Write On	Interrupt Mask	Outp	ut Config.	Interrupt	Edge	Interrupt Cl	ear	Input Sta	tus Pin Config.	Debounce
	e e e e e e e e e e e e e e e e e e e	Interrup	and the second se	(married)						
Write All		FF	FF	FF	FF	03	Ø			
		0x49	0x4A	0x4B	0x4C	Ox4D				
1		▼ 0.7 ▼ 0.6	▼ 1.7 ▼ 1.6	✓ 2.7 ✓ 2.6	▼ 3.7 ▼ 3.6					
Read All		V 0.5	▼ 1.5	₹ 2.5	▼ 3.5					
		♥ 0.4	▼ 1.4	₹ 2.4	₹ 3.4					
		V 0.3	▼ 1.3	₹ 2.3	▼ 3.3					
		♥ 0.2	▼ 1.2	₹ 2.2	₹ 3.2					
		✓ 0.1 ✓ 0.0	✓ 1.1✓ 1.0	✓ 2.1 ✓ 2.0	✓ 3.1 ✓ 3.0					
		• 0.0		Write						
				Read						
				Kedu						

11. Output port configuration register read or write is shown in Figure 19.

PCAL6534 demonstration board OM13541

NXP Fm+ Evaluati	on Board - [PC	AL6534 (Jitra low-voltage	translating 34	-bit IO Expander				-	0
File Device Opt	ions Window	Help							\odot	
Device Address										
0x46 -	Input	Output	Polarity	Port Config.	Drive Strengt	h In	put Latch	PU/PD Enable	PU/PD Select	
Auto Write On	Interrupt M	lask	Output Config.	Interrupt E	dge Interrup	t Clear	Input St	atus Pin Config	. Debounce	
Write All Read All		Ou	tput Config 00 0x53 0DEN 0DEN 0DEN 0DEN 0DEN 0DEN 0DEN 0DEN	3 2 1						
			Read							
Transmissi	on successful	_	USB-I2C Ha	dware Detected		_		I2C: 1000 kHz	SPI: 1 MHz	

Figure 19. Device configuration screen for registers 53 hex

12. Interrupt edge registers read or write are shown in Figure 20.

0x46	Input Interrupt	Output Mask C	Polarity utput Config.	Port Config.		Drive Strength Interrupt		put Latch Input Stat	PU/PD E	Enable in Config.	PU/PD Se Debou	
Write All	Interrup	ot Edge (0x:		00 00		00 00		00 00	1	00	0	
	0.7 love	el-triggered			27	level-triggered	37			100		
Read All		el-triggered	1 10 1810 D	and the second sec		level-triggered	and the second					
		el-triggered	ANALYSI CONTRACTOR			level-triggered	and the second second					
		el-triggered		-triggered		level-triggered	-					
						level-triggered	Autora .			3 level-trig	gered 💌	
		el-triggered		-triggered 💌		level-triggered						
						level-triggered						
	0.0 leve	el-triggered	 1.0 level 	-triggered 💌	2.0	level-triggered	3.0	level-trigger	ed 🔽 4.() level-trig	gered 🛓	

13. Interrupt Clear registers write are shown in Figure 21.

PCAL6534 demonstration board OM13541

File Device Op Device Address												
0x46 🔻	Input	Output	Po	olarity	Port Config.	Driv	/e Strength	Inp	ut Latch	PU/PD Enable	PU/PD Select	
Auto Write On	Interrupt	Mask	Outpu	t Config.	Interrupt	Edge	Interrupt Cl	lear	Input Statu	s Pin Config.	Debounce	
		_int	terrupt	Clear 00	00	00	00					
Write All			Ix5E	00 0x5F	00 0x60	0x61	00 0x62	0				
			0.7	1.7	2.7	3.7	0,02					
Read All			0.6	1.7	2.6	3.6						
Kead All			0.5	1.5	2.5	3.5						
			0.4	1.4	2.4	1 3.4						
			0.3	1.3	2.3	3.3						
			0.2	1.2	2.2	3.2	- 4.1					
			0.0	1.0	2.1	3.0	- 4.0					
					Write							
					write							

Figure 21. Device configuration screen for registers 5E-62 hex

14. Input status registers read are shown in Figure 22.

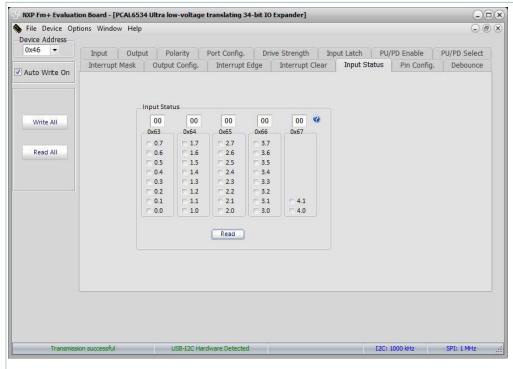


Figure 22. Device configuration screen for registers 63-67 hex

15.Pin Configuration registers read or write are shown in Figure 23.

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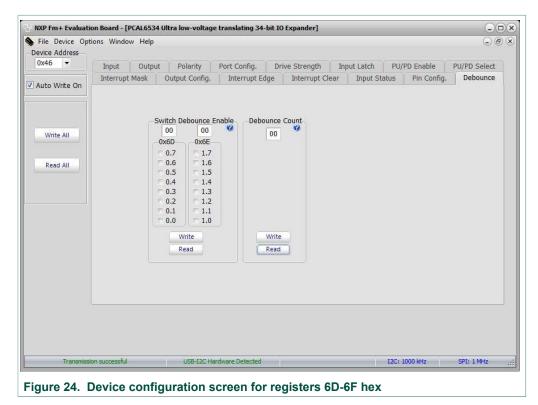
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Device Address											
OXTO T	Input Outp		olarity	Port Config.		e Strength			PD Enable	PU/PD Select	
Auto Write On	Interrupt Mask	Outpu	t Config.	Interrupt	Edge	Interrupt	Clear	Input Status	Pin Config.	Debounce	
		* 1 1									
		Individua 00	Pin Outpu	of Config.	00	00	0				
Write All		0x68	0x69	0x6A	0x6B	0x6C					
		0.7	1.7	2.7	3.7	UNUC					
Read All		0.6	□ 1.6	2.6	3.6						
		0.5	□ 1.5	2.5	3.5						
		0.4	□ 1.4	2.4	3.4						
		0.3	□ 1.3 □ 1.2	2.3	3.3						
		0.2	1.2	2.2	3.1	4.1					
		0.0	1.0	2.0	3.0	4.0					
				Write							
				Read							

Figure 23. Device configuration screen for registers 68-6C hex

16. Debounce registers read or write are shown in Figure 24.



7 Support

For support, please send an E-mail to: <u>i2c.support@nxp.com</u>

8 Abbreviations

Table 5. Abbrevi	iations
Acronym	Description
ESD	Electro Static Discharge
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
I ² C-bus	Inter-integrated Circuit bus
LED	Light Emitting Diode
PC	Personal Computer
РСВ	Printed-Circuit Board
SMBus	System Management Bus
USB	Universal Serial Bus

9 References

- 1. PCAL6534, Ultra low-voltage translating 34-bit Fm+ I²C-bus/SMBus I/O expander; Product data sheet; NXP Semiconductors
- 2. UM10741, Fm+ Development Kit OM13320 User manual; NXP Semiconductors

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