

N-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{(BR)DSS} (V)	$r_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ)	
150	0.018 at V _{GS} = 10 V	90 ^d	64	

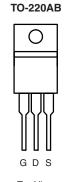
FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- 100 % R_g and UIS Tested



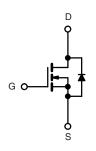
APPLICATIONS

- · Primary Side Switch
- Industrial



Top View

Ordering Information: SUP90N15-18P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_C = 25 ^{\circ}C$, unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	150	V		
Gate-Source Voltage		V _{GS}	± 20	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
Continuous Drain Current (T _{.I} = 175 °C)	T _C = 25 °C	I-	90 ^d		
Continuous Diain Current (1j = 175 C)	T _C = 70 °C	I _D	75	A	
Pulsed Drain Current		I _{DM}	180	A .	
Avalanche Current	I _{AS}	50			
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	125	mJ	
	T _C = 25 °C	В	375 ^b	14/	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	P _D	3.75	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)	R _{thJC}	0.4		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).
- d. Package limited.

SUP90N15-18P

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SPECIFICATIONS $T_J = 25^{\circ}$	C, unless o	therwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	150			V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA	
Zero Gate Voltage Drain Current		$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ	
	I _{DSS}	$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50		
		V _{DS} = 150 V, V _{GS} = 0 V, T _J = 150 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	120			Α	
	r	V _{GS} = 10 V, I _D = 20 A		0.0145	0.018	0	
Drain-Source On-State Resistance ^a	^r DS(on)	V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.029	0.036	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		55		S	
Dynamic ^b							
Input Capacitance	C _{iss}			4180		pF	
Output Capacitance	C _{oss}	V _{GS} = 0 V, V _{DS} = 75 V, f = 1 MHz		235			
Reverse Transfer Capacitance	C _{rss}			83			
Total Gate Charge ^c	Q_g			64	100	nC	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 85 \text{ A}$		23			
Gate-Drain Charge ^c	Q _{gd}			16			
Gate Resistance	R_{g}	f = 1 MHz		2.1	4.2	Ω	
Turn-On Delay Time ^c	t _{d(on)}			15	25		
Rise Time ^c	t _r	$V_{DD} = 75 \text{ V}, R_{L} = 0.88 \Omega$		10	15	- ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 85 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	40		
Fall Time ^c	t _f			8	15		
Source-Drain Diode Ratings and Ch	aracteristics 7	Γ _C = 25 °C ^b					
Continuous Current	Is				90	_	
Pulsed Current	I _{SM}				180	Α	
Forward Voltage ^a	V_{SD}	I _F = 30 A, V _{GS} = 0 V		1.0	1.5	٧	
Reverse Recovery Time	t _{rr}	I _F = 50 A, di/dt = 100 A/μs		130	200	ns	
Peak Reverse Recovery Current	I _{RM(REC)}			8	12	Α	
Reverse Recovery Charge	Q _{rr}			0.52	1.2	μC	

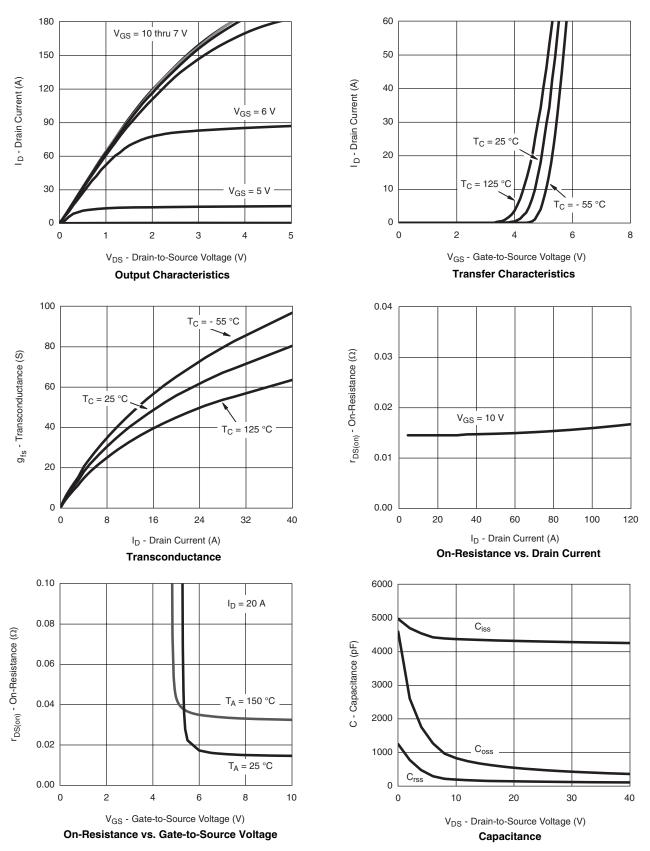
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



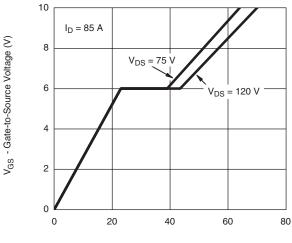
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



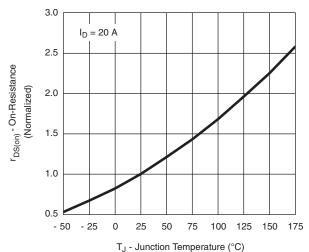
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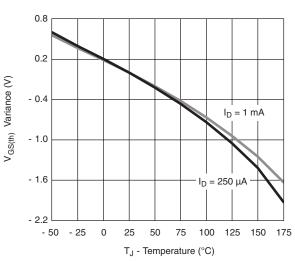
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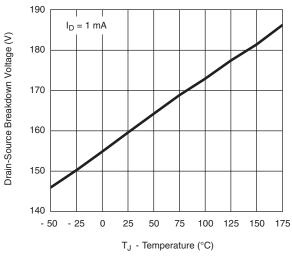
 Q_g - Total Gate Charge (nC) $\label{eq:qg} \textbf{Gate Charge}$



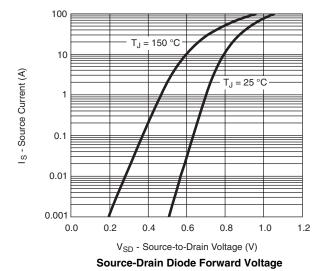
On-Resistance vs. Junction Temperature

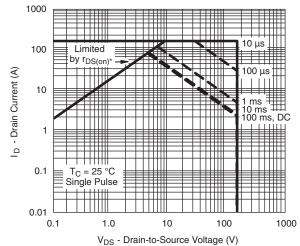


Threshold Voltage



Drain-Source Breakdown vs. Junction Temperature

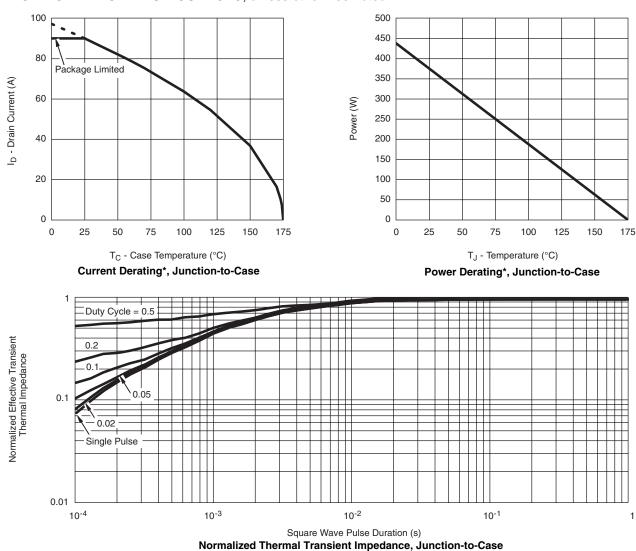




 * V_{GS} > minimum V_{GS} at which r_{DS(on)} is specified **Safe Operating Area, Junction-to-Case**



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



^{*} The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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