- **Two 16-Bit Analog-to-Digital Converters (ADC)**
- **Two 16-Bit Digital-to-Analog Converters (DAC)**
- **Programmable Input/Output Gain**
- **Analog Crosspoint to Connect the Two Coder/Decoders (Codecs) to Any of the I/O Ports. Controlled Through the Serial Port or the I^2C Bus**
- **8-Bit A-Law/μ-Law Companded Data or 16-Bit Linear Data Complying With G.711 Standard**
- **Programmable ADC and DAC Conversion Rate**
- **Typical 77-dB Signal-to-Noise + Distortion for ADC**
- **Typical 78-dB Signal-to-Noise + Distortion for the DAC**
- **Typical 80-dB Dynamic Range**
- **All Typical Sampling Rates, Such as 7.2, 8, 8.229, 9.6, 10.285, 12, 14.4, and 16 kHz Supported**
- **Preamplifiers for Microphone, Handset, Headset, and Speaker Phone Gain Selectable Via the Serial Port or I^2C Bus**
- **2.5-V Microphone Bias Voltage**
- **Seamless Interface to a Single Multichannel Buffered Serial Port (McBSP) of a C54x or a C6x DSP**
- **Four TLV320AIC22 ICs Can Be Cascaded Together to Allow up to Eight Channels**
- **2s-Complement Data Format**
- **Differential Outputs**
- **Typical Low Crosstalk < –85 dB (Interchannel)**
- **Hardware/Software Power Down**
- **Independent Power Down for Drivers**
- **Single 3.3-V Supply Operation**
- **120-mW Typical Power Consumption**
- **Packaged in 48-Pin Low-Profile Quad Flatpack (LQFP) Package**

description

The TLV320AIC22 is a dual coder/decoder (codec) for voice applications, including voice-over-internet protocol (VOIP). It features two ADC conversion channels and two DAC conversion channels that can be connected to a handset, headset, speaker, microphone, or a subscriber line via an analog crosspoint.

The TLV320AIC22 has a flexible serial interface that allows the two channels of the TLV320AIC22 to be interfaced to a single multichannel buffered serial port (McBSP) of the DSP. The two channels share the digital interface at different time slots. Up to four TLV320AIC22 units can be cascaded together to allow eight channels. For control purposes, either the serial interface or the I^2C interface can be used. Programmable gain amplifiers, preamplifier gain, microphone bias voltages, and analog crosspoint are programmed through the serial interface or the I^2C interface. The TLV320AIC22 can be powered down, via a dedicated pin or by using software control, to reduce power dissipation.

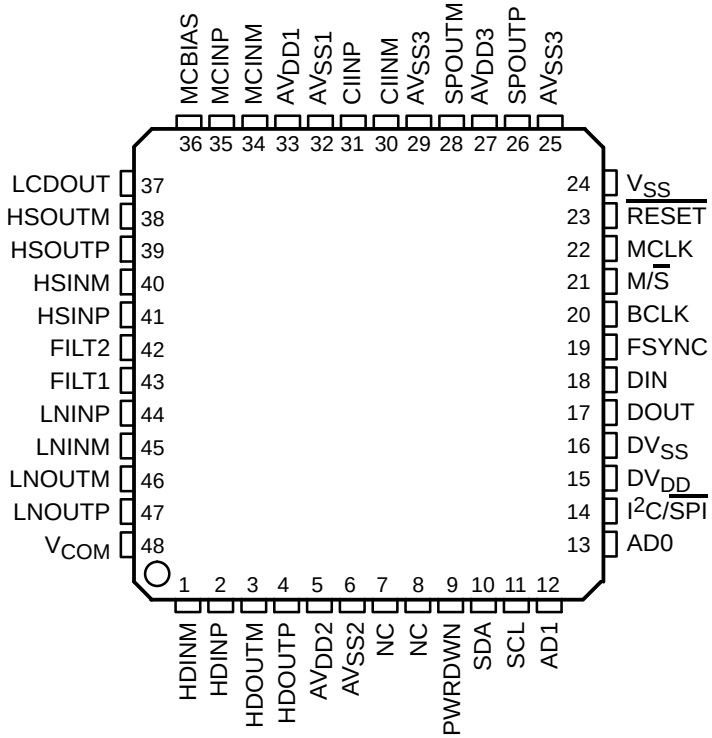
The TLV320AIC22 is available in a 48-pin LQFP package and is characterized for operation from –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE
	PLASTIC QUAD FLATPACK (PT)
–40°C to 85°C	TLV320AIC22PT

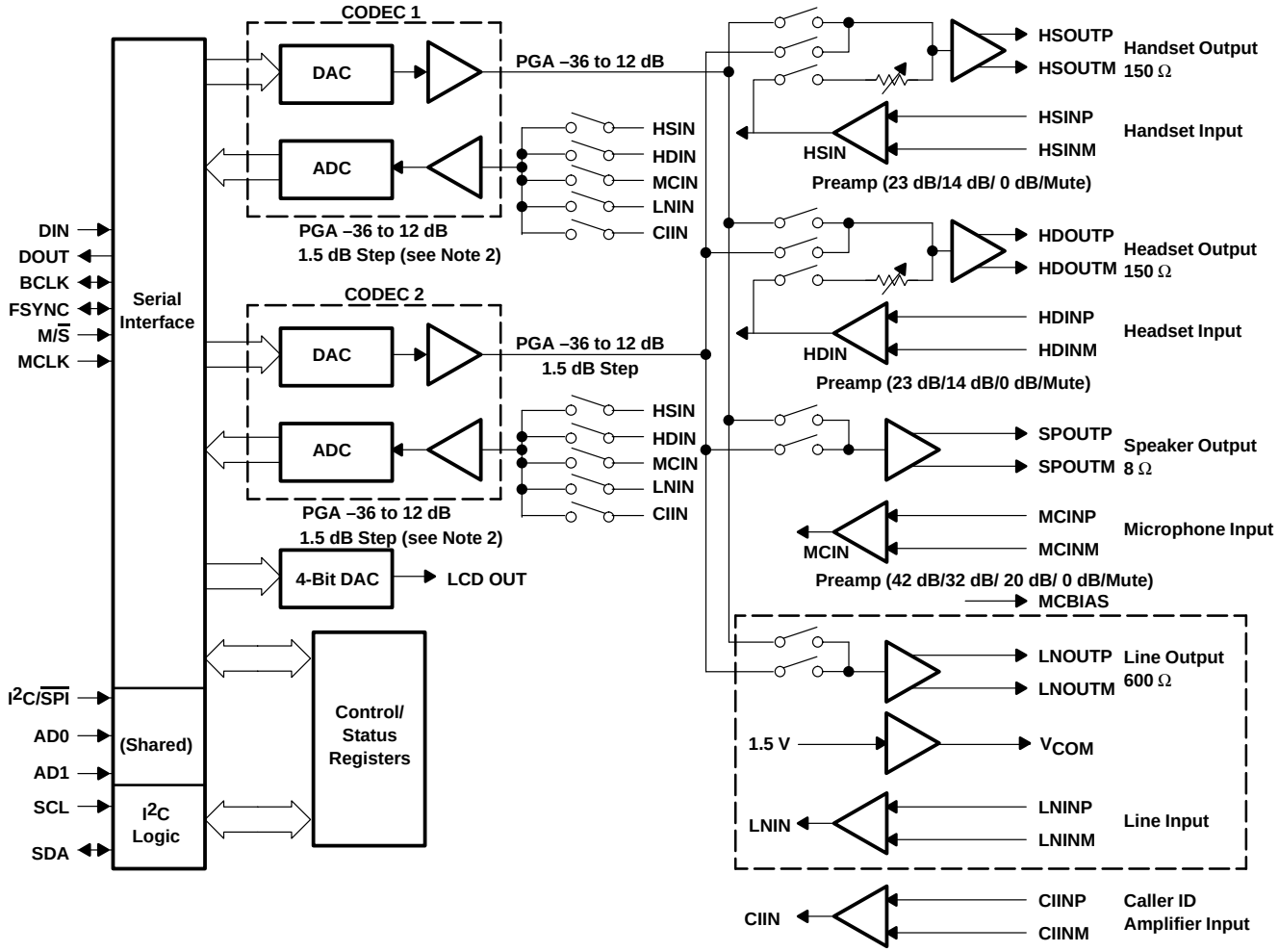
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PT PACKAGE
(TOP VIEW)



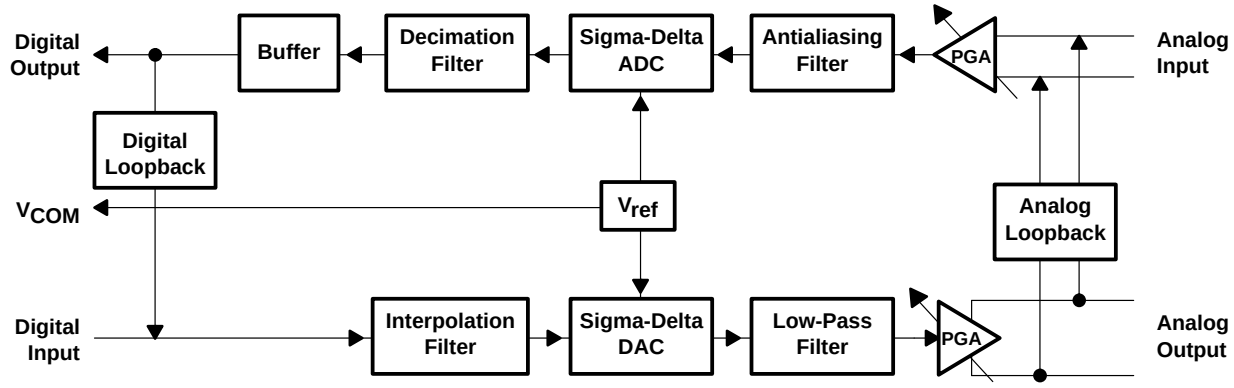
NC – No internal connection

functional block diagram



NOTES: 1. Input and output analog signals are differential. All switches are register controlled.
2. The attenuation on the ADC PGA (12 dB to –36 dB) is done after the ADC. This attenuation cannot prevent clipping. To prevent clipping, both the gain of the preamp and the PGA should be lowered to the required value.

functional block diagram (one of two codecs shown)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AD1	12	I	In I^2C mode, AD1 is used with AD0 to form the lower two bits of the 7-bit I^2C chip address. The upper five bits are fixed at 11100. AD1 also is used in conjunction with AD0 to assign the two time slots for the codec in serial-port mode. AD1 is the MSB.
AD0	13	I	In I^2C mode, AD0 is used with AD1 to form the lower two bits of the 7-bit I^2C chip address. The upper five bits are fixed at 11100. AD0 also is used in conjunction with AD1 to assign the two time slots for the codec in serial-port mode. AD0 is the LSB.
AV_{DD1}	33	I	Analog power supply. Connect to AV_{DD2}. See Note 3
AV_{DD2}	5	I	Analog power supply. Connect to AV_{DD1}. See Note 3
AV_{DD3}	27	I	Analog power supply for 8-Ω speaker driver. This pin can be connected to AV_{DD1} and AV_{DD2}. Because this signal requires large amounts of current, it is recommended that a separate PCB trace be run to this pin and connected to the main supply at the power-supply connection to the PC board. See Note 3
AV_{SS1}	32	I	Analog ground. Connect to AV_{SS2}. See Note 3
AV_{SS2}	6	I	Analog ground. Connect to AV_{SS1}. See Note 3
AV_{SS3}	25, 29	I	Analog ground for 8-Ω speaker driver. These pins can be connected to AV_{SS1} and AV_{SS2}. Because this signal requires large amounts of current, it is recommended that a separate PCB trace be run to this pin and connected to the main supply at the power-supply connection to the PC board. See Note 3
BCLK	20	I/O	Bit clock. BCLK clocks serial data into DIN and out of DOUT. When configured as an output (master mode), BCLK is generated internally by multiplying the frame-sync signal frequency by 256. When configured as an input (slave mode), BCLK is an input and must be synchronous with the master clock and frame sync.
CIINM	30	I	CallerID amplifier analog inverting input
CIINP	31	I	CallerID amplifier analog noninverting input
DIN	18	I	Data input. DIN receives the DAC input data and register data from the external digital signal processor (DSP) or controller and is synchronized to BCLK. Data is latched on the falling edge of BCLK in the two time slots that are specified by the AD1 and AD0 bits. Codec 1 receives data in the first assigned time slot, followed by codec 2 receiving data in the second assigned time slot.
DOUT	17	O	Data output. DOUT transmits the ADC output bits and the register data. It is synchronized to BCLK. Data is transmitted on the rising edge of BCLK in the two time slots that are specified by the AD1 and AD0 bits. DOUT is at high impedance during time slots not assigned to the codec. Codec 1 transmits data in the first assigned time slot, followed by codec 2 in the second assigned time slot.
DV_{DD}	15	I	Digital power supply. See Note 3
DV_{SS}	16	I	Digital ground. See Note 3
FILT1	43	O	Reference filter node. FILT1 and FILT2 provide decoupling of the reference voltage. This reference is 2.25 V. The optimal capacitor value is 0.1 μF (ceramic) and is connected between FILT1 and FILT2. FILT1 should not be used as a voltage source.
FILT2	42	O	Reference filter node. FILT1 and FILT2 provide decoupling of the reference voltage. This reference is 0 V. The optimal capacitor value is 0.1 μF (ceramic) and is connected between FILT1 and FILT2.
FSYNC	19	I/O	Frame sync. FSYNC indicates the beginning of a frame and the start of time slot 0. When FSYNC is sampled high on the rising edge of BCLK, the codec receives or transmits data in its specified time slot (specified by AD0 and AD1) in the frame. FSYNC is generated by the master device (output) and is an input to the slave devices. Codec 1 communicates in the first assigned time slot, followed by codec 2 communicating in the second assigned time slot.
HDINM	1	I	Headset amplifier analog inverting input. A connection between HDIN and HDOUT occurs, with selected echo gain, unless the echo gain is muted. See register 14
HDINP	2	I	Headset amplifier analog noninverting input
HDOUTM	3	O	Inverting headset output. The HDOUTM pin, together with the HDOUTP pin, forms the differential output. With HDOUTP, a 150-Ω load can be driven, differentially. HDOUTM also can be used alone for single-ended operation.
HDOUTP	4	O	Noninverting headset output. HDOUTP can be used alone for single-ended operation. With HDOUTM, a 150-Ω load can be driven, differentially.

NOTE 3: This device has separate analog and digital power and ground pins. For best operation and results, the PC board design should utilize separate analog and digital power supplies as well as separate analog and digital ground planes. Mixed-signal design practices should be used.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
HSINM	40	I	Handset amplifier analog inverting input. A connection between HSIN and HSOUT occurs, with selected echo gain, unless the echo gain is muted. See register 13.
HSINP	41	I	Handset amplifier analog noninverting input. A connection between the HSIN and HSOUT occurs, with programmed echo gain, unless the echo gain is muted. See register 13.
HSOUTM	38	O	Inverting handset output. The HSOUTM pin, together with the HSOUTP pin forms the differential output. With HSOUTP, a 150-Ω load can be driven differentially. HSOUTM also can be used alone for single-ended operation.
HSOUTP	39	O	Noninverting handset output. With HSOUTM, a 150-Ω load can be driven, differentially. HSOUTP also can be used alone for single-ended operation.
$I^2C/\overline{SPI}$	14	I	I^2C/serial port interface select. Setting this pin high allows the user to program the registers using the I^2C interface. A low state configures the serial interface to be used for control register programming during normal data transmission using time slots 0 and 1. When set high (I^2C interface selected) time slots 0 and 1 in the normal data transmission are ignored.
LCDOUT	37	O	4-bit DAC output voltage, programmed through the control interface. This can be used to provide the bias voltage for an LCD display.
LNINP	44	I	Line-port amplifier analog noninverting input. See Note 4.
LNINM	45	I	Line-port amplifier analog inverting input. See Note 4.
LNOUTM	46	O	Inverting line-port output. The LNOUTM pin, together with the LNOUTP pin, forms the differential output. With LNOUTP, a 600-Ω load can be driven differentially. LNOUTM also can be used alone for single-ended operation. See Note 4.
LNOUTP	47	O	Noninverting line-port output. With LNOUTM, a 600-Ω load can be driven, differentially. LNOUTP also can be used alone for single-ended operation. See Note 4.
MCLK	22	I	Master clock input. All internal clocks are derived from this clock. This clock typically is 32.768 MHz or 24.576 MHz.
MCBIAS	36	O	MCBIAS provides a bias voltage and current to operate Electret microphones. The bias voltage is specified across the microphone at 2.5 V.
MCINM	34	I	Microphone amplifier analog inverting input
MCINP	35	I	Microphone amplifier analog noninverting input
$M/\overline{S}$	21	I	Master/slave select input. When $M/\overline{S}$ is high, the device is the master, and when it is low, it is a slave.
PWRDWN	9	I	Power down. PWRDWN is active high. When PWRDWN is pulled high, the device goes into a power-down mode, and the output drivers and most of the high-speed clocks are disabled. The serial interface and I^2C interface are enabled. However, all register values are sustained and the device resumes full-power operation without reinitialization when PWRDWN is pulled low again. PWRDWN resets the counters only and preserves the programmed register contents.
$\overline{RESET}$	23	I	Codec device reset. $\overline{RESET}$ initializes all device internal registers to default values. This signal is active low.
SCL	11	I	SCL is the serial control interface clock for the I^2C interface, and is used to clock control bits into and out of the device through the SDA pin. Tie this pin to DV_{DD} when not used.
SDA	10	I/O	Bidirectional control data I/O line for the I^2C interface. Data is clocked into and out of the device by SCL. Tie this pin to DV_{DD} when not used.
SPOUTP	26	O	Inverting analog output from 8-Ω speaker amplifier
SPOUTM	28	O	Noninverting analog output from 8-Ω speaker amplifier
NC	7, 8		Reserved. Leave unconnected.
V_{COM}	48	O	V_{COM} provides a reference voltage of 1.5 V. The maximum source or sink current at this terminal is 2.5 mA.
V_{SS}	24	I	Internal substrate connection. V_{SS} should be tied to AV_{SS1} and AV_{SS2}. See Note 3.

NOTES: 3. This device has separate analog and digital power and ground pins. For best operation and results, the PC board design should utilize separate analog and digital power supplies as well as separate analog and digital ground planes. Mixed-signal design practices should be used.

4. The LNINP and LNINM are sensitive to crosstalk from LNOUTP and LNOUTM. Keep the LNOUT and LNIN signals separated on the printed circuit board. Do not route the LNOUT signals parallel to the LNIN signals.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AV_{DD1}, AV_{DD2}, AV_{DD3} to AV_{SS1}, AV_{SS2}, AV_{SS3}, AV_{SS}, DV_{DD} to DV_{SS} . . . –0.3 V to 4.5 V
Analog input voltage range to AV_{SS1}, AV_{SS2}, and AV_{SS3} . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD} (3.3-V supply)		3	3.3	3.6	V
Analog signal peak-to-peak input voltage, $V_{I(analog)}$ differential (LNINP, LNINM, CIINP, CIINM)	Preamplifier gain set to 0 dB			4	V
Analog signal peak-to-peak input voltage, $V_{I(analog)}$, differential (HSINP, HSINM, HDINP, HDINM, MCINP, MCINM)	Preamplifier gain set to 0 dB			4 (scaled by the selected gain)	V
High-level input voltage, any digital input, V_{IH}		2			V
Low-level input voltage, any digital input. V_{IL}				0.8	V
Differential output load resistance, R_L (LNOUTP, LNOUTM)			600		Ω
Differential output load resistance, R_L (SPOUTP, SPOUTM)		8			Ω
Differential output load resistance, R_L (HDOUTP, HDOUTM)		150			Ω
Differential output load resistance, R_L (HSOUTP, HSOUTM)		150			Ω
Input resistance connected externally to hybrid amps (LNINP, LNINM)			68		kΩ
Master clock input				32.768	MHz
Load capacitance, C_L (unless otherwise specified)				20	pF
ADC or DAC conversion rate		7.2		16	kHz
Operating free-air temperature, T_A		–40		85	°C

electrical characteristics over recommended operating free-air temperature range, DV_{DD} = 3.3 V, AV_{DD1} = AV_{DD2} = AV_{DD3} = 3.3 V (unless otherwise noted)

digital inputs and outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, any digital output	I_{OH} = –360 µA	2.4			V
V_{OL}	Low-level output voltage, any digital output	I_{OL} = 2 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 3.3 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.6 V			10	µA
C_I	Input capacitance, any digital input			5		pF
C_O	Output capacitance, any digital output			10		pF
I_{lkg1}	Input leakage current, any digital input (except for DIN)				10	µA
I_{lkg2}	Input leakage current, DIN	V_{IH}= 3.3 V			10	µA
		V_{IL} = 0.6 V			–60	µA
I_{OZ}	Output leakage current, any digital output				10	µA

ADC channel transfer response characteristics over recommended ranges of supply voltage and operating free-air temperature, when selecting handset or headset as input

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	–17 dBr input signal, preamp gain = 14 dB, HSIN or HDIN selected, PGA gain = 0 dB (seen Note 5 and Note 6), Sampling rate = 8 kHz	0 Hz to 60 Hz			–26	dB
		200 Hz	–1.8		0.35	
		300 Hz to 3 kHz	–0.3		0.3	
		3.3 kHz	–0.4		0.2	
		3.4 kHz	–1		–0.1	
		4 kHz			–12.5	
		4.6 kHz to 8 kHz			–60	
		Above 8 kHz			–70	
	–24 dBr input signal, preamp gain = 14 dB, HSIN or HDIN selected, PGA gain = 0 dB (seen Note 5 and Note 7), Sampling rate = 16 kHz	0 Hz to 120 Hz			–26	dB
		400 Hz	–1.8		0.35	
		600 Hz to 6 kHz	–0.3		0.3	
		6.6 kHz	–0.4		0.2	
		6.8 kHz	–1		–0.1	
		8 kHz			–12.5	
		9.2 kHz to 16 kHz			–60	
		Above 16 kHz			–56	

NOTES: 5. The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dBr = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal.
6. When the high-pass filter is bypassed, the passband is 0 Hz to 3 kHz. When the high-pass filter is inserted, the passband is 300 Hz to 3 kHz.
7. When the high-pass filter is bypassed, the passband is 0 Hz to 6 kHz. When the high-pass filter is inserted, the passband is 600 Hz to 6 kHz.

ADC channel passband frequency characteristics with microphone selected as input

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz (see Note 6)	–35 dBr input signal, preamp gain = 32 dB, MICIN selected. PGA gain = 0 dB (see Note 5), Sampling rate = 8 kHz	300 Hz to 3 kHz	–0.3		0.3	dB
		3.3 kHz	–0.4		0.2	
		3.4 kHz	–1		–0.1	
Gain relative to gain at 1.02 kHz (see Note 7)	–38 dBr input signal, preamp gain = 32 dB, MICIN selected. PGA gain = 0 dB (see Note 5), Sampling rate = 16 kHz	600 Hz to 6 kHz	–0.3		0.3	dB
		6.6 kHz	–0.5		0.2	
		6.8 kHz	–1.1		–0.1	

NOTES: 5. The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dBr = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal.
6. When the high-pass filter is bypassed, the passband is 0 Hz to 3 kHz. When the high-pass filter is inserted, the passband is 300 Hz to 3 kHz.
7. When the high-pass filter is bypassed, the passband is 0 Hz to 6 kHz. When the high-pass filter is inserted, the passband is 600 Hz to 6 kHz.

ADC channel passband frequency characteristics with line input selected

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz (see Note 6)	–10 dBr input signal, LNIN selected, PGA gain = 0 dB (see Note 5) Sampling rate = 8 kHz Pole select = 64, 32, 21.3, or 16 kHz	300 Hz to 3 kHz	–0.3		0.3	dB
		3.3 kHz	–0.4		0.2	
		3.4 kHz	–1		–0.1	
Gain relative to gain at 1.02 kHz (see Note 7)	–9 dBr input signal, LNIN selected, PGA gain = 0 dB (see Note 5) Sampling rate = 16 kHz Pole select = 64, 32, or 21.3 kHz	600 Hz to 6 kHz	–0.7		0.3	dB
		6.6 kHz	–0.9		0.2	
		6.8 kHz	–1.5		–0.1	
	–21 dBr input signal, LNIN selected, PGA gain = 0 dB (see Note 5) Sampling rate = 16 kHz Pole select = 16 kHz	600 Hz to 6 kHz	–0.9		0.3	dB
		6.6 kHz	–1.5		0.15	
		6.8 kHz	–2.5		0	

NOTES: 5. The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dBr = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal.
6. When the high-pass filter is bypassed, the passband is 0 Hz to 3 kHz. When the high-pass filter is inserted, the passband is 300 Hz to 3 kHz.
7. When the high-pass filter is bypassed, the passband is 0 kHz to 6 kHz. When the high-pass filter is inserted, the passband is 600 Hz to 6 kHz.

ADC dynamic performance characteristics (see Note 5 and Note 8)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC dynamic performance with line input selected	V_I = –3 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz	THD			–72	dB
		SNR			–70	
		THD+N			–68	
	V_I = –9 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz	THD			–72	dB
		SNR			–70	
		THD+N			–68	
	V_I = –40 dBr, PGA Gain = 0 dB, Sampling rate = 8 kHz	THD			–45	dB
		SNR			–40	
		THD+N			–38	
ADC dynamic performance with microphone input selected	V_I = –35 dBr, Preamp gain = 32 dB, PGA gain = 0 dB, Sampling rate = 16 kHz (–3 dBr at ADC input)	THD			–72	dB
		SNR			–70	
		THD+N			–68	
	V_I = –41 dBr, Preamp gain = 32 dB, PGA gain = 0 dB, Sampling rate = 16 kHz (–9 dBr at ADC input)	THD			–70	dB
		SNR			–68	
		THD+N			–65	
	V_I = –45 dBr, Preamp gain = 42 dB, PGA gain = 0 dB, Sampling rate = 16 kHz (–3 dBr at ADC input)	THD			–70	dB
		SNR			–62	
		THD+N			–60	

NOTES: 5. The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dBr = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal.
8. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.5 V.

ADC dynamic performance characteristics (see Note 5 and Note 8) (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC dynamic performance with caller ID input selected	V_I = –9 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz	THD			–68	dB
		SNR			–66	
		THD+N			–65	
	V_I = –40 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz	THD			–45	dB
		SNR			–40	
		THD+N			–38	
ADC dynamic performance with handset or headset selected	V_I = –3 dBr, PGA gain = 0 dB, Preamp gain = 0 dB Sampling rate = 16 kHz	THD			–72	dB
		SNR			–70	
		THD+N			–68	
	V_I = –9 dBr, PGA gain = 0 dB, Preamp gain = 0 dB Sampling rate = 16 kHz	THD			–72	dB
		SNR			–70	
		THD+N			–68	
	V_I = –40 dBr, PGA gain = 0 dB, Preamp gain = 0 dB Sampling rate = 16 kHz	THD			–50	dB
		SNR			–42	
		THD+N			–40	

NOTES: 5. The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dBr = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal.
8. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.5 V.

ADC characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Peak-input voltage, differential	Preamp gain = 0 dB			4	V
	Dynamic range			82		dB
	Intrachannel isolation (measured at ADC output)	HSIN is selected for ADC input. Ground the input to the ADC; full-scale input applied to DAC.	85			dB
E_G	Gain error (valid for HSIN, HDIN, and MCIN)	V_I = –1 dB at 1020 kHz	–1		1	dB
	Gain error (valid for LNIN)			±2.5		dB
$E_{O(ADC)}$	ADC channel offset error	HSIN selected for ADC input, preamp gain = 14 dB, 0-V differential input signal, inputs are ac coupled			50	mV
CMRR	Common-mode rejection ratio	HSIN selected for ADC input, preamp gain = 14 dB, 0-V differential input signal, common mode signal of –10 dB applied	50	65		dB
	Idle channel noise	HSIN selected for ADC input, preamp gain = 14 dB, 0-V differential input signal, inputs are ac coupled		30	75	μV rms
	Channel delay (high-pass filter bypassed)			$14/f_S$		s

callerID frequency response characteristics (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{co(L)}$	Low-cutoff frequency	Connected as shown in Figure 23		570		Hz
A_p	Passband gain at 2 kHz			1.5		dB
	Attenuation from input to IC pin at 60 Hz			–44		dB

NOTE 9: All values are applicable when used with external components as shown in Figure 23.

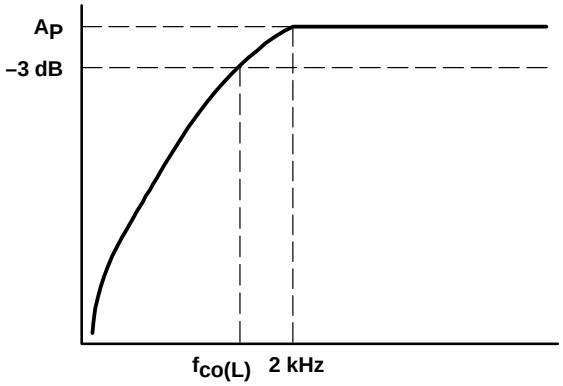


Figure 1. CallerID Frequency Response

DAC dynamic performance characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC dynamic performance with handset or headset drivers (HSOUT or HDOUT)	V_I = –3 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz, See Note 10	THD			–72	dB
		SNR			–70	
		THD+N			–65	
	V_I = –9 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz, See Note 10	THD			–63	dB
		SNR			–70	
		THD+N			–60	
	V_I = –40 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz, See Note 10	THD			–45	dB
		SNR			–40	
		THD+N			–38	
DAC dynamic performance with 8-Ω driver (SPOUT)	V_I = –3 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 12	THD			–62	dB
		SNR			–75	
		THD+N			–60	
	V_I = –9 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 12	THD			–60	dB
		SNR			–70	
		THD+N			–55	
	V_I = –40 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 12	THD			–38	dB
		SNR			–35	
		THD+N			–32	

NOTES: 10. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dBr). A 0 dBr or full-scale digital input results in a 4-$V_{(P-P)}$ differential output.

12. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dBr). A 0 dBr or full-scale digital input results in a 5-$V_{(P-P)}$ differential output.

DAC dynamic performance characteristics (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC dynamic performance with line-output driver (LNOUT), 16-kHz pole selected, 1000-Hz input signal	V_I = –3 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 10	THD			–72	dB
		SNR			–73	
		THD+N			–70	
	V_I = –10 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 10	THD			–72	dB
		SNR			–73	
		THD+N			–70	
	V_I = –40 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 10	THD			–50	dB
		SNR			–40	
		THD+N			–38	
DAC dynamic performance with line-output driver (LNOUT), 64-kHz pole selected, 1000-Hz input signal	V_I = –3 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 10	THD			–72	dB
		SNR			–73	
		THD+N			–70	
	V_I = –10 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 10	THD			–72	dB
		SNR			–73	
		THD+N			–70	
	V_I = –40 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, See Note 10	THD			–50	dB
		SNR			–40	
		THD+N			–38	

NOTES: 10. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dBr). A 0 dBr or full-scale digital input results in a 4-$V_{(P-P)}$ differential output.

DAC channel transfer response characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 10 and Note 11), with DAC connected to handset (HSOUT) or headset (HDOUT) drivers

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at DIN is 0 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz	0 Hz to 3 kHz	–0.3		0.3	dB
		3.3 kHz	–0.5		0.1	
		3.4 kHz	–1		–0.1	
		4 kHz			–12.5	
		4.6 kHz, and above			–40	
	Input signal at DIN is 0 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz	0 Hz to 6 kHz	–0.3		0.3	dB
		6.6 kHz	–0.5		0.1	
		6.8 kHz	–1		–0.1	
		8 kHz			–12.5	
		9.2 kHz, and above			–40	

NOTES: 10. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dBr). A 0 dBr or full-scale digital input results in a 4-$V_{(P-P)}$ differential output.
11. The filter gain is measured with respect to the gain at 1020 Hz.

DAC channel passband frequency characteristics with DAC connected to 8-Ω speaker driver (SPOUT) (see Note 11 and Note 12)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at DIN is 0 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz	0 Hz to 3 kHz	–0.2		0.4	dB
		3.3 kHz	–0.4		0.2	
		3.4 kHz	–1.5		–0.1	
	Input signal at DIN is 0 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz	0 Hz to 6 kHz	–0.2		0.4	dB
		6.6 kHz	–0.5		0.2	
		6.8 kHz	–1.5		–0.1	

NOTES: 11. The filter gain is measured with respect to the gain at 1020 Hz.
12. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dBr). A 0 dBr or full-scale digital input results in a 5-$V_{(P-P)}$ differential output.

DAC channel passband frequency characteristics with DAC connected to line output driver (LNOUT) (see Note 10 and Note 11)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at DIN is 0 dBr, PGA gain = 0 dB, Sampling rate = 8 kHz, Pole select = 64, 32, 21.3, or 16 kHz	0 Hz to 3 kHz	–0.2		0.4	dB
		3.3 kHz	–0.4		0.2	
		3.4 kHz	–1		–0.1	
		4 kHz			–12.5	
		Above 4.6 kHz			–40	
	Input signal at DIN is 0 dBr, PGA gain = 0 dB, Sampling rate = 16 kHz, Pole select = 64, 32, 21.3, or 16 kHz	0 Hz to 6 kHz	–0.2		0.4	dB
		6.6 kHz	–0.4		0.2	
		6.8 kHz	–1		–0.3	
		8 kHz			–12.5	
		Above 9.2 kHz			–40	

NOTES: 10. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dBr). A 0 dBr or full-scale digital input results in a 4-$V_{(P-P)}$ differential output.
11. The filter gain is measured with respect to the gain at 1020 Hz.

line output out-of-band performance characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Line output out-of-band performance	Noise measured in 1-kHz bandwidth from 4.6 kHz to 300 kHz; –10-dB input signal; PGA gain is 0 dB; output load = 600 Ω.	Pole select = 64 kHz		32		$\mu V/\sqrt{Hz}$
		Pole select = 32 kHz		20		
		Pole select = 21.3 kHz		14		
		Pole select = 16 kHz		11		

DAC characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			82		dB
	Intrachannel isolation (measured at SPOUT)	All zeros applied to DAC. Full-scale signal applied to ADC at HSIN.	85			dB
E_G	Gain error, 0 dB	V_I = –1 dB at 1020 kHz	–1		1	dB
	Idle channel noise	0 kHz to 4 kHz, See Note 12		30	75	μV rms
	Channel delay			$13/f_S$		s
V_O	Analog output voltage, (SPOUTP–SPOUTM)	Differential for full-scale digital input; See Note 13 and Note 14.		±2.5		$V_{(P–P)}$
	Analog output voltage (handset/headset and line interfaces)	Differential for full-scale digital input; See Note 13 and Note 14.		±2		

NOTES: 12. The conversion rate is 8 kHz.
13. This amplifier should be used only in differential mode.
14. Common mode: 1.5 V

power-supply rejection characteristics (see Note 15)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD(1)}$	Supply-voltage rejection ratio, ADC channel, AV_{DD1}, and AV_{DD2}	f_I = 0 to $f_S/2$			–50	dB
$V_{DD(2)}$	Supply-voltage rejection ratio, DAC channel, and DV_{DD}	f_I = 0 to 30 kHz			–50	

NOTE 15: Power-supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

power-supply characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(analog)}$	Codec power-supply current, analog (including drivers); AV_{DD1}, AV_{DD2}	Operating		30.8	61.5	mA
$I_{DD(digital)}$	Codec power-supply current, digital; DV_{DD}.	Operating		5.5		
$I_{DD(speaker)}$	Power-supply current, 8-Ω speaker driver; AV_{DD3}.	Operating		200	400	
$I_{DD(quiescent)}$	8-Ω driver dc current without swing at output; AV_{DD3}.			1		
$I_{DD(analog)}$	Codec power-supply current, analog (hardware power down mode)	PWRDWN pin = logic 1		100		μA
$I_{DD(digital)}$	Codec power-supply current, digital (hardware power down mode)	PWRDWN pin = logic 1		2.2	4	mA
$I_{DD(analog)}$	Codec power-supply current, analog	Analog master power down			500	μA

speaker driver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N(PP)}$	Output peak-to-peak voltage (between SPOUTP and SPOUTM)	AV_{DD3} = 3.3 V, fully differential, 8-Ω load, 0 dBr = full-scale digital input; PGA gain = 0 dB.		5		$V_{(P–P)}$
V_{OO}	Output offset voltage	Fully differential		±5		mV
THD	Total harmonic distortion	AV_{DD3} = 3.3 V, 80-mW output, 8-Ω load		–60		dB
	Max output power (peak)	R_I = 8 Ω, AV_{DD3} = 3.3 V		390		mW
	Mute			–80		dB
	Max capacitive load			25		pF
	Minimum resistive load			8		Ω

handset and headset driver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N(PP)}$	Output peak-to-peak voltage	AV_{DD1}, AV_{DD2} = 3.3 V, fully differential, 150-Ω load		4		V
V_{OO}	Output offset voltage	Fully differential		±5		mV
THD	Total harmonic distortion	AV_{DD1}, AV_{DD2} = 3.3 V, 150-Ω load		–60		dB
	Max capacitance load			100		pF
	Mute			–80		dB
	Minimum resistive load			150		Ω

line driver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N(PP)}$	Output peak-to-peak voltage	AV_{DD1}, AV_{DD2} = 3.3 V, fully differential, 600-Ω load, 0-dB gain		4		V
V_{OO}	Output offset voltage	Fully differential		±5		mV
	Max capacitive load for LNOUT			25		pF
	Max resistive load for LNOUT			600		Ω
THD	Total harmonic distortion	AV_{DD1}, AV_{DD2} = 3.3 V, 600-Ω load		–80		dB
	Mute (neither DAC connected to line driver)			–80		dB

4-bit DAC characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	AV_{DD1}, AV_{DD2} = 3.3 V	0		3	V
	Linearity			±0.5		LSB
	Output load				600	Ω
					20	pF
t_s	Settling time			0.2		µs

microphone bias characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	At MCBIAS pin, sourcing 4 mA		2.5		V
I_O	Output current, max	Source only		4		mA
	Output noise	20 Hz to 20 kHz		60		µVrms
	Output PSRR	Up to 8 kHz		76		dB

timing requirements

MCLK

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency			32.768 or 24.576	32.768	MHz
	Accuracy			±200		ppm
	Duty cycle		40%	50%	60%	
t_r	Rise time			8		ns
t_f	Fall time			8		ns

timing requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(1)}$	Delay time, BCLK↑ to FSYNC↑ (slave mode)				15	ns
$t_{d(2)}$	Delay time, MCLK↑ to BCLK↑ (slave mode)				29	ns
$t_{su(1)}$	Setup time, DIN valid before BCLK ↓		10			ns
$t_{h(1)}$	Hold time, DIN valid after BCLK ↓		9			

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(1)}$	Delay time, BCLK↑ to FSYNC↑ (master mode)		5		10	ns
$t_{d(2)}$	Delay time, MCLK ↑ to BCLK ↑ (master mode)		19		29	ns
$t_{d(3)}$	Delay time, BCLK ↑ to DOUT valid	C_L = 20 pF			25	ns
$t_{d(4)}$	Delay time, BCLK↑ to FSYNC ↓ (master mode)		3			ns
$t_{d(5)}$	Delay time, BCLK ↓ to DOUT invalid				BCLK low time/ 2 + $t_{d(2)}$	ns
$t_{d(6)}$	Delay time, BCLK ↑ to DOUT high impedance following last data-bit transfer				25	ns

reset timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	$\overline{\text{RESET}}$ pulse width		2/MCLK			ns
$t_{h(r)}$	Wait time after $\overline{\text{RESET}}$			10		µs

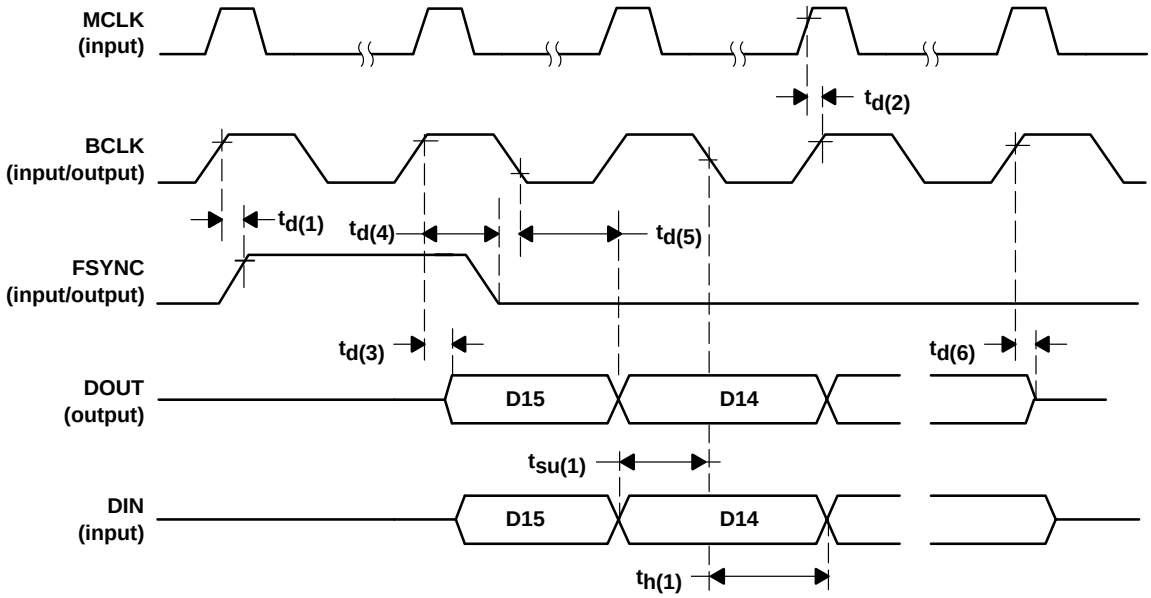


Figure 2. Digital I/O Timing for Data Channel

detailed description

codecs

There are two codecs on the TLV320AIC22 that can be connected to any of the analog inputs or outputs via the internal analog crosspoint. The codecs are full 8-bit PCM companded or 16-bit linear codecs that meet G.711 standards and include transmit band-pass and receive low-pass filters. A-law/μ-law companding or linear coding and –36 dB to 12 dB of analog gain adjustment in steps of 1.5 dB for each path are selectable via the I^2C or serial interface. These modes can be selected by programming the appropriate register. In the 8-bit PCM companded mode, the data is zero padded to 15 bits, and the 16th bit serves as the valid data bit.

analog crosspoint

The internal analog crosspoint is a lossless analog switch matrix controlled via the I^2C or serial interface. It allows any source device to be connected to any sink device. Additionally, special summing connections with adjustable loss are included to implement sidetone for the handset and headset ports. A muting function is included on any of the sink devices. The control for the analog crosspoint, defined in the register map, is done in such a way that a particular analog input or output can be connected to a codec by setting a single bit. This implies that more than one analog input or output can be connected to a codec at one time. Full performance is assured for two or fewer inputs and outputs connected to a codec, except in the case of the line output. Connecting the output of both codecs to the line output (LNOUTP and LNOUTM) is not allowed.

ADC channel

The ADC channel consists of a programmable gain amplifier (PGA), antialiasing filter, sigma-delta ADC and decimation filter. The ADC is an oversampling sigma-delta modulator. The ADC provides high resolution and low-noise performance using oversampling techniques and the noise-shaping advantages of sigma-delta modulators.

The analog input signals are amplified and filtered by on-chip buffers and an antialiasing filter before being applied to ADC input. The ADC converts the signal into discrete output digital words, in 2s-complement format, corresponding to the analog signal value at the sampling time.

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio equal to the oversampling ratio. The output of this filter is a 15-bit 2s-complement data word, clocking at the selected sample rate. The sixteenth bit is a data-valid flag.

These 15-bit digital words, representing sampled values of the analog input signal, are sent to the host via the serial-port interface. If the ADC reaches its maximum value, a control register flag is set. This bit can be read only via the serial port. The ADC and DAC conversions are synchronous.

The digital conversion data is transmitted out of the device via the serial interface, with the data-valid flag being transmitted first, followed by the MSB of the conversion data. Data is transmitted on the rising edge of BCLK.

The bandwidth of the codec is 3.6 kHz, for a sampling rate of 8 kHz, and scales linearly for other sampling rates. The gain of the ADC input amplifier is programmed in register 3 for codec 1 and register 8 for codec 2.

The ADC channel contains a high-pass filter that suppresses power-line frequencies that can be bypassed by programming the appropriate bits in registers 15 and 16 for codec 1 or codec 2, respectively.

detailed description (continued)

DAC channel

The DAC channel consists of an interpolation filter, a sigma-delta DAC, low-pass filter, and a programmable gain amplifier. The DAC is an oversampling sigma-delta modulator. The DAC performs high-resolution, low-noise DAC, using oversampling sigma-delta techniques.

The DAC receives 16-bit data words (2s complement) from the host via the serial-port interface. Data is latched on the falling edge of BCLK. The MSB of the digital data is transmitted to the DAC first, ending with the LSB as the last bit.

The data is converted to an analog voltage by the sigma-delta DAC, composed of a digital interpolation filter and a digital modulator. The interpolation filter resamples the digital data at a rate of N times the incoming sample rate, where N is the oversampling ratio. The high-speed data output from this filter then is applied to the sigma-delta DAC.

The DAC output then is passed to an internal, low-pass filter to complete the signal reconstruction, resulting in an analog signal. This analog signal then is buffered and amplified by a differential output driver capable of driving the required load. The gain of the DAC output amplifier is programmed in register 4 for codec 1 and register 9 for codec 2.

analog and digital loopback

The test capabilities include an analog loopback and digital loopback. The loopbacks allow the user to test the ADC/DAC channels and can be used for in-circuit system-level tests. The digital loopback feeds the ADC output to the DAC input on the device. The analog loopback loops the DAC output back into the ADC input.

power down and reset

When the power-down pin (PWRDWN) is pulled high, the device goes into a power-down mode, where the required analog power-supply current drops to approximately 100 μA and the digital power-supply current drops to approximately 2 mA. This is called the hardware power-down mode. The serial interface and I^2C interface still are enabled. All register values are sustained and the device resumes full-power operation without reinitialization when PWRDWN is pulled low again. PWRDWN resets the counters only and preserves the programmed register contents. After the PWRDWN pin has been pulled low, the user must wait at least two frame syncs before communicating control or conversion information.

Software control can be used to power down individual codecs. Each codec is composed of an ADC, DAC, and a digital filter. Codec power down resets all internal counters, but leaves the contents of the programmable control registers unchanged. Analog circuitry and the analog power-supply current are not affected when programming codec power-down mode. Codec power down is achieved by programming register 2 for codec 1 and register 7 for codec 2.

An analog master power down also can be initiated via software control by programming register 14. Analog master power down is used to power down all of the analog circuitry within the device. This mode is similar to hardware power down in that the required analog power-supply current drops to approximately 100 μA.

Table 1 shows the state of the pins during codec power down and hardware power down.

power down and reset (continued)

Table 1. Pin States During Hardware and Codec Power Down

PIN NAME	STATE DURING CODEC POWER DOWN	STATE DURING HARDWARE POWER DOWN
HDOUTM	Internal common-mode voltage (1.5 V)	Floating
HDOUTP	Internal common-mode voltage (1.5 V)	Floating
SPOUTP	Internal common-mode voltage (1.5 V)	Floating
SPOUTM	Internal common-mode voltage (1.5 V)	Floating
HSOUTM	Internal common-mode voltage (1.5 V)	Floating
HSOUTP	Internal common-mode voltage (1.5 V)	Floating
LNOUTM	Internal common-mode voltage (1.5 V)	Floating
LNOUTP	Internal common-mode voltage (1.5 V)	Floating
HDINP	Normal operation	Floating
HDINM	Normal operation	Floating
MCINP	Normal operation	Floating
MCINM	Normal operation	Floating
HSINM	Normal operation	Floating
HSINP	Normal operation	Floating
LNIN	Normal operation	Floating
LNINM	Normal operation	Floating
LCDOUT	Normal operation	Floating
MCBIAS	Normal operation	Floating
PWRDWN	Normal operation	Normal operation
SDA	Normal operation	Normal operation
SCL	Normal operation	Normal operation
AD1	Normal operation	Normal operation
AD0	Normal operation	Normal operation
$I^2C/\overline{SPI}$	Normal operation	Normal operation
DOUT	Normal operation	Normal operation
DIN	Normal operation	Logic high
FSYNC	Normal operation	Normal operation
BCLK	Normal operation	Normal operation
VCOM	Normal operation	Floating
$M/\overline{S}$	Normal operation	Normal operation
CIINP		Pulled to AV_{SS1}/AV_{SS2} through 40 kΩ
CIINM		Pulled to AV_{SS1}/AV_{SS2} through 40 kΩ

The capability to individually power down each output driver also is present. Table 2 shows the typical power savings that can be achieved if the associated driver is powered down.

Table 2. Powering Down Individual Drivers

DRIVER POWERED DOWN	REGISTER USED TO POWER DOWN DRIVER	TYPICAL POWER SAVINGS WHEN OUTPUT POWERED DOWN
Handset	13	3.2 mA
Headset	14	3.2 mA
Speaker	11	1 mA
Line output	14	2.5 mA

power down and reset (continued)

There are two ways to reset the TLV320AIC22:

- By pulling the $\overline{\text{RESET}}$ pin low, or
- By writing to the software reset bits in control registers 2 and/or 7 to reset either codec

Asserting the $\overline{\text{RESET}}$ pin low puts the device into a default state with default register settings. After deasserting the $\overline{\text{RESET}}$ pin, the user should wait a minimum of 10 μs before sending control or conversion data to the device.

The default register settings are described in the sections titled *suggested configuration sequence* and *register map*. After a software reset has been removed, control and conversion data can be sent in the next frame.

Asserting a software reset by programming register 2 puts register 1, 2, 3, 4, 5, and 15 in their default settings and resets codec 1.

Asserting a software reset by programming register 7 puts register 6–14, 16, and 17 in their default settings and resets codec 2.

microphone bias

To operate Electret microphones properly, a bias voltage and current are provided. Typically, the current drawn by the microphone is on the order of 100 μA to 800 μA and the bias voltage is specified across the microphone at 2.5 V. The bias has good power-supply noise rejection in the audio band, can source 4-mA max current, and can be shared between all the microphones.

microphone amplifiers

There are three microphone preamplifiers, one each for the handset, headset, and speakerphone microphones. The input signals for the handset and headset amps typically are less than 20 mVrms, 100 mV max. The input signals for the speakerphone amp typically are less than 2 mVrms, 20 mV max. The amplifiers have a differential input to minimize noise and EMC immunity problems. Three values for the gain for the handset and headset microphones and four values for the gain for the speakerphone microphone are selectable via the I^2C or serial interface to cater to the requirements in Europe and North America. The frequency response is flat, up to 8 kHz.

Table 3. Gain Settings

INPUT	GAIN SETTINGS
Handset microphone preamp (HSINP,M)	0 dB, 14 dB, 23 dB, or mute
Headset microphone preamp (HDINP,M)	0 dB, 14 dB, 23 dB, or mute
Speakerphone microphone preamp (MCINP,M)	0 dB, 20 dB, 32 dB, 42 dB, or mute

By default, the echo gain for the handset and headset are 14 dB. Therefore, a connection exists between the handset and headset inputs (microphones) and their respective outputs (speakers) in order to implement sidetone.

driver amplifiers

There are two driver amplifiers that are meant to drive a 150-Ω handset or headset speakers, differentially. The drive amplifier is differential, to minimize noise and EMC immunity problems. The frequency response is flat, up to 8 kHz.

speakerphone amplifiers

The speakerphone speaker impedance is 8 Ω. The drivers are capable of providing a 5-V peak-to-peak differential signal, which means that the peak power is about 390 mW. The differential drive amplifier achieves this and minimizes noise and EMC immunity problems. The frequency response is flat, up to 8 kHz.

4-bit DAC

The 4-bit DAC can be used to provide bias to any component on the board, such as a liquid-crystal display (LCD). The output of the 4-bit DAC is controlled through the I^2C or the serial interface by writing to the four LSBs of control register 12. It uses 2s-complement data. The DAC has a settling time of about 5 μs, a linearity of ±0.5 LSB, and is a voltage output DAC. It provides a maximum output of 3 V. For a 16-character by 2-line LCD display module, the contrast control requires 0.2 mA. The input codes and the corresponding output voltages at the LCDOUT pin are shown in Table 4.

Table 4. 4-Bit DAC Input Code vs Output Voltage

INPUT VALUE (DECIMAL)	INPUT CODE (2s COMPLEMENT) D3–D0	OUTPUT VOLTAGE
7	0111	2.8125
6	0110	2.625
5	0101	2.4375
4	0100	2.25
3	0011	2.0625
2	0010	1.875
1	0001	1.6875
0	0000	1.5
–1	1111	1.3125
–2	1110	1.125
–3	1101	0.9375
–4	1100	0.75
–5	1011	0.5625
–6	1010	0.375
–7	1001	0.1875
–8	1000	0

callerID amplifier

The callerID amplifier has a fixed 0-dB gain (typ), attenuates the low-frequency ring signal, and isolates from the line. This input also can be connected to the ADC via the analog crosspoint.

line ports

The line ports can be connected, via a transformer, to a telephone line. The driver stage is capable of driving a 600-Ω load, differentially, to near rail-to-rail swing. This stage is implemented such that the resistors and capacitors are integrated. Signal levels at the input pins can be as high as 1.4 Vrms (2 V). The analog pole select option (register 14) allows the user to select the position of the filter pole for the line input and output.

serial interface

The serial interface is designed to provide glueless interface to the MCBSP port of a TMS320C54x or TMS320C6x DSP. This interface is used primarily for transferring ADC and DAC data. However, control register information also can be transferred; refer to *register programming using the serial interface*. The serial interface is a four-line interface, consisting of the following:

- BCLK: the bit clock used to transmit and receive data bits
- FSYNC: the frame-sync signal that denotes the start of a new frame of data
- DOUT: the output serial data used to transfer ADC data and register information to the attached DSP

- DIN: the input serial data used to transfer DAC data and register control information from the attached DSP

serial interface (continued)

The TLV320AIC22 can be configured as a master or a slave. See the *master/slave functionality* section for a detailed description. When configured as a master device, FSYNC and BCLK are generated by the master codec and input to the DSP.

Data is received and transmitted in frames consisting of 256 BCLKs, which is 16, 16-bit time slots. Each frame is subdivided into time slots, consisting of 16 BCLKs per time slot. In each frame, two time slots are reserved for control-register information and eight time slots are reserved for codec data. The remaining six time slots are unused. A pulse on the FSYNC pin indicates the beginning of a frame.

The control information is valid only when the serial interface has been selected by connecting the I^{2}C/$\overline{\text{SPI}}$ pin to logic 0. The frame format is shown in Figure 3, and the timing diagram for the frame is shown in Figure 4.

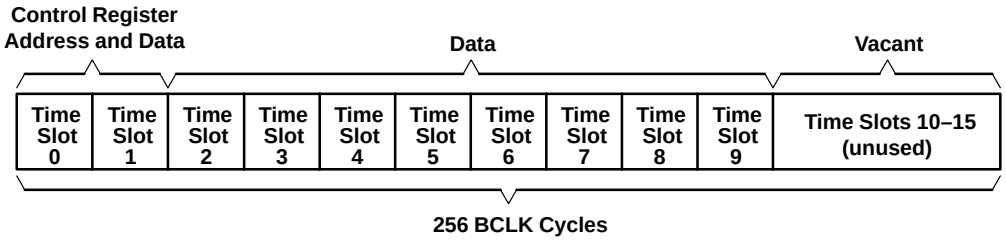


Figure 3. Frame Format Used by the TLV320AIC22

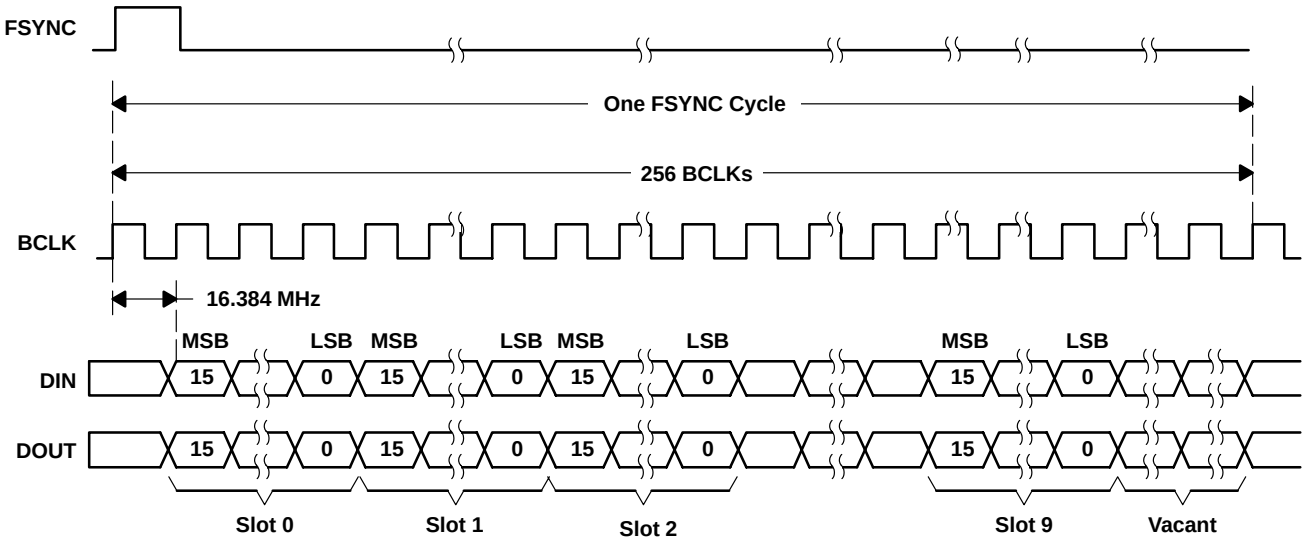


Figure 4. Timing Diagram for the TLV320AIC22 Frame Format

When the serial interface is selected for control (the I^{2}C/$\overline{\text{SPI}}$ pin set to logic 0), the first two time slots after the FSYNC pulse (time slots 0 and 1) are used for sending and receiving control data. The next eight slots are used for actual conversion data sent and received by the codec.

Each time slot is 16 bits wide. Data bytes always are sent, with the first bit representing the MSB. Transmitted data is sent on the rising edge of BCLK and data being received is latched on the falling edge of BCLK.

detailed description (continued)

control register address and data

When the $I^2C/\overline{SPI}$ pin is tied to a logic low, the serial interface is selected for controlling the device. Control information is sent and received in time slots 0 and 1. An active-high pulse on the FSYNC pin indicates the start of a frame. The structure of time slots 0 and 1 is shown in Figures 5 and 6. Bit 15 (the MSB) is transmitted or received first. Transmitted data is sent on the rising edge of BCLK and data being received is latched on the falling edge of BCLK.

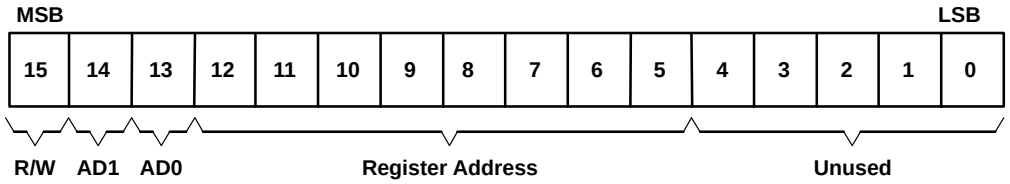
Time slot 0 indicates:

- If a read or write operation is occurring
- Which device is being accessed
- The register address within the device being accessed

AD0 (LSB) and AD1 (MSB) form the device address. Up to four TLV320AIC22 devices can be addressed, with addresses ranging from 0 to 3. The five LSBs in time slot 0 are unused.

Slot 0:

B15	Read/write control	1 = Write, 0 = Read
B14	AD1 device address bit (MSB)	
B13	AD0 device address bit (LSB)	
B12–B5	Register address (8 bits)	
B4–B0	Unused	



NOTE: The register address is the binary equivalent of the register number

Figure 5. Bit Assignment and Definition for Slot-0 Word

If bit 15 in slot 0 is a 1, a write operation has been requested by the DSP. The DSP drives data onto the DIN pin in the next time slot (time slot 1) as follows:

- The 8 bits of data to be written into the register appear on the first 8 bits, with the MSB appearing first.
- The next 8 bits (8 LSBs) are unused.

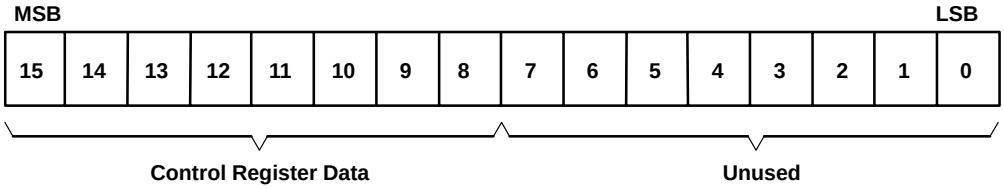
If bit 15 in slot 0 is a 0 a read operation has been requested. The TLV320AIC22 compares the values of the device address bits, bits 14 and 13 of time slot 0 (AD1 and AD0 bits) to the configuration of the AD1 and AD0 pins on the device to determine if it is the device being addressed. The device drives data on DOUT if it is the addressed device, as follows:

- The 8 bits of data from the addressed register appear in the first 8 bits, with the MSB appearing first.
- The next 8 bits (8 LSBs) are unused.

Slot 1:

B15–B8	Control register data
B7–B0	Unused

control register address and data (continued)



NOTES: A. If the register address is 0x00h, then no register will be updated.

B. The default condition is for control information to be updated every frame. If control information is not to be updated every frame, then register 17 can be programmed to cause the control slots to appear with N frames of empty control slots between them. The contents of register 17 is equal to N. In this condition, the data in slots 0 and 1 that appear in the N frames between frames with valid control slots are ignored. The default setting for register 17 is 0; control slots will appear in every frame. After register 17 is programmed with a nonzero value, the first sequence will have N – 1 frames with empty control slots.

Figure 6. Bit Assignment and Definition for Slot-1 Word

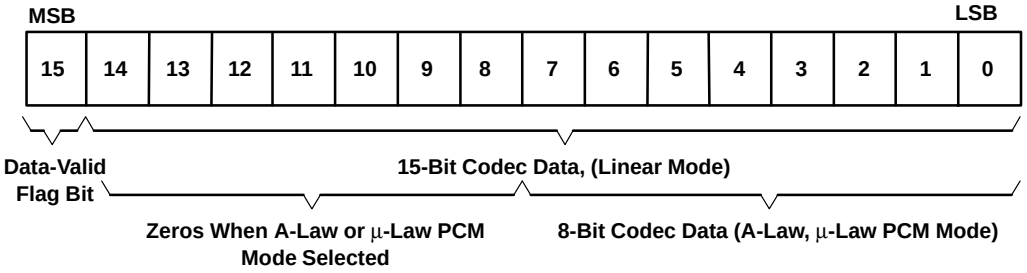
ADC data word

A data word occupies one time slot and is 16 bits long. The ADC data word (output on DOUT) can be any of the following:

- Data-valid flag + 15 bits of linear data
- 16 bits of linear data (no data-valid flag)
- Data-valid flag + A-law or μ-law coded PCM data
- A-law or μ-law coded PCM data (no data-valid flag)

The selection of linear, A-law, or μ-law coding is programmed in register 15, bits 6 and 7. The selection for providing the data-valid flag bit is programmed in register 13. See the *ADC and DAC channel data* section for a detailed description of the valid and invalid data.

The structure of a data word is shown in Figure 7 and Figure 8.



NOTE: The MSB of the codec data is bit 14 for linear mode and bit 7 for A-law and μ-law.

Figure 7. Bit Assignment and Definition for ADC Data Word When the Data-Valid Flag is Enabled

Figure 7 describes the ADC data-word format when the data-valid flag is used. The data-valid flag is positioned in bit 15 (the MSB of the data word) and is transmitted first. The flag bit is enabled by programming register 13.

Bit 14 of the data word is the most significant bit of the 15-bit codec data when the linear mode is selected and the data-valid flag is enabled.

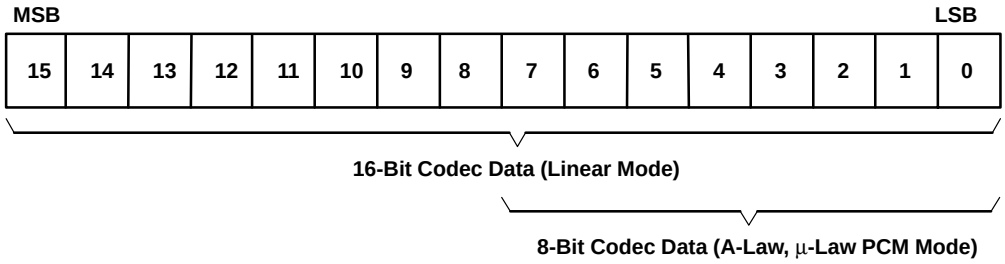
When A-law or μ-law PCM coding is selected, the 8 bits of the PCM data are located, with the MSB in the bit 7 location and the LSB in the bit 0 location of the data word. Unused bits are zero when PCM coding is enabled.

Bit 15 always is the data-valid flag for both the PCM and linear coding when the data-valid flag is enabled. The selection of linear, A-law, or μ-law coding is programmed in register 15, bits 6 and 7.

ADC data word (continued)

Figure 8 describes the ADC data-word format when the data-valid flag is disabled.

When the data-valid flag is disabled, 16 bits of data are presented in the linear mode, with the MSB in bit 15. When A-law or μ-law PCM coding is selected, the 8 bits of the PCM data are located with the MSB in the bit-7 position and the LSB in the bit 0 position. The upper byte of the 16-bit word can be ignored for PCM coding and will contain zeros.



NOTE: The MSB of the codec data is bit 15 for linear mode and bit 7 for A-law and μ-law.

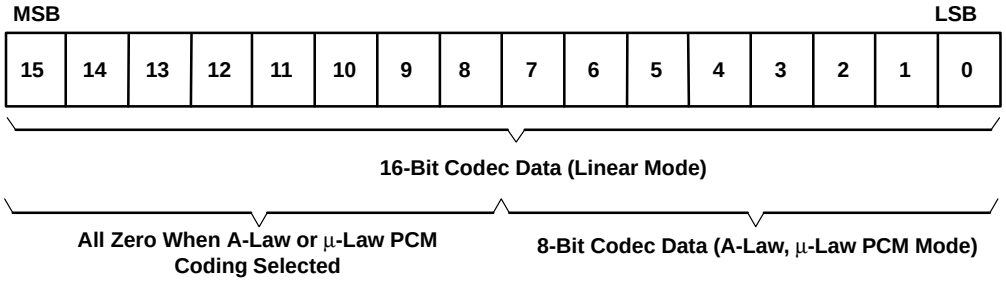
Figure 8. Bit Assignment and Definition for ADC Data Word When the Data-Valid Flag is Disabled

DAC data word

The DAC data word (input on DIN) can be any of the following:

- 16 bits of linear data
- A-law or μ-law coded PCM data

The structure of the DAC data word is shown in Figure 9.



NOTE: The MSB of the DAC data is bit 15 for linear mode and bit 7 for A-law and μ-law.

Figure 9. Bit Assignment and Definition for DAC Data Word

address pins description

The AD1 and AD0 pins are used to define the address of the codec in the I^2C mode and for the serial interface. See the *register programming using the I^2C bus* section for a detailed description of the I^2C mode. For the serial interface, the address determines the time slot used by a certain codec. Provisions are made to support up to four TLV320AIC22s connected to a single DSP. Therefore, eight slots are used for data.

Table 4 shows how the time slots used are related to the AD1 and AD0 address lines. Codec 1 in a TLV320AIC22 communicates during the first assigned time slot, based on the AD0 and AD1 configuration, while codec 2 in the same TLV320AIC22 communicates during the second assigned time slot, based on that same AD0/AD1 configuration.

address pins description (continued)

Table 5. AD0 and AD1 vs Time-Slot Assignment

TLV320AIC22 DEVICE	AD1	AD0	TIME SLOT CODEC 1	TIME SLOT CODEC 2
0	0	0	2	3
1	0	1	4	5
2	1	0	6	7
3	1	1	8	9

This address description also is used to make the codec register address map unique across the codecs. This is explained further below.

master/slave functionality

The TLV320AIC22 can be configured as a master or a slave. A particular codec is configured as the master by tying the M/$\overline{S}$ pin (pin 21) high. Tying this pin low configures the device as a slave.

This functionality can be used for connecting multiple TLV320AIC22 devices to a single MCBSP port. See Figure 20 for details. Only one device can be a master in such a system. The master device generates the FSYNC and the BCLK signals that are used by the DSP and the remaining TLV320AIC22s in the system. The slave devices input the FSYNC and BCLK signals generated by the master device.

The TLV320AIC22 also can be used as a stand-alone slave. In this configuration, there is no master TLV320AIC22 device providing the FSYNC and BCLK signals. FSYNC and BCLK are provided by some other device, such as a DSP or ASIC.

Careful attention must be paid to the relationship between MCLK, FSYNC, and BCLK when using stand-alone slave configurations. When operating the device in the default mode (sampling-rate mode-1 configuration), the configurations shown in Table 6 must be met.

Table 6. Slave-Mode Clock Inputs

MCLK INPUT FREQUENCY	BCLK INPUT FREQUENCY	FSYNC INPUT FREQUENCY	REGISTER 12 VALUE (BITS D6–D4, DECIMAL)
24.576 MHz	2.048 MHz	8 kHz	0
24.576 MHz	4.096 MHz	16 kHz	2
32.768 MHz	2.048 MHz	8 kHz	1
32.768 MHz	4.096 MHz	16 kHz	3

All of these signals (BCLK, MCLK, and FSYNC) must be synchronous. The appropriate values for register 12, bits D6 – D4, as well as the I values for codec 1 (register 2) and codec 2 (register 7), must be loaded prior to transmitting and receiving valid conversion data to obtain the desired sampling rate. See the *channel sampling rates* section for a detailed description.

zero-crossing block

The zero-crossing functionality (programmed in registers 15 and 16) comes into play when the user changes a preamp or PGA gain setting. When the user wishes to change a gain setting in a particular channel (ADC or DAC path), the changed gain takes effect when the signal level coming from the particular channel crosses a programmed threshold. The threshold can be specified in registers 15 and 16 for either channel, for example, if the user is talking on the handset and wishes to mute it. The zero-crossing block checks the ADC input to see whether the input falls within the programmed range before making the mute effective internally. This is to avoid noise if a sharp change is implemented. Note, in the TX path, the zero crossing block checks the ADC input value only. If both the handset and the microphone are in use with one ADC channel, and the user wishes to mute the handset only, the zero-crossing block does not avoid noise when muting the handset. If the user mutes both the handset and the microphone, then zero crossing will be evaluated properly.

On the DAC side, the zero crossing is effective in a similar manner. The DAC output is checked to see whether the value is within the programmed range. The mute then becomes effective in the driver where mute has been selected.

Deactivating mute also is taken care of in the same fashion. If the user wants to deactivate mute, the TLV320AIC22 internally checks to see if the signal level is within the programmed limit and then allows the device to deactivate. Internally, a change in gain setting becomes effective only after the signal level has reached a value close to zero.

If the signal does not cross the programmed zero-crossing threshold, the gain change occurs automatically after $64/f_S$ seconds.

channel sampling rates

The TLV320AIC22 can be configured to have standard sampling rates (8 kHz and 16 kHz), or other popular sampling rates, by loading appropriate registers with a divider to scale the master clock input with an I + N/D divider. Two modes of operation are discussed below.

- Mode 1 configures the device for the standard sampling rates. In this mode, the sampling rate (f_S) equals the frame sync rate (FSYNC).
- Mode 2 allows user defined sampling rates and uses an (I + N/D) divider.

A block diagram of the clock-division scheme used in the TLV320AIC22 is shown in Figure 10.

channel sampling rates (continued)

Register 12 (Bits D6 to D4 and Value of R)

R	REG 12	MODE
12	0	1
16	1	1
6	2	1
8	3	1
2	5	2

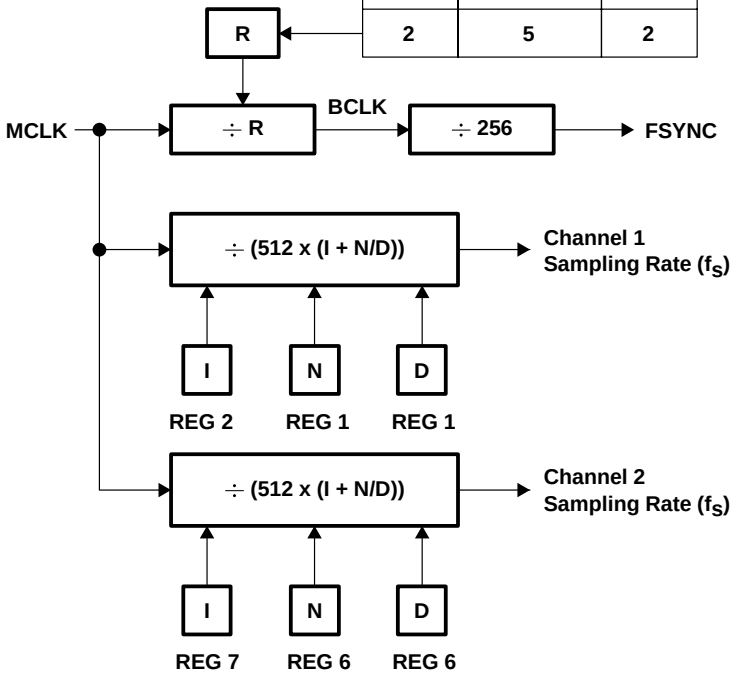


Figure 10. Block Diagram of the Clock-Division Scheme

detailed description (continued)

sampling rate mode 1

Examples of popular master clock frequencies, with the derivations of the sampling rates, bit clocks, and the frame sync frequencies, are given in Table 7. The default setting is for a case in which the channel sampling rate and FSYNC are at 8 kHz when a MCLK of 24.576 MHz is provided. The default setting is for register 12 to have bits D6–D4 equal to 000 and registers 1, 2, 6, and 7 to be left in their default configuration.

The various parameters for sampling rate-mode 1 are determined using the following equations:

BCLK = See Table 7
FSYNC = BCLK/256
Sample rate = MCLK/[512(I + N/D)]

Table 7. FSYNC, BCLK, and Sample Rate Derivations With Register Settings

D6	D5	D4	MCLK INPUT (MHz)	FSYNC	BCLK	SAMPLE RATE	I	N	D
0†	0†	0†	24.576	BCLK/256 or 8 kHz	MCLK/12 or 2.048 MHz	MCLK/[512 x (I + N/D)] or 8 kHz	*6	*0	*6
0	0	1	32.768	BCLK/256 or 8 kHz	MCLK/16 or 2.048 MHz	MCLK/[512 x (I + N/D)] or 8 kHz	8	0	*6
0	1	0	24.576	BCLK/256 or 16 kHz	MCLK/6 or 4.096 MHz	MCLK/[512 x (I + N/D)] or 16 kHz	3	0	*6
0	1	1	32.768	MCLK/(512x4) or 16 kHz	MCLK/8 or 4.096 MHz	MCLK/[512 x (I + N/D)] or 16 kHz	4	0	*6

† This is the default setting.

sampling rate mode 2

In mode 2, the sampling rate for each channel is derived by the noninteger-divide (I + N/D) of the FSYNC signal. Each channel has dedicated 4-bit programmable fields (I, N, and D) to achieve this. All sampling rates of interest such as 7.2 kHz, 8 kHz, 8.229 kHz, 9.6 kHz, 10.285 kHz, 12 kHz, and 14.4 kHz, are achievable by programming the appropriate values into the I, N, and D registers. Register 12 also must be programmed with a decimal value of 5, 6, or 7 in bits D6 through D4.

The various parameters for sampling rate-mode 2 are determined using the following equation:

BCLK = MCLK/2
FSYNC = BCLK/256
Sample rate = MCLK/[512 x (I + N/D)]

BCLK is generated by the master codec according to the following relationship (note that MCLK is 32.768 MHz for this example):

BCLK = MCLK/2 = 32.768 MHz/2 = 16.384 MHz

and the FSYNC is obtained by dividing the BCLK by 256:

FSYNC = BCLK/256 = 16.384 MHz/256 = 64 kHz

An example of how to achieve a channel sample rate of 12 kHz with an MCLK of 32.768 MHz is shown in Table 8.

sampling rate mode 2 (continued)

Table 8. I, N, and D Derivation for 32.768-MHz Clock and 12-kHz Sampling Rate

PARAMETER OR VARIABLE	EQUATION	VALUE
MCLK	None	32.768 MHz (given)
BCLK	MCLK/2	16.384 MHz
FSYNC	BCLK/256	64 kHz
Sample rate	MCLK/[512 x (I + N/D)]	12 kHz (given)
I + N/D	MCLK/(512 x sample rate)	5.3333
I		5
N		3
D		9

The binary equivalent of the following values are loaded into the respective registers for a 12-kHz channel sampling rate: I = 5 (I – 1 = 4), N = 3 and D = 9 (D – 1 = 8).

Table 7 shows the corresponding values for I, N, and D for some of the popular sampling rates, with MCLK = 32.768 MHz. Note, that the value of D always should be a nonzero value. When programming the TLV320AIC22, the values of I and D are decremented by one and the N value is entered without any change. The values to be programmed also are shown in Table 9.

Table 9. I, N, and D Derivation for Various Sample Rates, With MCLK = 32.768 MHz

	I, N, AND D VALUES FOR CHANNEL SAMPLE RATES, WITH MCLK = 32.768 MHz				ACTUAL VALUES TO BE PROGRAMMED IN REGISTERS 1, 2, 6, AND 7		
Channel sample rate (kHz)	I + N/D	I	N	D	I–1	N	D–1
7.2	8.8889	8	8	9	7	8	8
8	8.0000	8	0	9	7	0	8
8.229	7.7774	7	7	9	6	7	8
9.6	6.6667	6	6	9	5	6	8
10.285	6.2227	6	2	9	5	2	8
12	5.3333	5	3	9	4	3	8
14.4	4.4444	4	4	9	3	4	8
16	4.0000	4	0	9	3	0	8

It is possible to use other frequencies for MCLK and achieve the above channel sample rates. For example, using an MCLK frequency of 24.576 MHz, the following occurs:

BCLK = MCLK/2 = 12.288 MHz
FSYNC = BCLK/256 = 48 kHz
Channel sample rate = MCLK/ [512 x (I + N/D)] = 48 kHz/(I + N/D)

Therefore, (I + N/D) = 48 kHz/channel sample rate

Table 10 shows the corresponding values for I, N, and D for some of the popular sampling rates, with MCLK equal to 24.576 MHz. Again, note that the value of D should always be a nonzero value. As discussed earlier, the values that the TLV320AIC22 are actually programmed with are I–1, N, and D–1.

sampling rate mode 2 (continued)

Table 10. I, N, and D Derivation for Various Sample Rates, With MCLK = 24.576 MHz

	I, N, AND D VALUES FOR CHANNEL SAMPLE RATES, WITH MCLK = 24.576 MHz				ACTUAL VALUES TO BE PROGRAMMED IN REGISTERS 1, 2, 6, AND 7		
Channel sample rate (kHz)	I + N/D	I	N	D	I–1	N	D–1
7.2	6.6667	6	4	6	5	4	5
8	6	6	0	6	5	0	5
8.229	5.833	5	5	6	4	5	5
9.6	5	5	0	6	4	0	5
10.285	4.6669	4	4	6	3	4	5
12	4	4	0	6	3	0	5
14.4	3.3333	3	2	6	2	2	5
16	3	3	0	6	2	0	5

ADC and DAC channel data

The ADC channel produces 15 bits of 2s-complement conversion data in linear mode or 7 bits of zeros and 8 bits of PCM coded data in A-law or μ-law mode, plus a data-valid flag bit which, by default, is enabled. For the cases where register 12 is programmed for the standard sampling frequencies and the I + N/D divider is not used, the ADC will place a 1 in the data-valid bit for all conversion data if the data-valid flag is enabled in register 13.

The DAC uses 16 bits of 2s-complement data or 8 bits of zeros, followed by 8 bits of PCM data as input. No data-valid flag is required for the DAC data.

Based on the rate of the FSYNC pulse, the ADC generates the internal circuit clocks using the (I + N/D) divider. Two examples below show how different sampling rates are obtained using this technique for sampling rate mode 2. Both examples are valid for MCLK equal to 32.768 MHz. Note that when FSYNC is not equal to the sample rate, the valid data is present between several occurrences of invalid data.

Example 1: If an 8-kHz sampling rate is needed and the frame sync rate is at 64 kHz, only one out of every 8th frame will carry valid data for the codec in its slot. The data-valid flag bit in the data word is used to identify whether the data is valid (flag bit = 1) or invalid (flag bit = 0). The flag bit is the MSB of the 16-bit data word and is enabled, by default. The I, N, and D fields are used to decide the setting for the valid bit in the respective data slot. The codec generates the data-valid flag bits. See Table 11 for I, N, and D derivations for this example.

Table 11. I, N, and D Derivation for 32.768-MHz Clock and 8-kHz Sampling Rate

PARAMETER OR VARIABLE	EQUATION	VALUE
MCLK	None	32.768 MHz (given)
BCLK	MCLK/2	16.384 MHz
FSYNC	BCLK/256	64 kHz
Sample rate	MCLK/(512 x (I + N/D))	8 kHz (given)
I + N/D	MCLK/(512 x sample rate)	8
I		8
N		0
D		9

Example 2: If a 14.4-kHz sampling rate is needed and the frame sync rate is at 64 kHz, then the codec sends a valid data word every fourth or every fifth frame for 40 frames. This effectively implements I + N/D = 4 + 4/9 to get 14.4 kHz from 64 kHz. The DSP collects the data from every slot in every frame, then checks the data-valid flag bit. If the flag bit is set, the data is loaded into the buffer, otherwise, it is discarded.

ADC and DAC channel data (continued)

On the receive side (DAC), the DSP can use the same flag bits it extracts from the DOUT bit stream. It can use it as the DATA request signal for the DAC of the same codec and send the DAC data on DIN during the next frame.

The valid data appears in the Ith or (I + N)th frame. For every D number of valid ADC data bytes, the ADC transmits a valid data word in the (I + 1)th frame, for N times, and in the Ith frame for (D – N) times. I, N, and D are the values used for the (I + N/D) divider.

For this example where MCLK = 32.768 MHz, I + N/D = 4 + 4/9 and the sample rate is 14.4 kHz, the ADC data will appear in the fifth frame four times and in the fourth frame five times, repeating. The valid data bit/FSYNC pattern will be (in terms of frame syncs):

4, 5, 4, 5, 4, 5, 4, 5, 4

Then, this sequence repeats. See Table 12 for I, N, and D derivations for this example.

Table 12. I, N, and D Derivation for 32.768-MHz Clock and 14.4-kHz Sampling Rate

PARAMETER OR VARIABLE	EQUATION	VALUE
MCLK	None	32.768 MHz (given)
BCLK	MCLK/2	16.384 MHz
FSYNC	BCLK/256	64 kHz
Sample rate	MCLK/(512 x (I + N/D))	14.4 kHz (given)
I + N/D	MCLK/(512 x sample rate)	4.4444
I		4
N		4
D		9

Example 3: This example is for the case where codec 1 and codec 2 have different sampling rates. If an 8-kHz sampling rate is needed on codec 1, then codec 1 sends a valid data word every eighth frame for its particular time slot. If a 16-kHz sampling rate is needed on codec 2, then codec 2 sends a valid data word every fourth frame for its particular time slot. Table 13 shows the derivation of the parameters for each codec. A 32.768-MHz master clock is assumed.

Table 13. I, N, and D Derivation for 32.768-MHz Clock, With an 8-kHz Sampling Rate for Codec 1 and a 16-kHz Sampling Rate for Codec 2

PARAMETER OR VARIABLE	CODEC	EQUATION	VALUE
MCLK	–	None	32.768 MHz (given)
BCLK	–	MCLK/2	16.384 MHz
FSYNC	–	BCLK/256	64 kHz
Sample rate	Codec 1	MCLK/[512 x (I + N/D)]	8 kHz (given)
I + N/D	Codec 1	MCLK/(512 x sample rate)	8
I	Codec 1		8
N	Codec 1		0
D	Codec 1		9
Sample rate	Codec 2	MCLK/[512 x (I + N/D)]	16 kHz (given)
I + N/D	Codec 2	MCLK/(512 x sample rate)	4
I	Codec 2		4
N	Codec 2		0
D	Codec 2		9

detailed description (continued)

register programming

The TLV320AIC22 contains 17 registers that are used to configure the device for the desired operation. Register programming can be accomplished in two different ways:

- The serial interface (time slots 0 and 1)
- The I^2C bus

The $I^2C/\overline{SPI}$ pin is used to select either interface for programming the device.

register programming using the serial interface

To program the control registers using the serial interface, the $I^2C/\overline{SPI}$ pin should be tied to logic 0. The frame format and control-word description are discussed in *serial interface* earlier in this document.

Time slots 0 and 1 are used for codec register programming and are configured as follows:

- Slot 0: Read/write, physical address of codec register

This is the register address, appended to the codec address, derived from pins AD0 and AD1.

- Slot 1: Value to be written in the codec register for a write operation

For a read operation, the DIN slot 1 is zero stuffed. Depending on the register to be read, the codec puts the register contents on the slot 1 of DOUT in the same frame.

The following are examples of programming a TLV320AIC22 whose device address is set to 0 (AD0=AD1=0).

Example 1. Write Operation ($\overline{R}/W$ = 1):

Programming control register 15 of a device with address 0x00h with the data set to 0x23h results in the following data being driven on the DIN pin for time slots 0 and 1:

Slot 0: 1 00 0000 1111 00000
Slot 1: 0010 0011 0000 0000

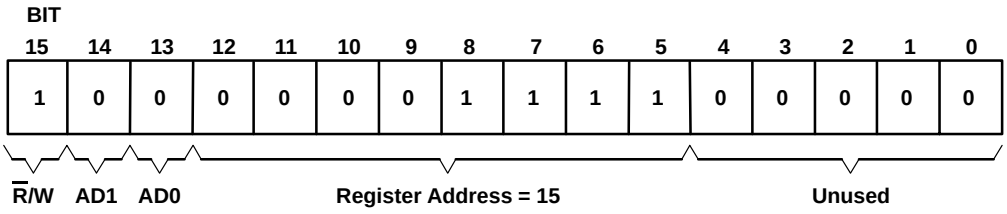


Figure 11. DIN Data Stream for Programming Example 1, Slot 0

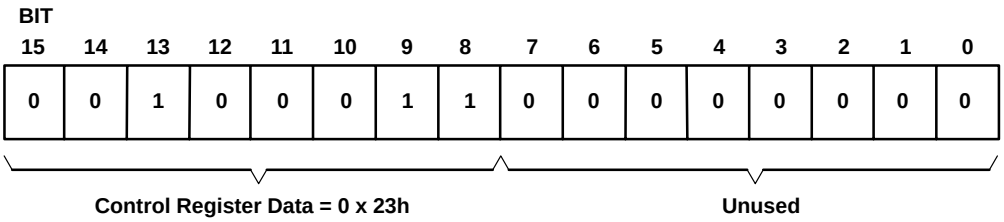


Figure 12. DIN Data Stream for Programming Example 1, Slot 1

The data seen on DOUT in these two time slots is:

Time slot 0: 0000 0000 0000 0000
Time slot 1: 0000 0000 0000 0000

register programming using the serial interface (continued)

Example 2. Read Operation ($\overline{R}$/W = 0):

Requesting a read operation from the device with address 0x00h and reading control register 15 results in the following data being driven on DIN for time slot 0 and 1:

Time slot 0: 0 00 0000 1111 00000
Time slot 1: 0000 0000 0000 0000

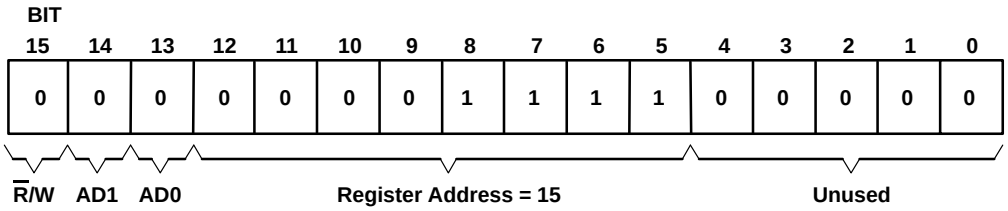


Figure 13. DIN Data Stream for Programming Example 2, Slot 0

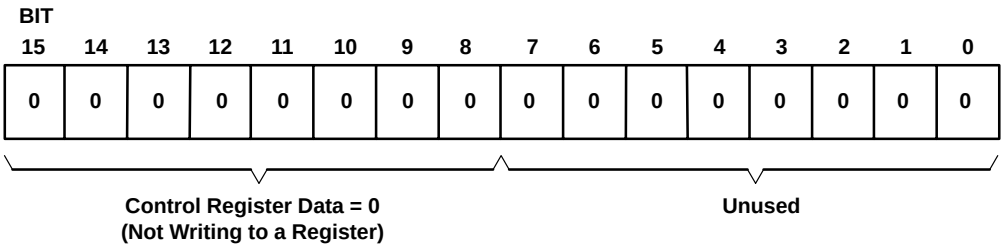


Figure 14. DIN Data Stream for Programming Example 2, Slot 1

DOUT provides the register data in slot 1. If register 15 had been programmed as in example 1 above, then DOUT drives the following data:

Time slot 0: 0000 0000 0000 0000 (data is always 0 in time slot 0 on DOUT)
Time slot 1: 0010 0011 0000 0000

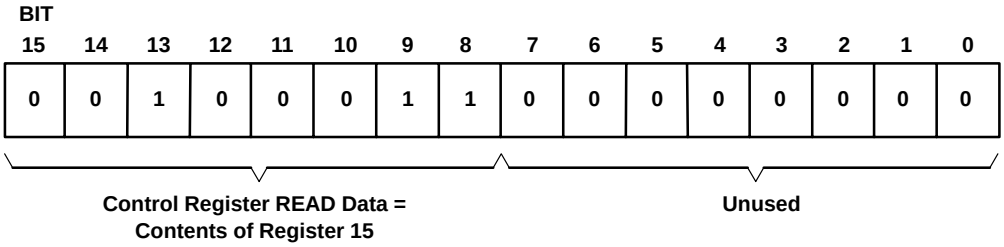


Figure 15. DOUT Data Stream for Programming Example 2, Slot 1

register programming using the I^{2}C bus

The I^{2}C interface is provided to program the registers of the TLV320AIC22 in situations where programming them through the serial interface is not convenient. The I^{2}C interface is selected by setting the I^{2}C/*SPI* pin to logic high. When the I^{2}C interface is selected, data contained in time slots 0 and 1 in the normal serial data transmission is ignored. The I^{2}C interface consists of the following pins:

SCL: I^{2}C-bus serial clock. This input is used to synchronize the data transfer from and to the codec. A maximum clock frequency of 400 kHz is allowed.

register programming using the I²C bus (continued)

SDA: I²C-bus serial address/data input/output. This is a bidirectional pin used to transfer register control address and data into and out of the codec. It is an open-drain terminal and, therefore, requires a pullup resistor to DVDD (typical 10 kΩ for 100 kHz).

AD0: In I²C mode, AD0 is a chip address bit.

AD1: In I²C mode, AD1 is a chip address bit.

Pins AD0 and AD1 form the partial chip address. The upper 5 bits (A6:A2) of the 7-bit address field must be 11100. To communicate with a TLV320AIC22, the LSBs of the chip address field (A1:A0), which is the first byte sent to the TLV320AIC22, should match the settings of the AD1, AD0 pins. For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the start and stop conditions. Data transfer can be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as a start or stop condition.

Table 14. I²C Bus Status

CONDITION	STATUS	DESCRIPTION
A	Bus not busy	Both data and clock lines remain high
B	Start data transfer	A high-to-low transition of the SDA line while the clock (SCL) is high determines a start condition. All commands must proceed from a start condition.
C	Stop data transfer	A low-to-high transition of the SDA line while the clock (SCL) is high determines a stop condition. All operations must end with a stop condition.
D	Data valid	The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal.

I²C-bus conditions

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit data and each data transfer is initiated with a start condition and terminated with a stop condition. The host device determines the number of data bytes transferred between the start and stop conditions. When addressed, the TLV320AIC22 generates an acknowledge after the reception of each byte. The host device (microprocessor or DSP) must generate an extra clock pulse which is associated with this acknowledge bit.

The TLV320AIC22 must pull the SDA line down during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During reads, a host device must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (TLV320AIC22) must leave the data line high to enable the host device to generate the stop condition.

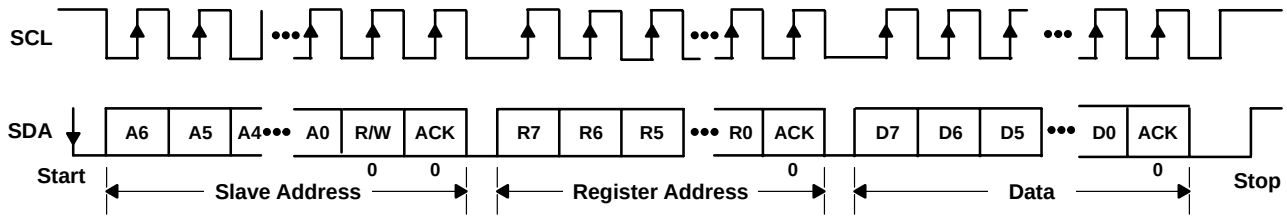


Figure 16. I²C-Bus Write to TLV320AIC22

I²C-bus conditions (continued)

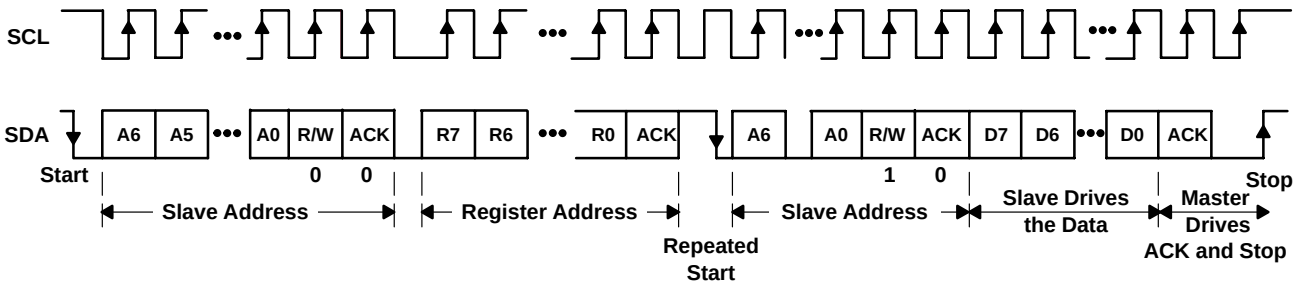
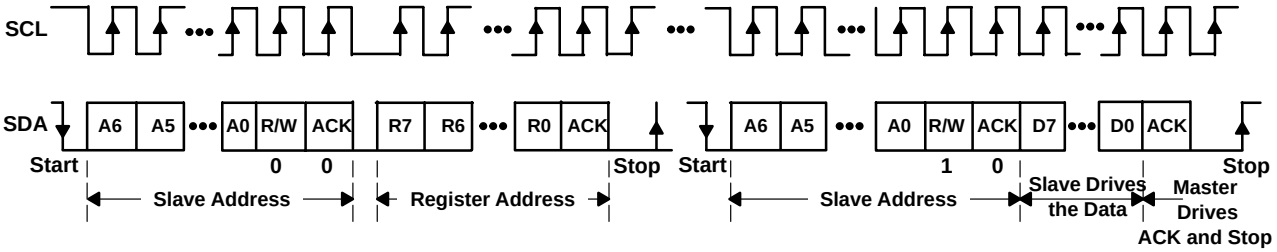


Figure 17. I²C Read From TLV320AIC22 (Protocol A)



NOTE: Slave = TLV320AIC22

Figure 18. I²C Read From TLV320AIC22 (Protocol B)

register functional summary

The following features are register programmable:

- Software reset
- Software power down
- Selection of digital loopback for both channels
- Selection of analog loopback for both channels
- Sample-rate mode selection and selection of I, N, and D (4 bits, 1 to 16) values for both channels
- Analog crosspoint control
  - Analog input for codec 1, selectable from five possible inputs
  - Analog input for codec 2, selectable from five possible inputs
  - Analog output for codec 1, selectable from four possible outputs
  - Analog output for codec 2, selectable from four possible outputs
- Handset input amplifier gain select (mute, 0/14/23 dB)
- Headset input amplifier gain select (mute, 0/14/23 dB)
- Handset and headset echo gain select (mute, –12 dB to –24 dB in steps of 2 dB)
- Microphone input amplifier gain select (mute, 42 dB, 32 dB, 20 dB, or 0 dB)
- Gain selection for the ADC input PGA (mute, 12 dB to –36 dB, in steps of 1.5 dB) and DAC output PGA (mute, 12 dB to –36 dB, in steps of 1.5 dB) for both channels

register functional summary (continued)

- Linear/A-law/μ-law mode select for both codecs
- Independent power down for drivers
- 4-bit DAC voltage control
- High-pass filter bypass for both channels
- Analog-filter pole select (16 kHz, 21.3 kHz, 32 kHz, 64 kHz)
- Zero-crossing enable and threshold
- Number of frames after which control information is to be sent

register map

Registers 1 – 5 and 15 are used to control codec 1.

Registers 6 –10 and 16 are used to control codec 2.

Registers 11 – 14 and 17 are used to configure the device inputs, outputs, and clocking.

control register 1 (for codec 1)

register address = 00000001

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	X	X					Binary number representing the D-register for codec 1 (loaded as D–1)
				X	X	X	X	Binary number representing the N-register for codec 1

Default value: 0101 0000 (D = 6 and N = 0)

control register 2 (for codec 1)

register address = 00000010

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	X	X					Binary number representing the I-register for codec 1 (loaded as I–1)
				1				Analog loopback asserted
				0				Analog loopback not asserted
					1			Digital loopback asserted
					0			Digital loopback not asserted
						1		Codec 1 power down asserted
						0		Codec 1 power down not asserted
							1	Software reset (registers 1 – 5 and 15 are reset to default settings)
							0	Software reset not asserted

Default value: 0101 0000 (I = 6)

register functional summary (continued)

control register 3 (for codec 1)

register address = 00000011

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X								ADC codec overflow indicator
	1	1	0	0	0	0		Codec 1 ADC input PGA gain = mute
	1	0	0	0	0	1		Codec 1 ADC input PGA gain = 12 dB
	1	0	0	0	0	0		Codec 1 ADC input PGA gain = 10.5 dB
	0	1	1	1	1	1		Codec 1 ADC input PGA gain = 9 dB
	0	1	1	1	1	0		Codec 1 ADC input PGA gain = 7.5 dB
	0	1	1	1	0	1		Codec 1 ADC input PGA gain = 6 dB
	0	1	1	1	0	0		Codec 1 ADC input PGA gain = 4.5 dB
	0	1	1	0	1	1		Codec 1 ADC input PGA gain = 3 dB
	0	1	1	0	1	0		Codec 1 ADC input PGA gain = 1.5 dB
	0	1	1	0	0	1		Codec 1 ADC input PGA gain = 0 dB
	0	1	1	0	0	0		Codec 1 ADC input PGA gain = –1.5 dB
	0	1	0	1	1	1		Codec 1 ADC input PGA gain = –3 dB
	0	1	0	1	1	0		Codec 1 ADC input PGA gain = –4.5 dB
	0	1	0	1	0	1		Codec 1 ADC input PGA gain = –6 dB
	0	1	0	1	0	0		Codec 1 ADC input PGA gain = –7.5 dB
	0	1	0	0	1	1		Codec 1 ADC input PGA gain = –9 dB
	0	1	0	0	1	0		Codec 1 ADC input PGA gain = –10.5 dB
	0	1	0	0	0	1		Codec 1 ADC input PGA gain = –12 dB
	0	1	0	0	0	0		Codec 1 ADC input PGA gain = –13.5 dB
	0	0	1	1	1	1		Codec 1 ADC input PGA gain = –15 dB
	0	0	1	1	1	0		Codec 1 ADC input PGA gain = –16.5 dB
	0	0	1	1	0	1		Codec 1 ADC input PGA gain = –18 dB
	0	0	1	1	0	0		Codec 1 ADC input PGA gain = –19.5 dB
	0	0	1	0	1	1		Codec 1 ADC input PGA gain = –21 dB
	0	0	1	0	1	0		Codec 1 ADC input PGA gain = –22.5 dB
	0	0	1	0	0	1		Codec 1 ADC input PGA gain = –24 dB
	0	0	1	0	0	0		Codec 1 ADC input PGA gain = –25.5 dB
	0	0	0	1	1	1		Codec 1 ADC input PGA gain = –27 dB
	0	0	0	1	1	0		Codec 1 ADC input PGA gain = –28.5 dB
	0	0	0	1	0	1		Codec 1 ADC input PGA gain = –30 dB
	0	0	0	1	0	0		Codec 1 ADC input PGA gain = –31.5 dB
	0	0	0	0	1	1		Codec 1 ADC input PGA gain = –33 dB
	0	0	0	0	1	0		Codec 1 ADC input PGA gain = –34.5 dB
	0	0	0	0	0	1		Codec 1 ADC input PGA gain = –36 dB
	0	0	0	0	0	0		Codec 1 ADC input PGA gain = 0 dB
							1	Line output (LNOUT) selected for analog output
							0	Line output (LNOUT) not selected for analog output

Default value: 00000000

register functional summary (continued)

control register 4 (for codec 1)

register address = 00000100

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X							Not used
		1	1	0	0	0	0	Codec 1 DAC output PGA gain = mute
		1	0	0	0	0	1	Codec 1 DAC output PGA gain = 12 dB
		1	0	0	0	0	0	Codec 1 DAC output PGA gain = 10.5 dB
		0	1	1	1	1	1	Codec 1 DAC output PGA gain = 9 dB
		0	1	1	1	1	0	Codec 1 DAC output PGA gain = 7.5 dB
		0	1	1	1	0	1	Codec 1 DAC output PGA gain = 6 dB
		0	1	1	1	0	0	Codec 1 DAC output PGA gain = 4.5 dB
		0	1	1	0	1	1	Codec 1 DAC output PGA gain = 3 dB
		0	1	1	0	1	0	Codec 1 DAC output PGA gain = 1.5 dB
		0	1	1	0	0	1	Codec 1 DAC output PGA gain = 0 dB
		0	1	1	0	0	0	Codec 1 DAC output PGA gain = –1.5 dB
		0	1	0	1	1	1	Codec 1 DAC output PGA gain = –3 dB
		0	1	0	1	1	0	Codec 1 DAC output PGA gain = –4.5 dB
		0	1	0	1	0	1	Codec 1 DAC output PGA gain = –6 dB
		0	1	0	1	0	0	Codec 1 DAC output PGA gain = –7.5 dB
		0	1	0	0	1	1	Codec 1 DAC output PGA gain = –9 dB
		0	1	0	0	1	0	Codec 1 DAC output PGA gain = –10.5 dB
		0	1	0	0	0	1	Codec 1 DAC output PGA gain = –12 dB
		0	1	0	0	0	0	Codec 1 DAC output PGA gain = –13.5 dB
		0	0	1	1	1	1	Codec 1 DAC output PGA gain = –15 dB
		0	0	1	1	1	0	Codec 1 DAC output PGA gain = –16.5 dB
		0	0	1	1	0	1	Codec 1 DAC output PGA gain = –18 dB
		0	0	1	1	0	0	Codec 1 DAC output PGA gain = –19.5 dB
		0	0	1	0	1	1	Codec 1 DAC output PGA gain = –21 dB
		0	0	1	0	1	0	Codec 1 DAC output PGA gain = –22.5 dB
		0	0	1	0	0	1	Codec 1 DAC output PGA gain = –24 dB
		0	0	1	0	0	0	Codec 1 DAC output PGA gain = –25.5 dB
		0	0	0	1	1	1	Codec 1 DAC output PGA gain = –27 dB
		0	0	0	1	1	0	Codec 1 DAC output PGA gain = –28.5 dB
		0	0	0	1	0	1	Codec 1 DAC output PGA gain = –30 dB
		0	0	0	1	0	0	Codec 1 DAC output PGA gain = –31.5 dB
		0	0	0	0	1	1	Codec 1 DAC output PGA gain = –33 dB
		0	0	0	0	1	0	Codec 1 DAC output PGA gain = –34.5 dB
		0	0	0	0	0	1	Codec 1 DAC output PGA gain = –36 dB
		0	0	0	0	0	0	Codec 1 DAC output PGA gain = 0 dB

Default value: 00000000

register functional summary (continued)

control register 5 (for codec 1)

register address = 00000101

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1								Handset input (HSIN) selected for analog input
0								Handset input (HSIN) not selected for analog input
	1							Headset input (HDIN) selected for analog input
	0							Headset input (HDIN) not selected for analog input
		1						Microphone input (MCIN) selected for analog input
		0						Microphone input (MCIN) not selected for analog input
			1					Line input (LNIN) selected for analog input
			0					Line input (LNIN) not selected for analog input
				1				CallerID amplifier input (CIIN) selected for analog input
				0				CallerID amplifier input (CIIN) not selected for analog input
					1			Handset output (HSOUT) selected for analog output
					0			Handset output (HSOUT) not selected for analog output
						1		Headset output (HDOUT) selected for analog output
						0		Headset output (HDOUT) not selected for analog output
							1	Speaker output (SPOUT) selected for analog output
							0	Speaker output (SPOUT) not selected for analog output

Default value: 1000 0100

control register 6 (for codec 2)

register address = 00000110

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	X	X					Binary number representing the D-register for codec 2 (loaded as D–1)
				X	X	X	X	Binary number representing the N-register for codec 2

Default value: 0101 0000 (D = 6 and N = 0)

control register 7 (for codec 2)

register address = 00000111

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	X	X					Binary number representing the I-register for codec 2 (loaded as I–1)
				1				Analog loopback asserted
				0				Analog loopback not asserted
					1			Digital loopback asserted
					0			Digital loopback not asserted
						1		Codec 2 power down asserted
						0		Codec 2 power down not asserted
							1	Software reset
							0	Software reset not asserted

Default value: 0101 0000 (I = 6)

register functional summary (continued)

control register 8 (for codec 2)

register address = 00001000

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X								ADC codec overflow indicator
	1	1	0	0	0	0		Codec 2 ADC input PGA gain = mute
	1	0	0	0	0	1		Codec 2 ADC input PGA gain = 12 dB
	1	0	0	0	0	0		Codec 2 ADC input PGA gain = 10.5 dB
	0	1	1	1	1	1		Codec 2 ADC input PGA gain = 9 dB
	0	1	1	1	1	0		Codec 2 ADC input PGA gain = 7.5 dB
	0	1	1	1	0	1		Codec 2 ADC input PGA gain = 6 dB
	0	1	1	1	0	0		Codec 2 ADC input PGA gain = 4.5 dB
	0	1	1	0	1	1		Codec 2 ADC input PGA gain = 3 dB
	0	1	1	0	1	0		Codec 2 ADC input PGA gain = 1.5 dB
	0	1	1	0	0	1		Codec 2 ADC input PGA gain = 0 dB
	0	1	1	0	0	0		Codec 2 ADC input PGA gain = –1.5 dB
	0	1	0	1	1	1		Codec 2 ADC input PGA gain = –3 dB
	0	1	0	1	1	0		Codec 2 ADC input PGA gain = –4.5 dB
	0	1	0	1	0	1		Codec 2 ADC input PGA gain = –6 dB
	0	1	0	1	0	0		Codec 2 ADC input PGA gain = –7.5 dB
	0	1	0	0	1	1		Codec 2 ADC input PGA gain = –9 dB
	0	1	0	0	1	0		Codec 2 ADC input PGA gain = –10.5 dB
	0	1	0	0	0	1		Codec 2 ADC input PGA gain = –12 dB
	0	1	0	0	0	0		Codec 2 ADC input PGA gain = –13.5 dB
	0	0	1	1	1	1		Codec 2 ADC input PGA gain = –15 dB
	0	0	1	1	1	0		Codec 2 ADC input PGA gain = –16.5 dB
	0	0	1	1	0	1		Codec 2 ADC input PGA gain = –18 dB
	0	0	1	1	0	0		Codec 2 ADC input PGA gain = –19.5 dB
	0	0	1	0	1	1		Codec 2 ADC input PGA gain = –21 dB
	0	0	1	0	1	0		Codec 2 ADC input PGA gain = –22.5 dB
	0	0	1	0	0	1		Codec 2 ADC input PGA gain = –24 dB
	0	0	1	0	0	0		Codec 2 ADC input PGA gain = –25.5 dB
	0	0	0	1	1	1		Codec 2 ADC input PGA gain = –27 dB
	0	0	0	1	1	0		Codec 2 ADC input PGA gain = –28.5 dB
	0	0	0	1	0	1		Codec 2 ADC input PGA gain = –30 dB
	0	0	0	1	0	0		Codec 2 ADC input PGA gain = –31.5 dB
	0	0	0	0	1	1		Codec 2 ADC input PGA gain = –33 dB
	0	0	0	0	1	0		Codec 2 ADC input PGA gain = –34.5 dB
	0	0	0	0	0	1		Codec 2 ADC input PGA gain = –36 dB
	0	0	0	0	0	0		Codec 2 ADC input PGA gain = 0 dB
							1	Line output (LNOUT) selected for analog output
							0	Line output (LNOUT) not selected for analog output

Default value: 00000001

register functional summary (continued)

control register 9 (for codec 2)

register address = 00001001

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X							Don't care
		1	1	0	0	0	0	Codec 2 DAC output PGA gain = mute
		1	0	0	0	0	1	Codec 2 DAC output PGA gain = 12 dB
		1	0	0	0	0	0	Codec 2 DAC output PGA gain = 10.5 dB
		0	1	1	1	1	1	Codec 2 DAC output PGA gain = 9 dB
		0	1	1	1	1	0	Codec 2 DAC output PGA gain = 7.5 dB
		0	1	1	1	0	1	Codec 2 DAC output PGA gain = 6 dB
		0	1	1	1	0	0	Codec 2 DAC output PGA gain = 4.5 dB
		0	1	1	0	1	1	Codec 2 DAC output PGA gain = 3 dB
		0	1	1	0	1	0	Codec 2 DAC output PGA gain = 1.5 dB
		0	1	1	0	0	1	Codec 2 DAC output PGA gain = 0 dB
		0	1	1	0	0	0	Codec 2 DAC output PGA gain = –1.5 dB
		0	1	0	1	1	1	Codec 2 DAC output PGA gain = –3 dB
		0	1	0	1	1	0	Codec 2 DAC output PGA gain = –4.5 dB
		0	1	0	1	0	1	Codec 2 DAC output PGA gain = –6 dB
		0	1	0	1	0	0	Codec 2 DAC output PGA gain = –7.5 dB
		0	1	0	0	1	1	Codec 2 DAC output PGA gain = –9 dB
		0	1	0	0	1	0	Codec 2 DAC output PGA gain = –10.5 dB
		0	1	0	0	0	1	Codec 2 DAC output PGA gain = –12 dB
		0	1	0	0	0	0	Codec 2 DAC output PGA gain = –13.5 dB
		0	0	1	1	1	1	Codec 2 DAC output PGA gain = –15 dB
		0	0	1	1	1	0	Codec 2 DAC output PGA gain = –16.5 dB
		0	0	1	1	0	1	Codec 2 DAC output PGA gain = –18 dB
		0	0	1	1	0	0	Codec 2 DAC output PGA gain = –19.5 dB
		0	0	1	0	1	1	Codec 2 DAC output PGA gain = –21 dB
		0	0	1	0	1	0	Codec 2 DAC output PGA gain = –22.5 dB
		0	0	1	0	0	1	Codec 2 DAC output PGA gain = –24 dB
		0	0	1	0	0	0	Codec 2 DAC output PGA gain = –25.5 dB
		0	0	0	1	1	1	Codec 2 DAC output PGA gain = –27 dB
		0	0	0	1	1	0	Codec 2 DAC output PGA gain = –28.5 dB
		0	0	0	1	0	1	Codec 2 DAC output PGA gain = –30 dB
		0	0	0	1	0	0	Codec 2 DAC output PGA gain = –31.5 dB
		0	0	0	0	1	1	Codec 2 DAC output PGA gain = –33 dB
		0	0	0	0	1	0	Codec 2 DAC output PGA gain = –34.5 dB
		0	0	0	0	0	1	Codec 2 DAC output PGA gain = –36 dB
		0	0	0	0	0	0	Codec 2 DAC output PGA gain = 0 dB

Default value: 00000000

register functional summary (continued)

control register 10 (for codec 2)

register address = 00001010

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1								Handset input (HSIN) selected for analog input
0								Handset input (HSIN) not selected for analog input
	1							Headset input (HDIN) selected for analog input
	0							Headset input (HDIN) not selected for analog input
		1						Microphone input (MCIN) selected for analog input
		0						Microphone input (MCIN) not selected for analog input
			1					Line input (LNIN) selected for analog input
			0					Line input (LNIN) not selected for analog input
				1				CallerID amplifier input (CIIN) selected for analog input
				0				CallerID amplifier input (CIIN) not selected for analog input
					1			Handset output (HSOUT) selected for analog output
					0			Handset output (HSOUT) not selected for analog output
						1		Headset output (HDOUT) selected for analog output
						0		Headset output (HDOUT) not selected for analog output
							1	Speaker output (SPOUT) selected for analog output
							0	Speaker output (SPOUT) not selected for analog output

Default value: 0001 0000

control register 11

register address = 00001011

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	0							Handset input amplifier gain = 14 dB
0	1							Handset input amplifier gain = 23 dB
1	0							Handset input amplifier gain = mute
1	1							Handset input amplifier gain = 0 dB
		0	0					Headset input amplifier gain = 14 dB
		0	1					Headset input amplifier gain = 23 dB
		1	0					Headset input amplifier gain = mute
		1	1					Headset input amplifier gain = 0 dB
				0	0	0		Microphone input amplifier gain = 32 dB
				0	0	1		Microphone input amplifier gain = 20 dB
				0	1	0		Microphone input amplifier gain = 42 dB
				0	1	1		Microphone input amplifier gain = 0 dB
				1	1	1		Microphone input amplifier gain = mute
							1	Speaker output powered down (mute)
							0	Speaker output enabled

Default value: 0000 0001

register functional summary (continued)

control register 12

register address = 00001100

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X								Don't care
	0	0	0					FSYNC is 8 kHz for MCLK = 24.576 MHz
	0	0	1					FSYNC is 8 kHz for MCLK = 32.768 MHz
	0	1	0					FSYNC is 16 kHz for MCLK = 24.576 MHz
	0	1	1					FSYNC is 16 kHz for MCLK = 32.768 MHz
	1	0	0					Reserved
	1	0	1					FSYNC is 64 kHz for MCLK = 32.768 MHz and 48 kHz for MCLK = 24.576 MHz
	1	1	0					Reserved
	1	1	1					Reserved
				X	X	X	X	LCD DAC output voltage = 1.5 + (3/16) x (decimal value)

Default value: 0000 0000

control register 13

register address = 00001101

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1								Handset output powered down (mute)
0								Handset output enabled
	X							Don't care
		X						Don't care
			0	0	0			Handset echo gain = –12 dB
			0	0	1			Handset echo gain = –14 dB
			0	1	0			Handset echo gain = –16 dB
			0	1	1			Handset echo gain = –18 dB
			1	0	0			Handset echo gain = –20 dB
			1	0	1			Handset echo gain = –22 dB
			1	1	0			Handset echo gain = –24 dB
			1	1	1			Handset echo gain = mute
						1		Data-valid flag is disabled.
						0		Data-valid flag is enabled. The fifteenth bit (MSB) of the 16-bit data word transmitted from the TLV320AIC22 indicates that the data is valid (bit 15 = 1) or invalid (bit 15 = 0)
							X	Don't care

Default value: 0000 0000

register functional summary (continued)

control register 14

register address = 00001110

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1								Headset output powered down (mute)
0								Headset output enabled
	0	0						Analog pole-select for line amplifier. Filter pole at 64 kHz
	0	1						Analog pole-select for line amplifier. Filter pole at 32 kHz
	1	0						Analog pole-select for line amplifier. Filter pole at 21.3 kHz
	1	1						Analog pole-select for line amplifier. Filter pole at 16 kHz
			0	0	0			Headset echo gain = –12 dB
			0	0	1			Headset echo gain = –14 dB
			0	1	0			Headset echo gain = –16 dB
			0	1	1			Headset echo gain = –18 dB
			1	0	0			Headset echo gain = –20 dB
			1	0	1			Headset echo gain = –22 dB
			1	1	0			Headset echo gain = –24 dB
			1	1	1			Headset echo gain = mute
						1		Analog master power down active. Entire analog section is powered down.
						0		Analog master power down not active
							1	Line output, line input amplifiers powered down; VCOM is floating
							0	Line output, line input and VCOM are enabled

Default value: 0000 0000

control register 15 (for codec 1)

register address = 00001111

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	X							Linear mode selected
1	0							A-law mode selected
1	1							μ-law mode selected
		1						Zero crossing disabled for ADC
		0						Zero crossing enabled for ADC
			1					Zero crossing disabled for DAC
			0					Zero crossing enabled for DAC
				1				ADC channel high-pass filter bypassed
				0				ADC channel high-pass filter not bypassed
					1			Zero crossing disabled
					0			Zero crossing enabled
						0	0	Number of LSBs used to determine the zero-crossing threshold = 6
						0	1	Number of LSBs used to determine the zero-crossing threshold = 4
						1	0	Number of LSBs used to determine the zero-crossing threshold = 8
						1	1	Number of LSBs used to determine the zero-crossing threshold = 10

Default value: 0000 0000

register functional summary (continued)

control register 16 (for codec 2)

register address = 00010000

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	X							Linear mode selected
1	0							A-law mode selected
1	1							μ-law mode selected
		1						Zero crossing disabled for ADC
		0						Zero crossing enabled for ADC
			1					Zero crossing disabled for DAC
			0					Zero crossing enabled for DAC
				1				ADC channel high-pass filter bypassed
				0				ADC channel high-pass filter not bypassed
					1			Zero crossing disabled
					0			Zero crossing enabled
						0	0	Number of LSBs used to determine the zero-crossing threshold = 6
						0	1	Number of LSBs used to determine the zero-crossing threshold = 4
						1	0	Number of LSBs used to determine the zero-crossing threshold = 8
						1	1	Number of LSBs used to determine the zero-crossing threshold = 10

Default value: 0000 0000

control register 17

register address = 00010001

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	X	X	X	X	X	X	Number of frames that do not contain control information present between frames containing control information. Loading zero makes control information present in every frame.

Default value: 0000 0000

APPLICATION INFORMATION

TLV320AIC22-to-DSP interface

The TLV320AIC22 interfaces gluelessly to the McBSP port of a C54x or C6x TI DSP. Figure 19 shows a single TLV320AIC22 connected to a C54x or C6x TI DSP. Figure 20 shows multiple TLV320AIC22s connected to a single McBSP port (master/slave functionality).

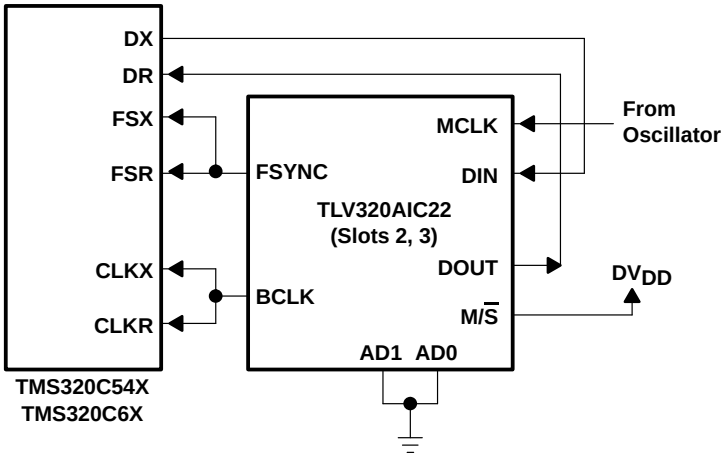


Figure 19. TLV320AIC22s Interface to McBSP Port of C54x or C6x DSP

APPLICATION INFORMATION

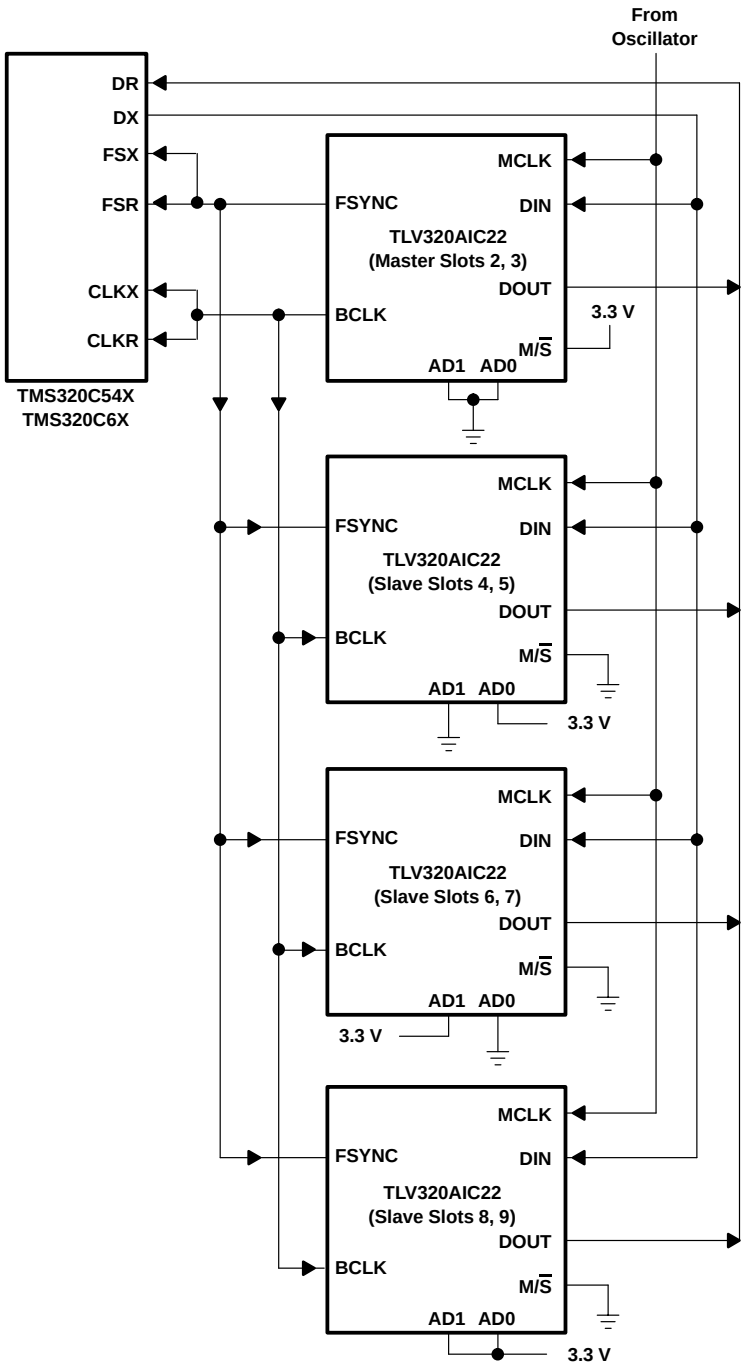


Figure 20. Four TLV320AIC22s Cascaded to Provide Eight Channels

APPLICATION INFORMATION

hybrid-circuit external connections

The TLV320AIC22 connected to the telephone line using the LNIN and LNOUT hybrid circuit is shown in Figure 21.

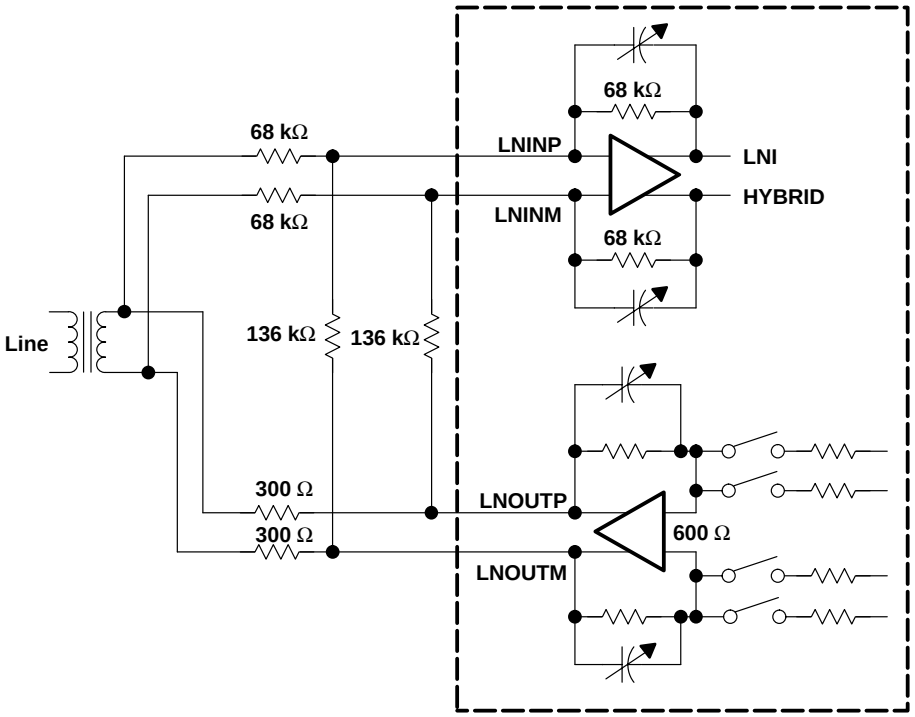


Figure 21. Hybrid-Circuit External Connections

APPLICATION INFORMATION

microphone, handset, and headset external connections

The microphone, headset, and handset external connections are shown in Figure 22. The suggested discrete components, with their values, also are included.

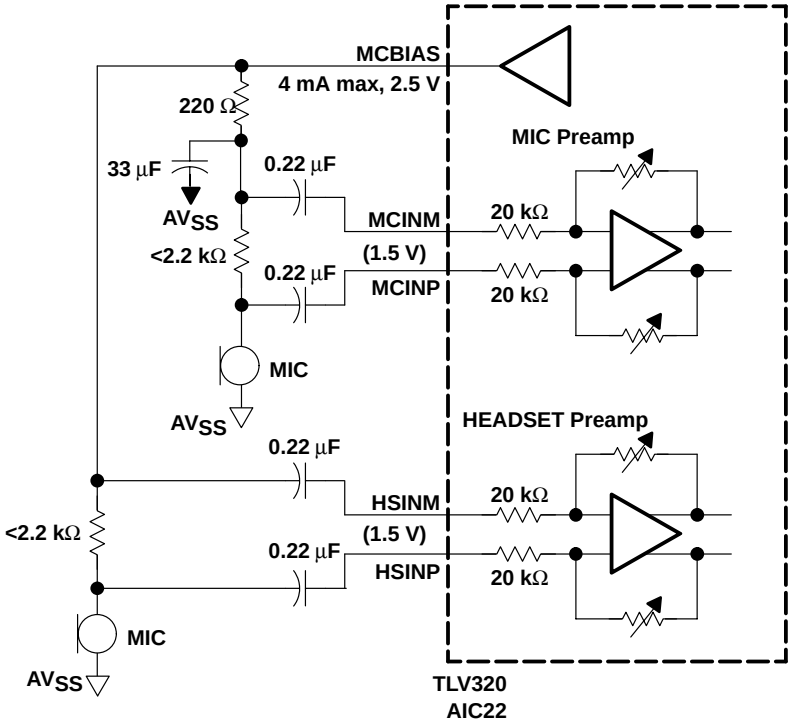


Figure 22. MIC/Handset/Headset External Connections

callerID interface

The callerID amplifier interface to the telephone line is shown in Figure 23.

The value for Rx is 365 kΩ (E96 series, which has 1% tolerance). Cx is 470 pF (10% tolerance) of high-voltage rating. Voltage rating is determined based on the telecom standards of the country. The typical value is 1 kV. The callerID input can be used as a lower performance line input. For this application, a larger value capacitor is required for Cx.

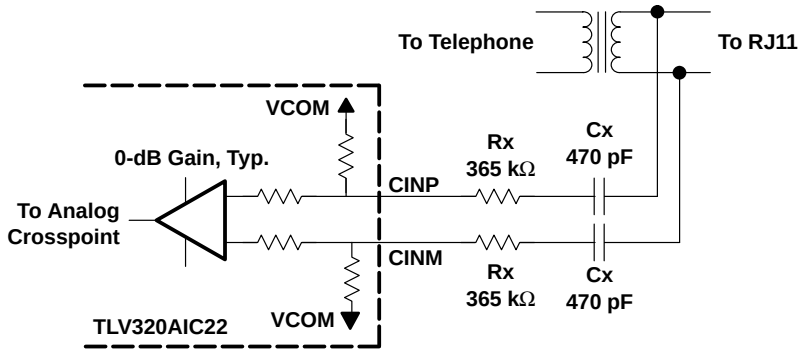
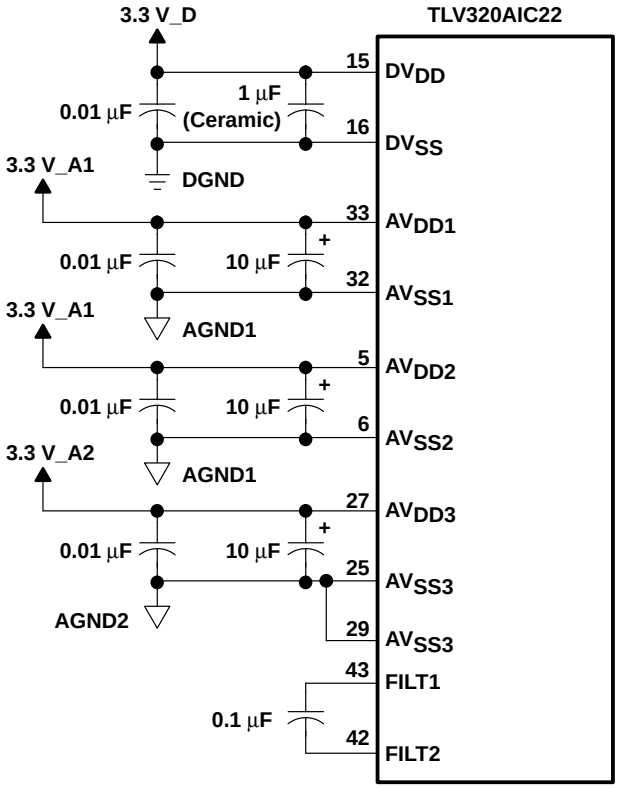


Figure 23. Typical Application Circuit for CallerID Amplifiers

APPLICATION INFORMATION

recommended power-supply decoupling

The recommended power-supply decoupling for the TLV320AIC22 is shown in Figure 24. Both high-frequency and bulk decoupling capacitors are suggested. The high-frequency capacitors should be X7R type capacitors or better. A 1-µF ceramic capacitor should be used to decouple the digital power supply.



3.3 V_D = 3.3-V Digital Power **3.3 V_A1 = 3.3-V Analog Power** **3.3 V_A2 = Separate 3.3-V Analog Power**
DGND = Digital Ground **AGND1 = Analog Ground** **AGND2 = Separate Analog Ground**

Figure 24. Recommended Decoupling

suggested configuration sequence

The default settings for the TLV320AIC22 are shown in Table 15.

Table 15. Default Codec Settings

CODEC 1 DEFAULT SETTINGS	CODEC 2 DEFAULT SETTINGS
I = 6, N = 0, D = 6	Same as codec 1
Analog and digital loopback not asserted	Same as codec 1
Codec power down not asserted	Same as codec 1
Software reset not asserted	Same as codec 1
ADC input PGA gain set for 0 dB	Same as codec 1
DAC output PGA gain set to 0 dB	Same as codec 1
Handset input selected for analog input	Line output selected for analog output
Handset output selected for analog output	Line input selected for analog input

APPLICATION INFORMATION

suggested configuration sequence (continued)

Other default settings include:

- Handset and headset input amplifier gains are set to 14 dB.
- Microphone input amplifier gain is set to 32 dB.
- Speaker output is powered down (muted).
- FSYNC is 8 kHz, MCLK = 24.576 MHz.
- LCD DAC output voltage is 1.5 V.
- Handset output is enabled, with echo gain set to –12 dB.
- Headset output is enabled, with echo gain set to –12 dB.
- Data-valid flag is enabled in ADC data.
- Line input, output and VCOM are enabled.
- Analog circuitry is powered up.
- Line amplifier has a filter pole at 64 kHz.
- Control information sent every frame
- Data-valid flag enabled for output data

If the default settings are not adequate, the user can reconfigure the registers settings. An example configuration sequence after power has been applied to the TLV320AIC22 is:

1. Wait 10 μs after the $\overline{\text{RESET}}$ has been deasserted.
2. Disable the analog outputs by programming the appropriate bits in registers 11, 13, and 14.
3. Program control register 12 for the desired MCLK and FSYNC frequencies.
4. Program control registers 1, 2, 6, and 7 to configure the I, N, and D values.
5. Select the desired codec analog input and output paths by programming control registers 3 and 5 for codec 1 and registers 8 and 10 for codec 2. This configures the analog crosspoint.
6. Program control registers 15 (for codec 1) and 16 (for codec 2) to select the conversion mode (A-law/μ-law/linear), the number of LSBs for the zero crossing (if enabled), and the ADC IIR filter enable/bypass.
7. Program the analog input and output gains in registers 3 and 4 for codec 1, and registers 8 and 9 for codec 2.
8. Program the handset, headset, and microphone gains (if required) in registers 11, 13, and 14.
9. Change the LCD DAC voltage (if required) by programming register 12.
10. Program how often the control information is sent via the serial interface in control register 17, if control words are not required every frame.
11. Enable the analog outputs by programming registers 11, 13, and 14.

APPLICATION INFORMATION

TLV320AIC22 DAC path-clipping avoidance

If large signals are input to either codec's DAC at the DIN pin, internal clipping of the signals can occur. The result is undesired signal distortion at the analog output of each DAC. To avoid signal distortion induced by clipping in the TLV320AIC22 DAC path, the following is recommended:

1. For linear operation:

- Always reduce the DAC signal input levels by 6 dB for each codec. This will ensure that large signals approaching digital full-scale amplitude will not cause clipping.
- Program each codec's internal programmable gain amplifier (PGA) for the desired overall channel gain, plus 6 dB. The PGA for codec 1 is programmed via control register 3. The PGA for codec 2 is programmed via control register 8.

Examples are provided in Table 16.

Table 16. Examples of Signal Attenuation and PGA Gain Settings for Various Overall Channel Gains

OVERALL DESIRED CHANNEL GAIN	INPUT LEVEL BEFORE –6-dB APPLICATION	INPUT LEVEL AFTER –6-dB APPLICATION	PGA GAIN
0 dB	0 dB	–6 dB	6 dB
0 dB	–6 dB	–12 dB	6 dB
–27 dB	0 dB	–6 dB	–21 dB
–27 dB	–12 dB	–18 dB	–21 dB

2. PCM companded (μ-Law or A-Law) operation:

Because μ-Law and A-Law transmission levels often are referenced in terms of dBm0, receive channel-input levels limits can be noted in terms of dBm0. The signal-level 0 dBm0 is the digital milliwatt transmission level, as addressed in the International Telecommunication Union (ITU) specification G.711. The ITU G.711 specification also shows the theoretical load capacity of the A-Law as 3.14 dBm0 and 3.17 dBm0 for the μ-Law.

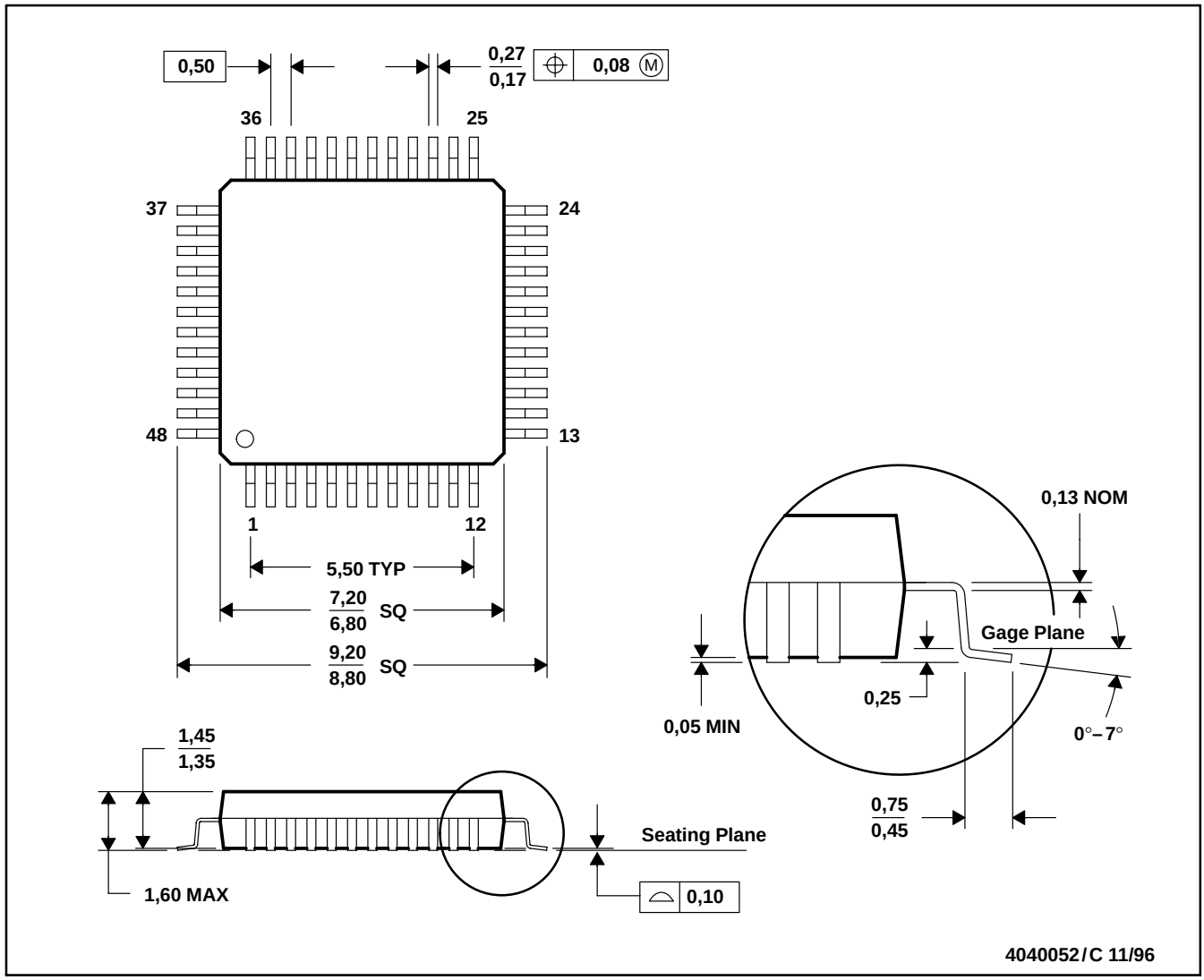
- Fundamentally, apply the same procedure as outlined in step 1 for linear operation.
- When using terms of dBm0, restrict A-Law signal levels to –2.88 dBm0 and μ-Law signal levels to –3.02 dBm0 signal levels. These levels correspond to A-Law and μ-Law to linear mapping codes that reflect a 6-dB or greater reduction in signal level.

performance issues associated with the recommended action to avoid signal clipping in the TLV320AIC22

The recommended action requires the attenuation of input signals by 6 dB prior to input to either codec's DAC on the device. The internal DAC path PGA should be programmed so that the desired channel gain and recovery of the 6-dB input signal attenuation is accomplished. Loss of a least significant bit (LSB) of information is typical by attenuating digital signals by 6 dB and can result in degraded signal-to-noise (SNR) performance. For the TLV320AIC22 DAC path, the recommended action described above to avoid signal clipping results in degradation of SNR performance typically less than 0.5 dB for signals larger than 5 LSBs and less than 2 dB for signals larger than 2 LSBs.

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV320AIC22PT	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI
TLV320AIC22PTR	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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