Product Document

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TMG3992

Gesture, Color, ALS, and Proximity Sensor Module with mobeam™ Barcode Emulation

General Description

The device features advanced Gesture detection, Proximity detection, Digital Ambient Light Sense (ALS), Color Sense (RGBC), and optical pattern generation/transmission for broadcast. The slim modular package, 2.0mm × 3.95mm × 1.36mm, incorporates an IR LED and factory calibrated LED driver.

Gesture detection utilizes four directional photodiodes to sense reflected IR energy (sourced by the integrated LED) to convert physical motion information (i.e. velocity, direction and distance) to a digital information. The architecture of the gesture engine features automatic activation (based on Proximity engine results), ambient light subtraction, cross-talk cancelation, dual 8-bit data converters, power saving inter-conversion delay, 32-dataset FIFO, and interrupt driven I^2C communication. The gesture engine accommodates a wide range of mobile device gesturing requirements: simple North-South-East-West gestures or more complex gestures can be accurately sensed. Power consumption and noise are minimized with adjustable IR LED timing.

The Proximity detection feature provides object detection (E.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur whenever proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for system offset caused by unwanted IR energy reflections appearing at the sensor. The IR LED intensity is factory trimmed to eliminate the need for end-equipment calibration due to component variations. Proximity results are further improved by automatic ambient light subtraction.

The Color and ALS detection feature provides red, green, blue and clear light intensity data. Each of the R, G, B, C channels have a UV and IR blocking filter and a dedicated data converter producing16-bit data simultaneously. This architecture allows applications to accurately measure ambient light and sense color which enables devices to calculate illuminance and color temperature, control display backlight, and chromaticity.

mobeam™ barcode emulation is achieved using the IRBeam optical pattern generation/transmission feature. IRBeam is primarily intended for 1-D barcode transmission over IR to point-of-sale (POS) terminals. The IRBeam engine features a 1024-bit RAM for pattern storage and specialized control logic that is tailored to repetitively broadcast a barcode pattern using the integrated LED. The IRBeam engine features adjustable timing, looping, and IR intensity to maximize successful barcode reception rate among the multitude of different barcode scanner/readers currently in use globally.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMG3992, Gesture, Color, ALS, and Proximity Sensor Module with mobeam™ Barcode Emulation are listed below:

Figure 1:
Added Value of using TMG3992

Benefits	Features
• Single Device Integrated Optical Solution	• Gesture Detection, Proximity, Color/ALS and IRBeam Support • Power Management Features
• Ambient Light Sensing	• UV and IR blocking filters • Programmable Gain & Integration Time • 16.7M:1 Dynamic Range
• Complex Gesture Sensing	• Four separate diodes sensitive to different directions • Ambient Light Rejection • Offset Compensation • Programmable Driver for IR LED current • 32 Dataset storage FIFO • Interrupt Driven I^2C Communication
• Ideal for Operation Behind Dark Glass	• Very High Sensitivity
• Proximity Detection	• Trimmed to provide consistent reading • Ambient Light Rejection • Proximity Offset Compensation • Saturation Indicator bit • Programmable Driver for IR LED current • 98000:1 Dynamic Range
• Barcode Pattern Generation and Transmission	• IRBeam Hardware Support • Pattern Storage in Internal RAM
• Dual Use of a Single Internal LED	• Integrated LED driver with current control for both Proximity and IRBeam

Applications

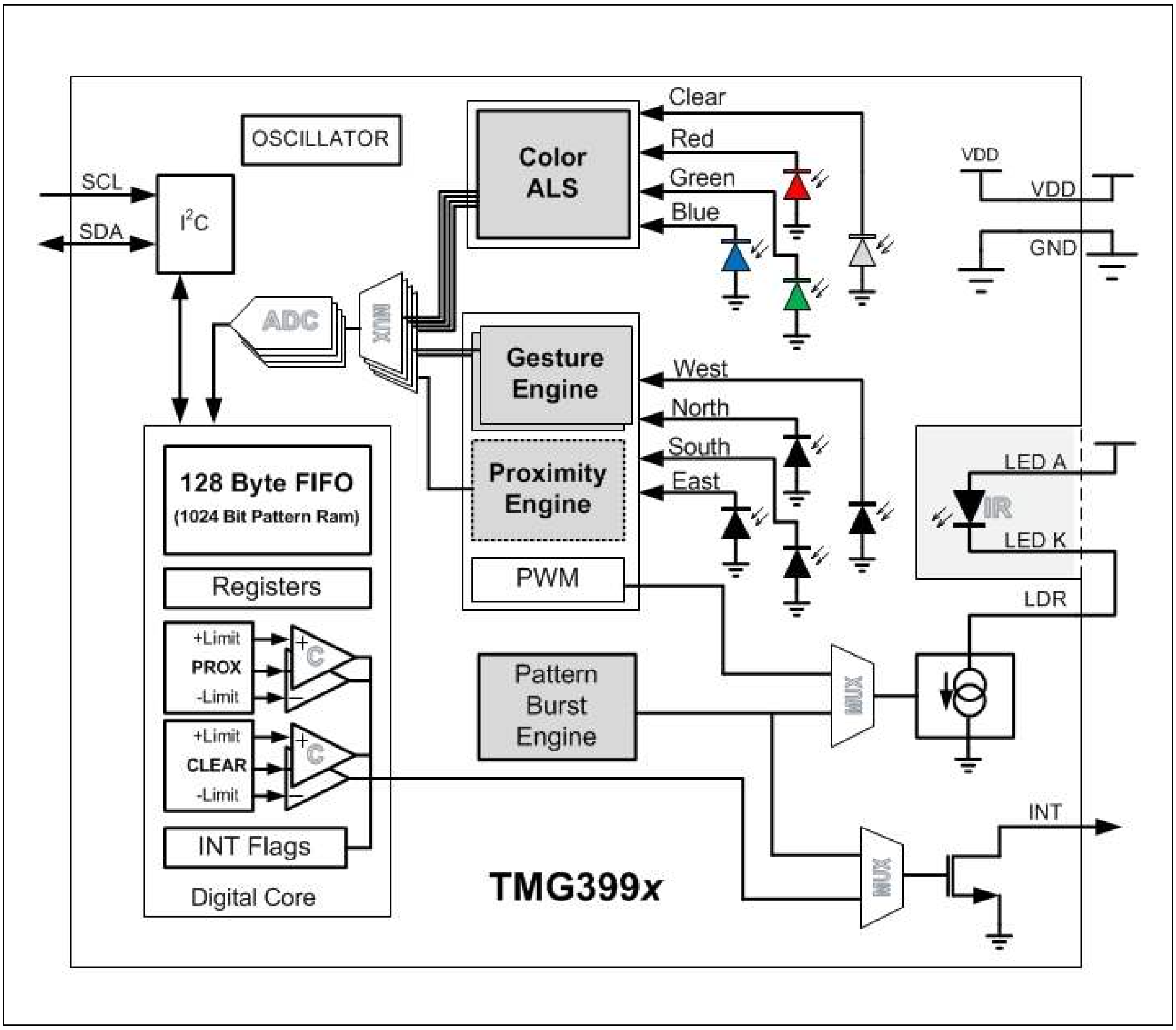
The TMG399x applications include:

- Gesture Detection
- Color Sense
- Ambient Light Sensing
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement
- Printed Bar Code Emulation

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TMG3992 Block Diagram



Block Diagram: "Pattern Burst Engine" is used for IRBeam operational mode.

Pin Assignment

The TMG3992 pin assignments are described below.

Figure 3:
Pin Diagram

(Top View)
Package drawing is not to scale.

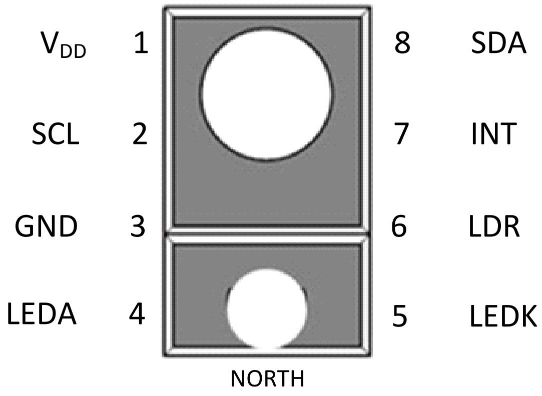


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	V_{DD}	Supply voltage.
2	SCL	I^2C serial clock input terminal.
3	GND	Ground. All voltages are referenced to GND.
4	LEDA	LED Anode.
5	LEDK	LED Cathode. Connect to LDR pin when using internal LED driver circuit.
6	LDR	LED drive. Current sink for LED.
7	INT	Interrupt. Open drain output (active low) and logic level output for external IR LED circuit.
8	SDA	I^2C serial data I/O terminal.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings (all voltages with respect to GND)

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Supply voltage		3.8	V	All voltages are with respect to GND
LEDA	Supply voltage		4.8	V	T_A = 0°C to 70°C
			4.4	V	T_A = -30°C to 85°C
	Digital I/O terminal voltage	- 0.5	3.8	V	
LDR	Max voltage		4.4	V	T_A = -30°C to 85°C (1)
			4.8	V	T_A = 0°C to 70°C (1)
			3.8	V	T_A = -30°C to 85°C (2)
(SDA, INT)	Output terminal current	- 1	20	mA	
T_{STRG}	Storage temperature range	- 40	85	°C	
ESD_{HBM}	ESD tolerance, human body model	±2000		V	

Note(s):

1. Measured with LDR = OFF.
2. LDR = ON.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	2.4	3	3.6	V
T_A	Operating free-air temperature (1)	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Specifications are stated at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency		3.525	3.675	3.825	MHz
IDD	Supply current (1)	Active ALS state (PON=AEN=1, PEN=PBEN=0)		220	330	µA
		Low slew rate (PON=PBEN=1, AEN=PEN=SLEW=0)		560		
		High slew rate (PON=PBEN=SLEW=1, AEN=PEN=0)		650		
		Proximity, During LDR Pulse (PPULSE: 8 pulses) (2)		790		
		Gesture, During LDR Pulse (GPULSE = 8) (3)		790		
		Wait state (PON=1, AEN=PEN=PBEN=0)		38		
		Sleep state (4)		1.0	10	
VOL	INT, SDA output low voltage	3 mA sink current 6 mA sink current	0 0		0.4 0.6	V

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td rowspan="2">ILEAK</td><td>Leakage current, SDA, SCL, INT pins</td><td></td><td>−5</td><td></td><td>5</td><td rowspan="2">µA</td></tr>
<tr><td>Leakage current, LDR pin</td><td></td><td>−10</td><td></td><td>10</td></tr>
<tr><td rowspan="2">VIH</td><td rowspan="2">SCL, SDA input high voltage</td><td>TMG39921
TMG39925</td><td>0.7 V_{DD}</td><td></td><td></td><td rowspan="2">V</td></tr>
<tr><td>TMG39923
TMG39927</td><td>1.26</td><td></td><td></td></tr>
<tr><td rowspan="2">VIL</td><td rowspan="2">SCL, SDA input low voltage</td><td>TMG39921
TMG39925</td><td></td><td></td><td>0.3 V_{DD}</td><td rowspan="2">V</td></tr>
<tr><td>TMG39923
TMG39927</td><td></td><td></td><td>0.54</td></tr>
</table>

Note(s):

1. Values are shown at the V_{DD} pin and do not include current through the IR LED.
2. Current consumption during an LDR pulse is referenced as "$I_{DEVICE\ ANALOG}$" later in this document when calculating average power consumption.
3. Current consumption by the device during sleep is also used to approximate "$I_{DEVICE\ DRIVE}$" referenced later in this document when calculating average power consumption.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Figure 8:
Optical Characteristics (RGBC), V_{DD} = 3V, T_A = 25°C

<table>
<tr><th rowspan="3">Parameter</th><th rowspan="3">Test Conditions</th><th colspan="6">Ratio of Color to Clear Channel</th></tr>
<tr><th colspan="2">Red Channel</th><th colspan="2">Green Channel</th><th colspan="2">Blue Channel</th></tr>
<tr><th>Min</th><th>Max</th><th>Min</th><th>Max</th><th>Min</th><th>Max</th></tr>
<tr><td rowspan="4">Color ADC count value ratio: Color/Clear</td><td>White LED, 2700 K</td><td>45%</td><td>65%</td><td>19%</td><td>39%</td><td>15%</td><td>40%</td></tr>
<tr><td>$λ_D$ = 465 nm (1)</td><td>0%</td><td>15%</td><td>10%</td><td>42%</td><td>70%</td><td>90%</td></tr>
<tr><td>$λ_D$ = 525 nm (2)</td><td>4%</td><td>25%</td><td>60%</td><td>85%</td><td>10%</td><td>45%</td></tr>
<tr><td>$λ_D$ = 615 nm (3)</td><td>80%</td><td>110%</td><td>0%</td><td>14%</td><td>5%</td><td>24%</td></tr>
</table>

Note(s):

1. The 465nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength $λ_D$ = 465nm, spectral halfwidth Δλ½ = 22nm.
2. The 525nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength $λ_D$ = 525nm, spectral halfwidth Δλ½ = 35nm.
3. The 615nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength $λ_D$ = 615nm, spectral halfwidth Δλ½ = 15nm.

Figure 9:
RGBC Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16×, AEN, ATIME = 0XF6 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Dark ADC count value	Ee = 0, AGAIN: 64×, ATIME=0xDC (100ms)	0	1	3	counts [1]
ADC integration time step size	ATIME = 0xFF		2.78		ms
ADC number of integration steps		1		256	steps
ADC counts per step [2]		0		1024	counts
ADC count value	ATIME = 0xC0	0		65535	counts
Gain scaling, relative to 16× gain setting	AGAIN = 1×	0.058	0.062	0.067	X
	AGAIN = 4×	0.237	0.25	0.263	
	AGAIN = 64×	3.75	4	4.37	
Clear channel irradiance responsivity [3]	White LED, 2700 K	11.13	13.92	16.70	counts/ (μW/ cm^2)
ADC noise [4]	AGAIN :16x		0.005		% full Scale

Note(s):

1. The typical value based on 3-sigma distribution. An AGAIN setting of 16x correlates to a typically dark ADC count value less than or equal to 1.
2. Actual step sizes are 1024, however and addition count must be added when calculating the full-scale count value. For example, an ATIME setting of 0xFF results in a full-scale count value of 1025.
3. The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 2700K.
4. Number of data samples is 1000.

Figure 10:
Gesture Characteristics, V_{DD} = 3 V, T_A = 25°C, GEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
ADC conversion time step size (1)			1.39		ms
LED pulse count (2)	GPULSE	1		64	pulses
LED pulse width (3)	GPLEN = 0		4.0		µs
	GPLEN = 1		8.0		
	GPLEN = 2		16.0		
	GPLEN = 3		32.0		
LED drive current (4)	GLDRIVE = 0		100		mA
	GLDRIVE = 1		50		
	GLDRIVE = 2		25		
	GLDRIVE = 3		12.5		
	LEDBOOST = 0		100		%
	LEDBOOST = 1		150		
	LEDBOOST = 2		200		
	LEDBOOST = 3		300		
Photodiode relative deviation (5)		-12		12	%
Gesture noise (6)	GPULSE: 16 Pulses, GPLEN: 8 µs, GGAIN: 4x, GLDRIVE = 0, LEDBOOST = 0		0.78	1.25	% full Scale

Note(s):

1. Each N/S or E/W pair requires a conversion time of 696.6µs. For all four directions the conversion requires twice as much time.
2. This parameter ensured by design and characterization and is not 100% tested.
3. Value may be as much as 1.36µs longer than specified.
4. GLDRIVE current may vary from the typical value. LEDBOOST multiplies LDR current by the percentage selected.
5. This is the percent mismatch between the N, S, W, and E channels. No glass or aperture above the module.
6. Number of data samples is 128. This is the standard deviation expressed as percent of full scale signal.

Figure 11:
Gesture Optical Characteristics, V_{DD} = 3 V, T_A = 25°C, GGAIN = 8x, GEN = 1, Angle of Incident light = 0° (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
ADC integration time step size	GDIMS = 0		1.36		ms
ADC count value		0		255	counts
Gain scaling, relative to 1× gain setting	GGAIN : 2x		2		X
	GGAIN : 4x		4		
	GGAIN : 8x		8		

Figure 12:
Proximity Characteristics, V_{DD} = 3 V, T_A = 25°C, PEN = 1 (unless otherwise noted)

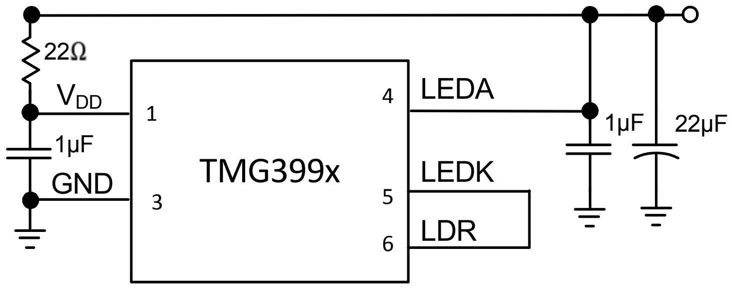
Parameter	Conditions	Min	Typ	Max	Units
ADC conversion time			696.6		µs
LED pulse count (1)	PPULSE	1		64	pulses
LED pulse width (2)	PPLEN = 0		4.0		µs
	PPLEN = 1		8.0		
	PPLEN = 2		16.0		
	PPLEN = 3		32.0		
LED drive current (3), (4)	LDRIVE = 0		100		mA
	LDRIVE = 1		50		
	LDRIVE = 2		25		
	LDRIVE = 3		12.5		
	LEDBOOST = 0		100		%
	LEDBOOST = 1		150		
	LEDBOOST = 2		200		
	LEDBOOST = 3		300		

Parameter	Conditions	Min	Typ	Max	Units
Proximity offset (no target response) [5]	PGAIN = 2 (4x) LDRIVE = 0 LEDBOOST = 1 PPLEN = 2 PPULSE= 2 (3 pulses) 100mm X 100mm 90% reflective Kodak Grey Card at 100mm distance		4		counts
Relative proximity response [6]	PGAIN = 2 (4x) LDRIVE = 1 LEDBOOST = 0 PPLEN = 1 PPULSE= 5 (6 pulses) d=23mm round target at 30mm distance	75	100	125	%
Proximity response [7]	PGAIN = 2 (4x) LDRIVE = 0 LEDBOOST = 1 PPLEN = 2 PPULSE= 2 (3 pulses) 100mm X 100mm 90% reflective Kodak Grey Card at 100mm distance	80	100	120	counts

Note(s):

1. This parameter ensured by design and characterization and is not 100% tested.
2. Value may be as much as 1.36µs longer than specified.
3. Value is factory-adjusted to meet the Proximity response specification. Considerable variation (relative to the typical value) is possible after adjustment. LEDBOOST increases current setting (as defined by LDRIVE or GLDRIVE). For example, if LDRIVE = 0 and LEDBOOST = 300%, LDR current is 300mA.
4. LEDBOOST multiplies LDR current by the percentage selected.
5. Proximity offset value varies with power supply characteristics and system noise.
6. Production tested value is the average of 5 readings.
7. Correlated result by characterization. Refer to Figure 25 and Figure 26 for typical operating settings.

Figure 13:
Proximity and Gesture Test Circuit



Proximity & Gesture Test Circuit: This circuit is used during evaluation of the device and during characterization data collection.

Figure 14:
Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Wait step size			2.78		ms

Figure 15:
Pattern Generation/Burst Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{(PBT\ min)}$	Minimum bit time	PBEN = 1		0.27		µs

Timing Characteristics

Figure 16:
AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

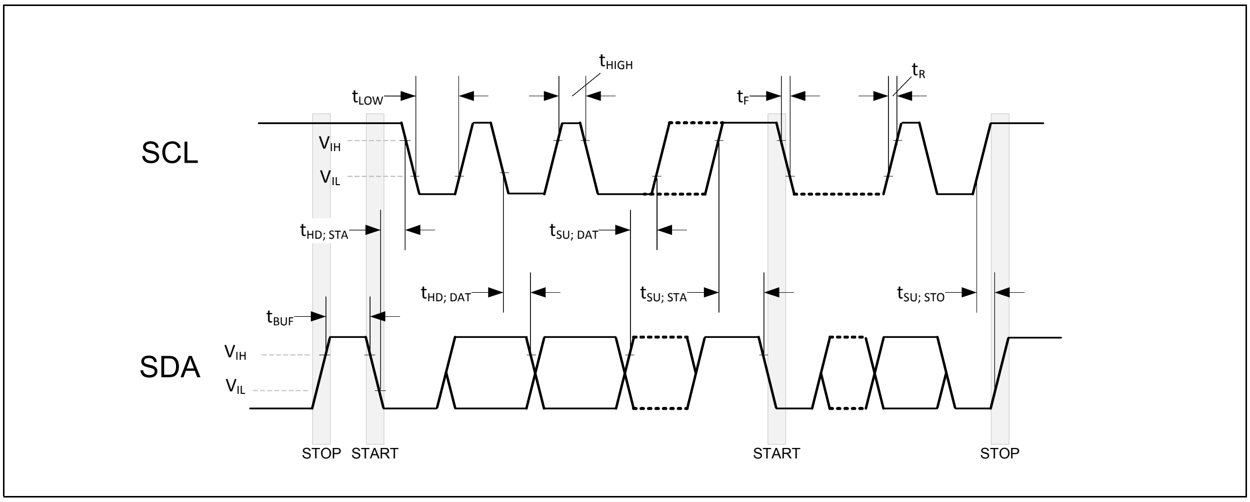
Parameter (1)	Description	Min	Max	Units
f_{SCL}	Clock frequency (I²C only)	0	400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3		µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		µs
$t_{SU;STA}$	Repeated start condition setup time	0.6		µs
$t_{SU;STO}$	Stop condition setup time	0.6		µs
$t_{HD;DAT}$	Data hold time	0		ns
$t_{SU;DAT}$	Data setup time	100		ns
t_{LOW}	SCL clock low period	1.3		µs
t_{HIGH}	SCL clock high period	0.6		µs
t_F	Clock/data fall time		300	ns
t_R	Clock/data rise time		300	ns
C_i	Input pin capacitance		10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagrams

Figure 17:
Timing Parameter Measurement Drawing



Typical Operating Characteristics

Figure 18:
Spectral Responsivity

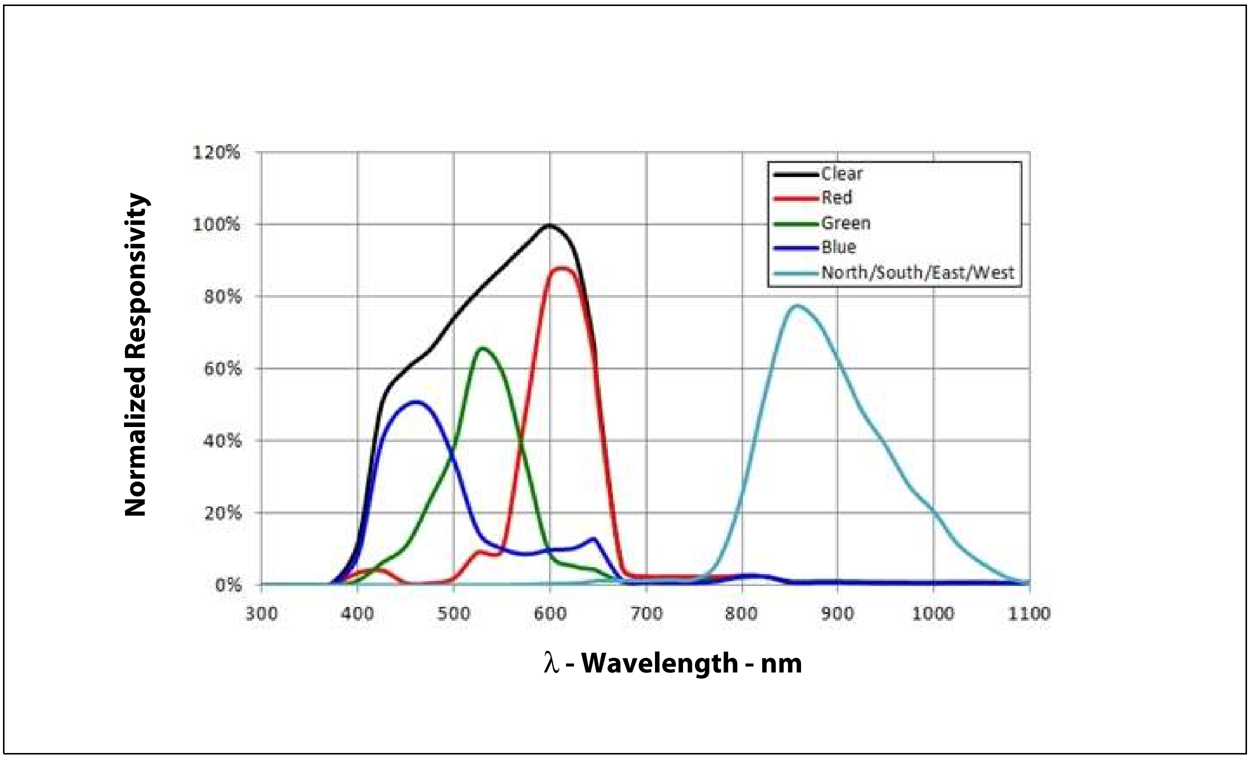


Figure 19:
RGBC Responsivity vs. Angular Displacement

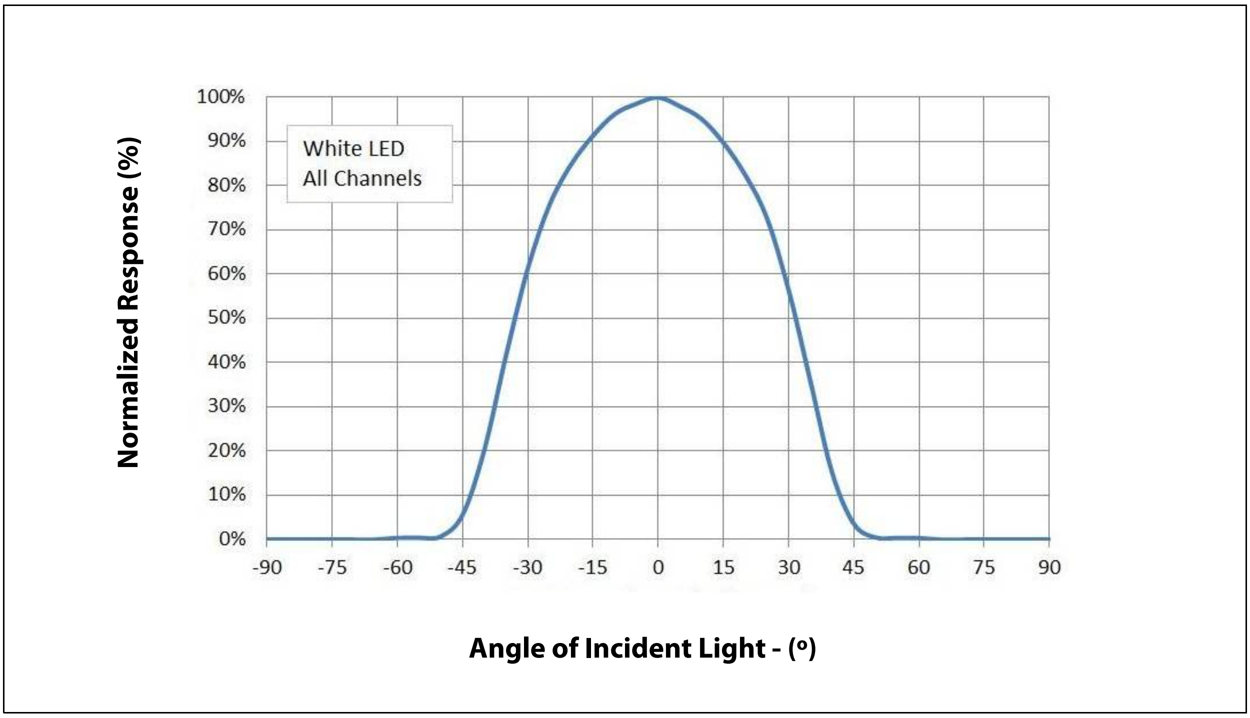


Figure 20:
Typical LDR Current vs. Voltage

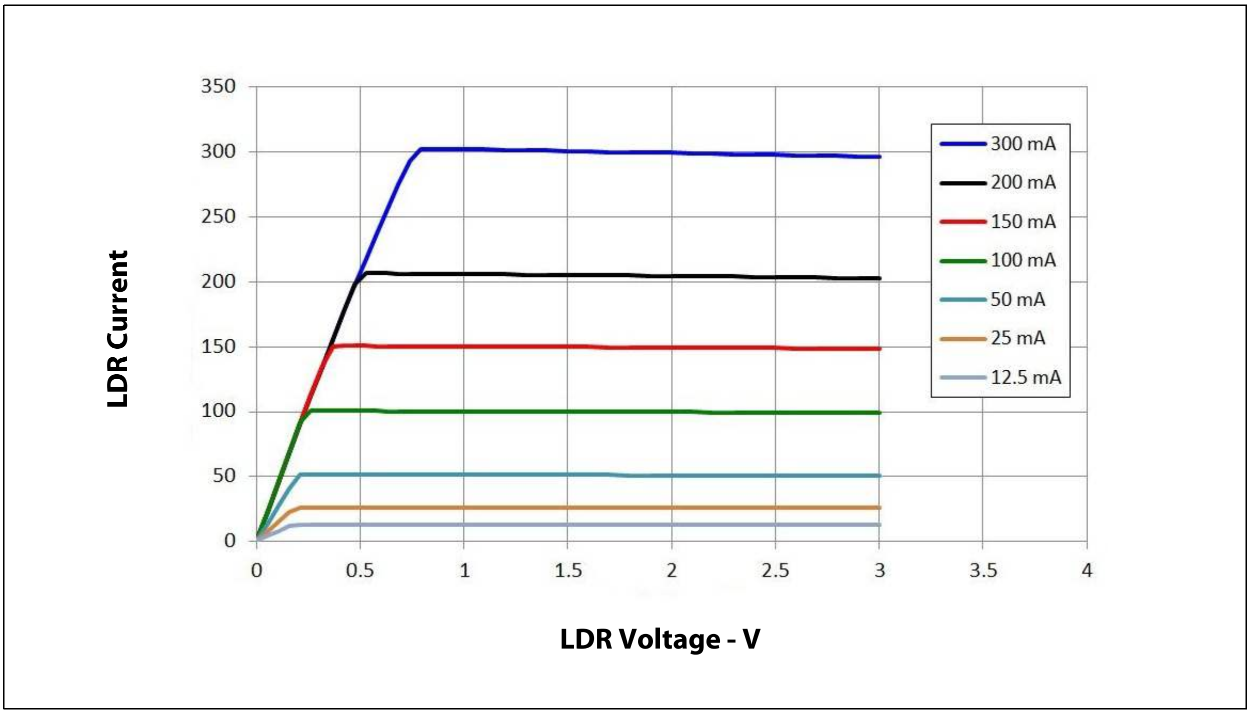


Figure 21:
Gesture Photodiodes Responsivity vs. Angular Displacement

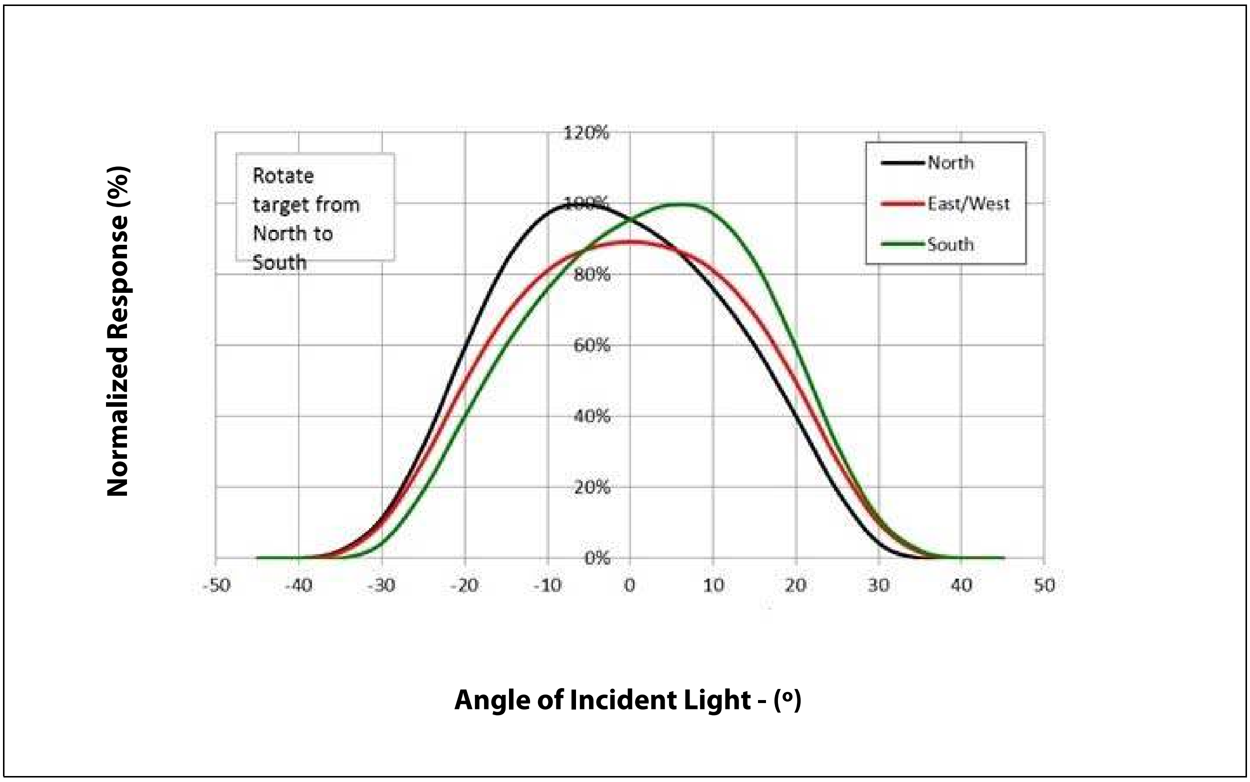


Figure 22:
Responsivity Temperature Coefficient

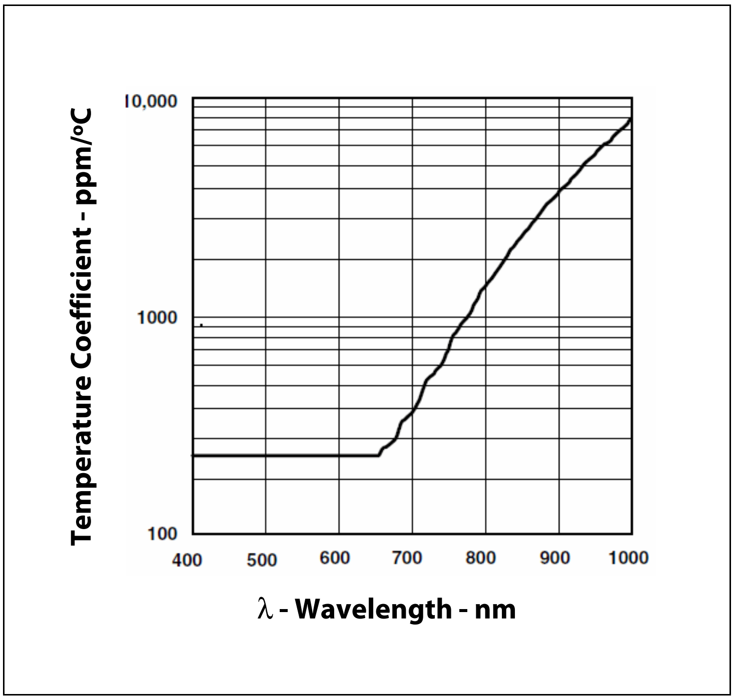
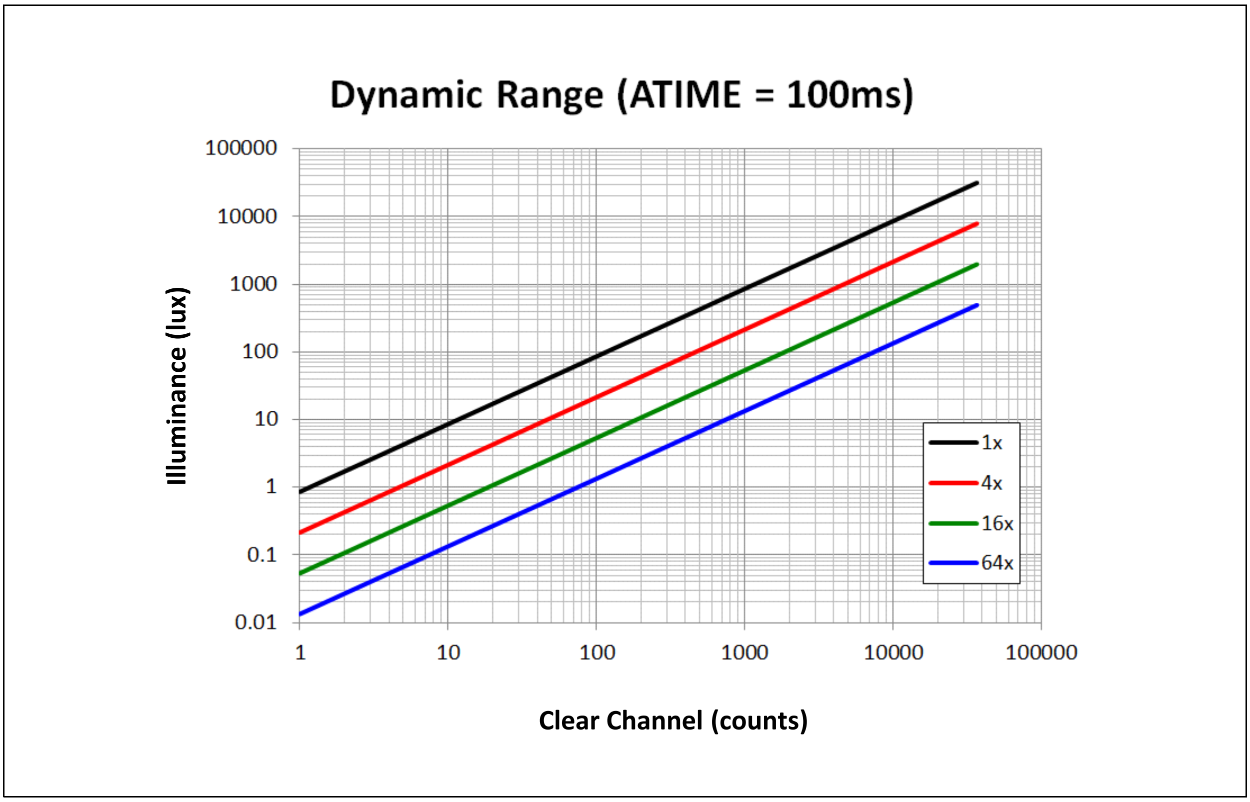
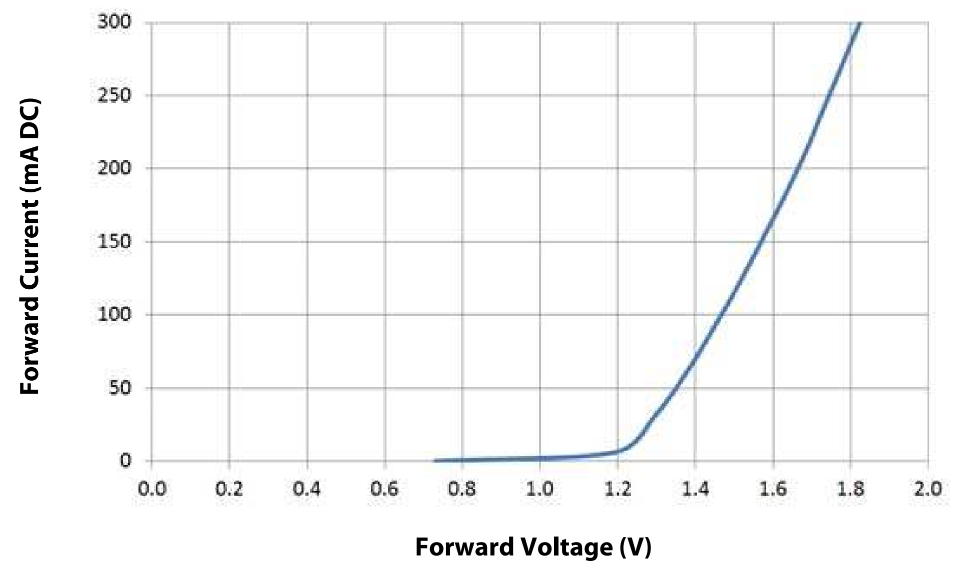


Figure 23:
Theoretical Illuminance (Lux) vs. Counts (Clear Channel)



Illuminance vs. Counts: This illustration depicts the theoretical relationship between illuminance and the Clear Channel result in Counts.

Figure 24:
940nm LED Forward Voltage vs. Current



Forward Voltage vs. Current: The voltage on the LDR pin ($V_{LEDA} – V_{LED FORWORD}$) must be sufficiently large to guarantee proper operation of the regulated current sink.

Figure 25:
Proximity Response vs. Target Distance (4µs, 8µs)

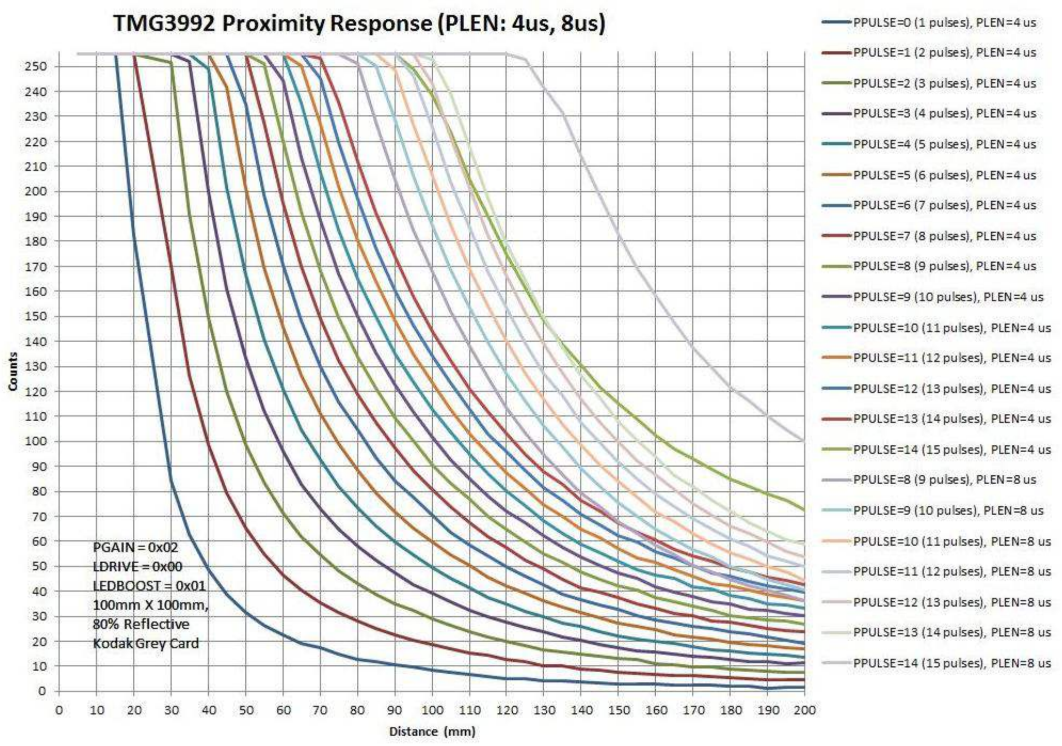
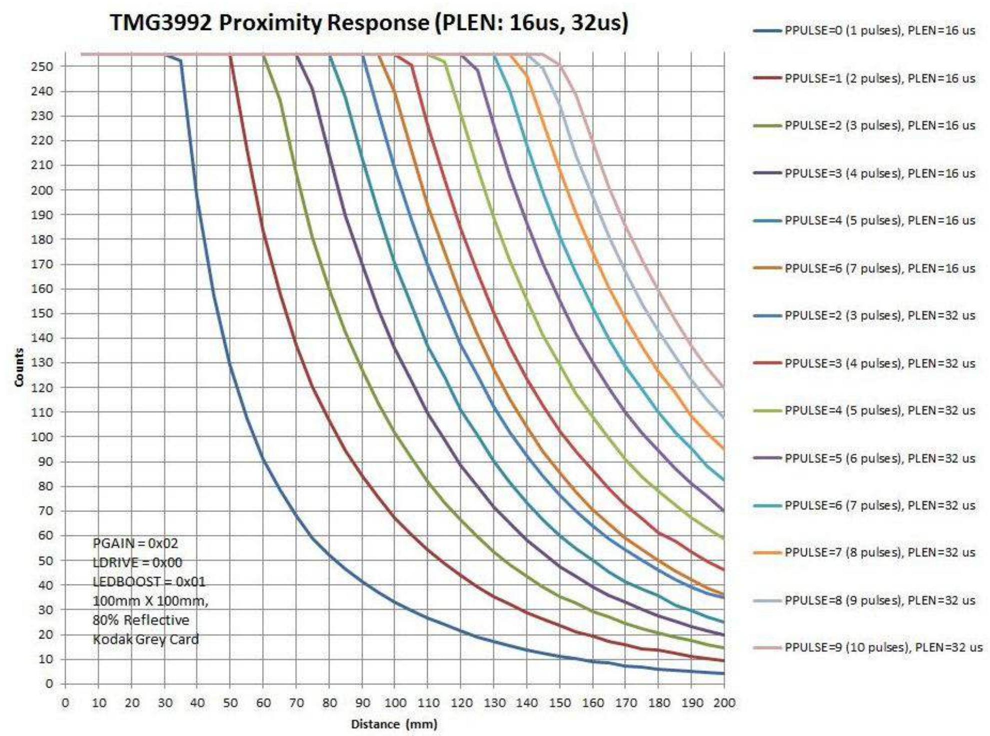


Figure 26:
Proximity Response vs. Target Distance (16µs, 32µs)



I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without "re"-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at: www.i2c-bus.org/references.

Detailed Description

Gesture detection, proximity detection, and RGBC color sense/ambient light sense functionality are controlled by a state machine, as depicted in Figure 32, which reconfigures on-chip analog resources when each functional engine is entered. Functional states/engines can be individually included or excluded from the progression of state machine flow. Each functional engine contains controls (E.g. Gain, ADC integration time, wait time, persistence, thresholds, etc.) that govern operation. Control of the Led Drive pin, LDR, is shared between Proximity, Gesture, and Pattern Burst functionality; consequently, while Pattern Burst functionality is activated, Gesture and Proximity should be deactivated.

Pattern Burst functionality uses a digital core that is independent of the analog sensor operation. The logic internal to the digital core is activated when PBEN=1, enabling Barcode Patterns (IRBeam) to be burst. The scanner receives the IR burst which emulates the pattern of reflected light during scan of a traditional paper barcode. In this operational mode the LDR pin is exclusively acquired. If proximity or gesture engines are also enabled, data generated will be invalid. The color/ALS engine does not use the IR LED, but cross talk from IR LED emissions during an optical pattern transmission may affect results.

Most of the functional engines are controlled by dedicated registers; however, controls for Gesture, and Pattern Burst are all accessed by the same address space: 0xA0 to 0xAF. Because each functional block serves a different purpose and utilizes common on-chip resources, only one may be activated at a time. For example, if Gesture and Pattern Burst engines are both activated simultaneously, the data stored in address 0xAx is available to both engines, but will only cause *the intended* engine to function properly.

Figure 27:
Simplified State Diagram

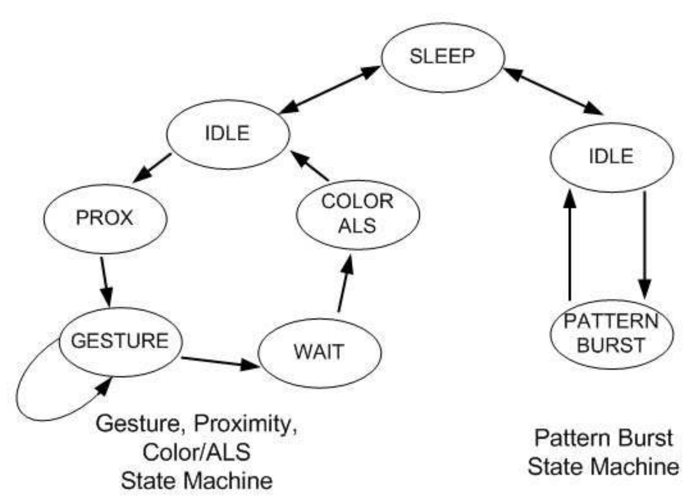
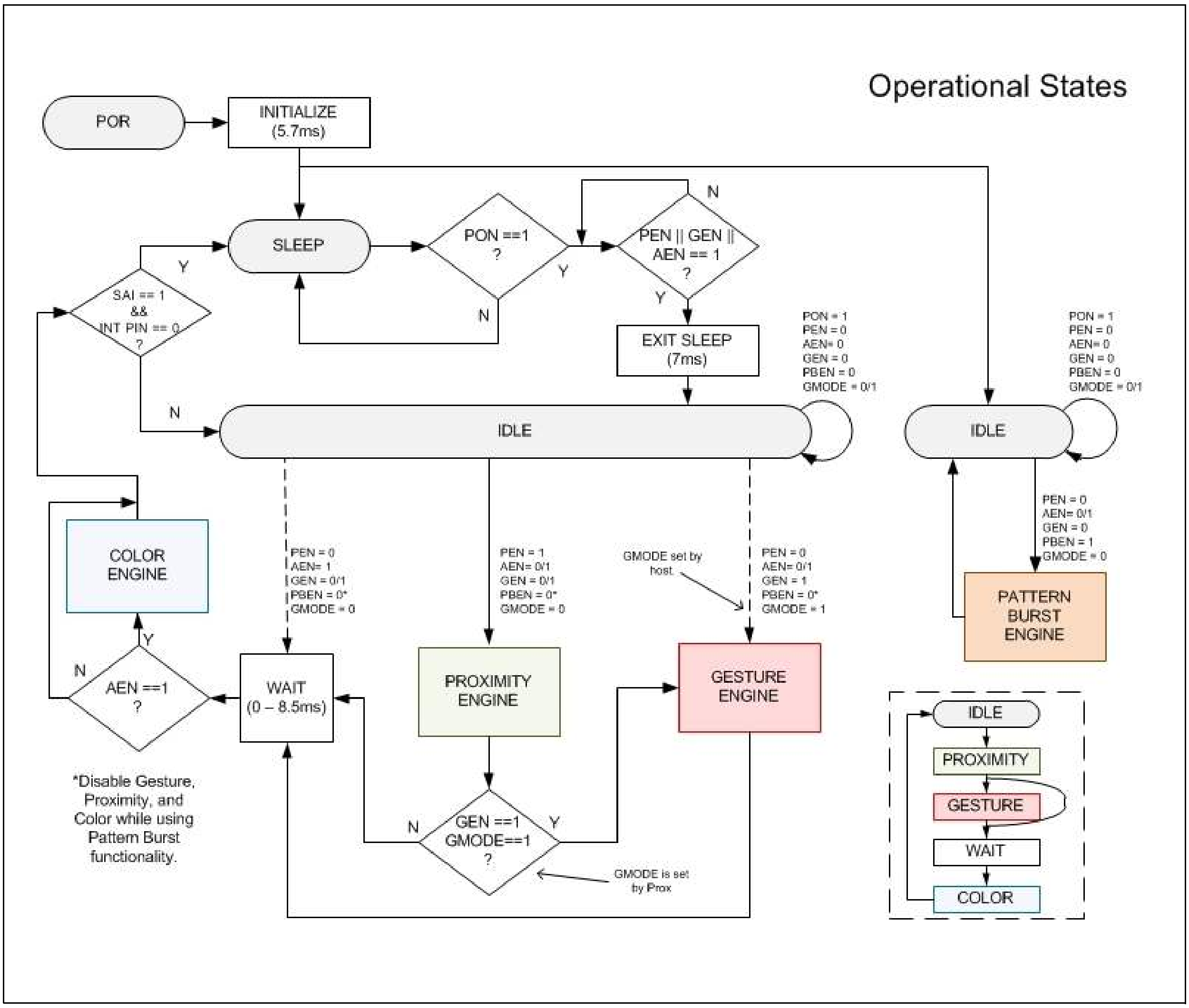


Figure 28:
Detailed State Diagram



As depicted in Figure 27 and Figure 28, the operational cycle of the device is divided into two parallel functional modes: Pattern Burst and Gesture/Proximity/Color.

Upon power-up, POR, the device initializes and immediately enters the low power SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If I^2C transaction occurs during this state, the oscillator and I^2C core wakeup temporarily to service the communication. Once the Power ON bit, PON, is enabled, the internal oscillator and attendant circuitry are active, but power consumption remains low until one of the functional engine blocks are entered. The first time the SLEEP state is exited and any of the analog engines are enabled (PEN, GEN, AEN =1) an EXIT SLEEP pause occurs; followed by an immediate entry into the selected engine. If multiple engines are enabled, then the operational flow progresses in the following order: idle, proximity, gesture (if GMODE = 1), wait, color/ALS, and sleep (if SAI = 1 and INT pin is asserted). The wait operational state functions to reduce the power consumption and data collection rate. If wait is enabled, WEN=1, the delay is adjustable from 2.78ms to 8.54s, as set by the value in the WTIME register and WLONG control bit.

Sleep After Interrupt Operation

After all the enabled engines/operational states have executed, causing a hardware interrupt, the state machine returns to either IDLE or SLEEP, as selected by the Sleep After Interrupt bit, SAI. SLEEP is entered when two conditions are met: SAI = 1, and the *INT* pin has been asserted. Entering SLEEP does not automatically change any of the register settings (E.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated by an I^2C clear of the INT pin or if SAI bit is cleared.

Proximity Operation

The Proximity detection feature provides object detection measurement by photodiode detection of reflected IR energy sourced by the integrated LED. The following registers and control bits govern proximity operation and the operational flow is depicted in Figure 30.

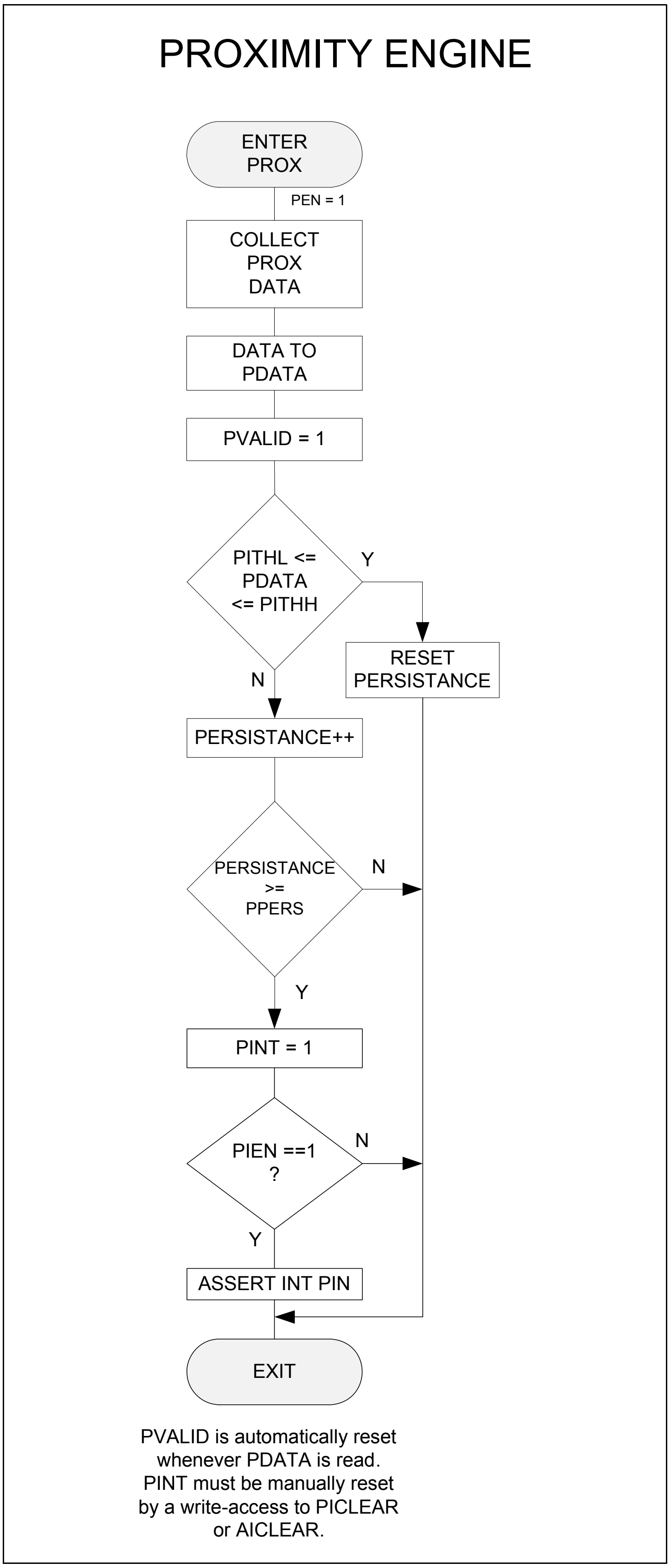
Figure 29:
Proximity Controls

Register/Bit	Address	Description
ENABLE<PON>	0x80<0>	Power ON
ENABLE<PEN>	0x80<2>	Proximity Enable
ENABLE<PIEN>	0x80<5>	Proximity Interrupt Enable
PITHL	0x89	Proximity low threshold
PITHH	0x8B	Proximity high threshold
PERS<PPERS>	0x8C<7:4>	Proximity Interrupt Persistence
PPULSE<PPLEN>	0x8E<7:6>	Proximity Pulse Length
PPULSE<PPULSE>	0x8E<5:0>	Proximity Pulse Count
CONTROL<PGAIN>	0x8F<3:2>	Proximity Gain Control
CONTROL<LDRIVE>	0x8F<7:6>	LED Drive Strength
CONFIG2<PSIEN>	0x90<7>	Proximity Saturation Interrupt Enable
CONFIG2<LEDBOOST>	0x90<5:4>	LED Boost
STATUS<PGSAT>	0x93<6>	Proximity Saturation
STATUS<PINT>	0x93<5>	Proximity Interrupt
STATUS<PVALID>	0x93<1>	Proximity Valid
PDATA	0x9C	Proximity Data
POFFSET_NE	0x9D	Proximity Offset North/East
POFFSET_SW	0x9E	Proximity Offset South/West
CONFIG3<PCMP>	0x9F<5>	Proximity Gain Compensation Enable
CONFIG3<PMSK_N>	0x9F<3>	Proximity Mask North Enable
CONFIG3<PMSK_S>	0x9F<2>	Proximity Mask South Enable
CONFIG3<PMSK_W>	0x9F<1>	Proximity Mask West Enable
CONFIG3<PMSK_E>	0x9F<0>	Proximity Mask East Enable
PICLEAR	0xE5	Proximity Interrupt Clear
AICLEAR	0xE7	All Non-Gesture Interrupt Clear

Note(s):

1. ENABLE<PBEN> must be low for proximity or gesture operation.

Figure 30:
Detailed Proximity Diagram



Proximity results are affected by three fundamental factors: IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from four [directional gesture] photodiodes and ends with the 8-bit proximity result in PDATA register. Signal from the photodiodes is combined, amplified, and offset adjusted to optimize performance. The same four photodiodes are used for gesture operation as well as proximity operation. Diodes are paired to form two signal paths: North/East and South/West. Regardless of pairing, any of the photodiodes can be masked to exclude its contribution to the proximity result. Masking one of the paired diodes effectively reduces the signal by half and causes the full-scale result to be reduced from 255 to 127. To correct this reduction in full-scale, the proximity gain compensation bit, PCMP, can be set, returning F.S. to 255. Gain is adjustable from 1x to 8x using the PGAIN control bits. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET_NE and POFSET_SW registers. The analog circuitry of the device applies the offset value as a *subtraction* to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Optically, the IR emission appears as a pulse train. The number of pulses is set by the PPULSE bits and the period of each pulse is adjustable using the PPLEN bits. The intensity of the IR emission is selectable using the LDRIVE control bits. These bits correspond to four factory calibrated current levels. If a higher intensity is required (E.g. longer detection distance or device placement beneath dark glass) then the LEDBOOST bits can be used to increase LDR current 150%, 200%, or 300% of LDRIVE setting.

LED duty cycle and subsequent power consumption of the integrated IR LED can be calculated using the following table shown in Figure 31, and equations. If proximity events are separated by a wait time, as set by AWAIT and WLONG, then the total LED OFF time must be increased by the wait time.

Figure 31:
Approximate Proximity Timing

PPLEN	t_{INIT} (µs)	$t_{LED\ ON}$ (µs)	t_{ACC} (µs)	t_{CNVT} (µs)
4 µs	40.8	5.4	28.6	796.6
8 µs	44.9	9.5	36.73	796.6
16 µs	53.0	17.7	53.1	796.6
32 µs	69.4	34.0	85.7	796.6

(EQ1) $t_{PROX\ RESULT} = t_{INIT} + t_{CNVT} + PPULSE \times t_{ACC}$

(EQ2) $t_{TOTAL\ LED\ ON} = PPULSE \times t_{LED\ ON}$

(EQ3) $t_{TOTAL\ LED\ OFF} = t_{PROX\ RESULT} - t_{TOTAL\ LED\ ON}$

An Interrupt can be generated with each new proximity result or whenever proximity results exceed or fall below levels set in the PITHL and/or PITHH threshold registers. To prevent premature/false interrupts an interrupt persistence filter is also included; interrupts will only be asserted if the consecutive number of out-of-threshold results is equal or greater than the value set by PPERS. Each "in-threshold" proximity result, PDATA, will reset the persistence count. If the analog circuitry becomes saturated, the PGSAT bit will be asserted to indicate PDATA results may not be accurate. The PINT and PGSAT bits are always available for I^2C polling, but PIEN bit must be set for PINT to assert a hardware interrupt on the INT pin. Similarly, saturation of the analog data converter can be detected by polling PGSAT bit; to enable this feature the PSIEN bit must be set. PVALID is cleared by reading PDATA. PGSAT and PINT are cleared PICLEAR or AICLEAR.

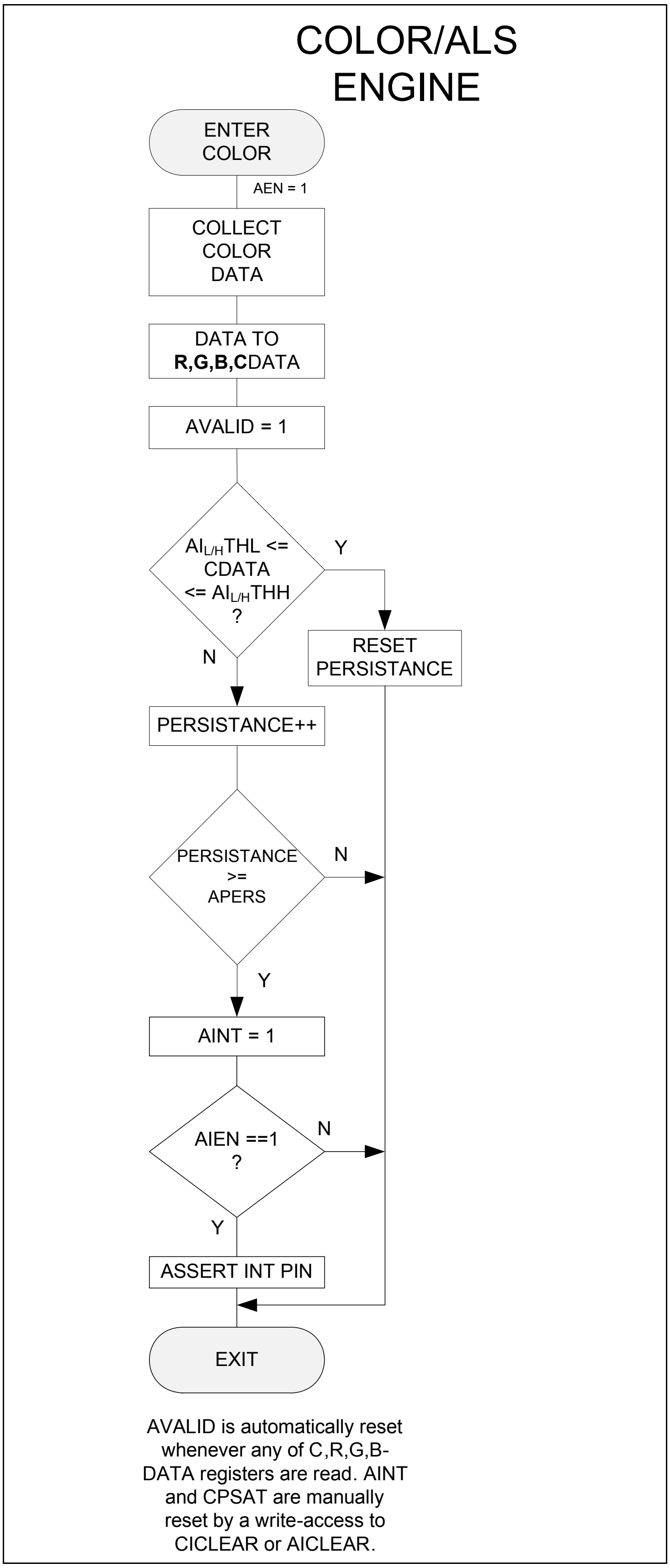
Color and Ambient Light Sense Operation

The Color and Ambient Light Sense detection functionality uses an array of color and IR filtered photodiodes to measure red, green, and blue content of light, as well as the *non-color filtered* clear channel. The following registers and control bits govern Color/ALS operation and the operational flow is depicted in Figure 33.

Figure 32:
Color / ALS Controls

Register/Bit	Address	Description
ENABLE<PON>	0x80<0>	Power ON
ENABLE<AEN>	0x80<2>	ALS Enable
ENABLE<AIEN>	0x80<4>	ALS Interrupt Enable
ENABLE<WEN>	0x80<3>	Wait Enable
ATIME	0x82	ALS ADC Integration Time
WTIME	0x83	Wait Time
AILTHL	0x84	ALS Low Threshold, Lower Byte
AIHTHL	0x85	ALS Low Threshold, Upper Byte
AILTHH	0x86	ALS High Threshold, Lower Byte
AIHTHH	0x87	ALS High Threshold, Upper Byte
PERS<APERS>	0x8C<3:0>	ALS Interrupt Persistence
CONFIG1<WLONG>	0x8D<1>	Wait Long Enable
CONTROL<AGAIN>	0x8F<1:0>	ALS Gain Control
CONFIG2<CPSIEN>	0x90<6>	Clear Diode Saturation Interrupt Enable
STATUS<CPSAT>	0x93<7>	Clear Diode Saturation
STATUS<AINT>	0x93<4>	ALS Interrupt
STATUS<AVALID>	0x93<0>	ALS Valid
CDATAL	0x94	Clear Data, Low Byte
CDATAH	0x95	Clear Data, High Byte
RDATAL	0x96	Red Data, Low Byte
RDATAH	0x97	Red Data, High Byte
GDATAL	0x98	Green Data, Low Byte
GDATAH	0x99	Green Data, High Byte
BDATAL	0x9A	Blue Data, Low Byte
BDATAH	0x9B	Blue Data, High Byte
CICLEAR	0xE6	Clear Channel Interrupt Clear
AICLEAR	0xE7	All Non-Gesture Interrupt Clear

Figure 33:
Color/ ALS State Diagram



The Color/ALS reception signal path begins with filtered RGBC detection at the photodiodes and ends with the 16-bit results in the RGBC data registers. Signal from the photodiode array accumulates for a period of time set by the value in ATIME before the results are placed into the RGBCDATA registers. Gain is adjustable from 1x to 64x, and is determined by the setting of CONTROL<AGAIN>. Performance characteristics such as accuracy, resolution, conversion speed, and power consumption can be adjusted to meet the needs of the application.

Before entering (re-entering) the Color/ALS engine, an adjustable, low power consumption, delay is entered. The wait time for this delay is selectable using the WEN, WTIME and WLONG control bits and ranges from 0 to 8.54s.

An interrupt can be generated whenever Clear Channel results exceed or fall below levels set in the AILTHL/AILTHH and/or AIHTHL/AIHTHH threshold registers. To prevent premature/false interrupts a persistence filter is also included; interrupts will only be asserted if the consecutive number of out-of-threshold results is equal or greater than the value set by APERS. Each "in-threshold" Clear channel result, CDATA, will reset the persistence count. If the analog circuitry becomes saturated, the ASAT bit will be asserted to indicate RGBCDATA results may not be accurate. The AINT and CPSAT bits are always available for I^2C polling, but AIEN bit must be set for AINT to assert a hardware interrupt on the INT pin. Similarly, saturation of the analog data converter can be detected by polling CPSAT bit; to enable this feature the CPSIEN bit must be set. AVALID is cleared by reading RGBCDATA. ASAT and AINT are cleared by using the Special Interrupt Clear I^2C transaction to access CICLEAR or AICLEAR.

RGBC results can be used to calculate ambient light levels (I.e. Lux) and color temperature (I.e. Kelvin).

Gesture Operation

The Gesture detection feature provides motion detection by utilizing *directionally sensitive* photodiodes to sense reflected IR energy by sourced by the integrated LED. The following registers and control bits govern gesture operation and the operational flow is depicted in Figure 35.

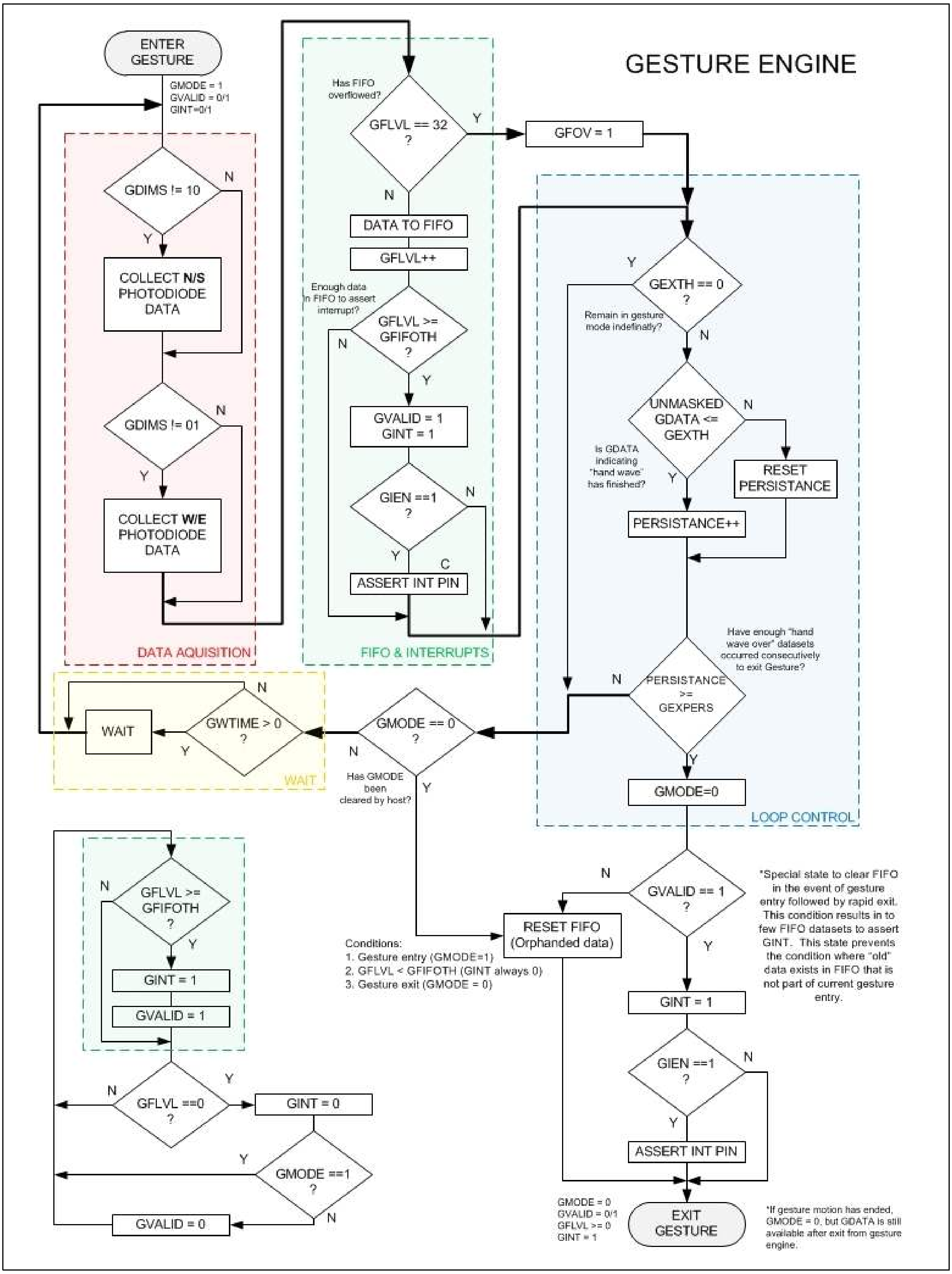
Figure 34:
Gesture Controls

Register/Bit	Address	Description
ENABLE<PON>	0x80<0>	Power ON
ENABLE<GEN>	0x80<6>	Gesture Enable
CONFIG_A0 (GPENTH)	0xA0	Gesture Proximity Entry Threshold
CONFIG_A1 (GEXTH)	0xA1	Gesture Exit Threshold
CONFIG_A2<GFIFOTH>	0xA2<7:6>	Gesture FIFO Threshold
CONFIG_A2<GEXMSK>	0xA2<5:2>	Gesture Exit Mask
CONFIG_A2<GEXPERS>	0xA2<1:0>	Gesture Exit Persistence
CONFIG_A3<GENAL>	0xA3<7>	Gesture Enter Always
CONFIG_A3<GGAIN>	0xA3<6:5>	Gesture Gain Control
CONFIG_A3<GLDRIVE>	0xA3<4:3>	Gesture LED Drive Strength
CONFIG_A3<GWTIME>	0xA3<2:0>	Gesture Wait Time
STATUS<PGSAT>	0x93<6>	Gesture Saturation
CONFIG2<LEDBOOST>	0x90<5:4>	LED Boost
CONFIG_A4 (GOFFSET_N)	0xA4	Gesture Offset, North
CONFIG_A5 (GOFFSET_S)	0xA5	Gesture Offset, South
CONFIG_A7 (GOFFSET_W)	0xA7	Gesture Offset, West
CONFIG_A9 (GOFFSET_E)	0xA9	Gesture Offset, East
CONFIG_A6 <GPULSE>	0xA6<5:0>	Gesture Pulse Count
CONFIG_A6 <GPLEN>	0xA6<7:6>	Gesture Pulse Length
CONFIG_AA <GDIMS>	0xAA<1:0>	Gesture Dimension Select
CONFIG_AB <GIEN>	0xAB<1>	Gesture Interrupt Enable
CONFIG_AB <GMODE>	0xAB<0>	Gesture Mode
CONFIG_AE (GFLVL)	0xAE	Gesture FIFO Level
CONFIG_AF<GFOV>	0xAF<1>	Gesture FIFO Overflow
CONFIG_AF <GVALID>	0xAF<0>	Gesture Valid
GFIFO_N	0xFC	Gesture FIFO Data, North
GFIFO_S	0xFD	Gesture FIFO Data, South
GFIFO_W	0xFE	Gesture FIFO Data, West
GFIFO_E	0xFF	Gesture FIFO Data, East

Note(s):

1. ENABLE<PBEN> must be low for proximity or gesture operation.

Figure 35:
Detailed Gesture Diagram



Gesture results are affected by three fundamental factors: IR LED emission, IR reception, and environmental factors, including motion.

During operation, the Gesture engine is entered when Gesture Enable, GEN, and Gesture Mode bit, GMODE, are both set. GMODE can be set/reset manually, via I^2C, or becomes set when proximity results, in PDATA, are greater or equal to the gesture proximity entry threshold, GPENTH. If the Gesture Enter Always, GENAL, bit is set, then any PDATA result will cause an entry into the gesture engine. Exit of the gesture engine will not occur until GMODE is reset to zero. During normal operation, GMODE is reset when all 4-bytes of a gesture dataset fall below the exit threshold, GEXTH, for GEXPERS times. This *exit condition* is also influenced by the gesture exit mask, GEXMSK, which includes all non-masked datum (i.e. singular 1-byte N, S, W, E points). To prevent premature exit, a persistence filter is also included; exit will only occur if a consecutive number of below-threshold results is greater or equal to the persistence value, GEXPERS. Each dataset result that is above-threshold will reset the persistence count. False or incomplete gestures (engine entry and exit without GVALID transitioning high) will not generate a gesture interrupt, GINT, and FIFO data will automatically be purged.

During North-South-West-East Gesture operation, the IR reception signal path begins with IR detection at the photodiodes and ends with the four, 8-bit gesture results loading into the FIFO. Each 8-bit result corresponds to the amount of IR energy measured by each photodiode sensor. Signal from the four photodiodes is amplified, and offset adjusted to optimize performance.

Photodiodes are paired to form two signal paths: North/South and West/East. Photodiode pairs can be masked to exclude its results from the gesture FIFO data. For example, if only North-South motions detection is required then the gesture dimension control bits, GDIMS, may be set to 0x01. FIFO data will be zero for East/West results and accumulation/ADC integration time will be approximately halved. Gain is adjustable from 1x to 8x using the GGAIN control bits. Offset correction is accomplished by individual adjustment to GOFFSET_N, GOFFSET_S, GOFFSET_W, GOFFSET_E registers which improves cross-talk performance. The analog circuitry of the device applies offset values as a *subtraction* to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

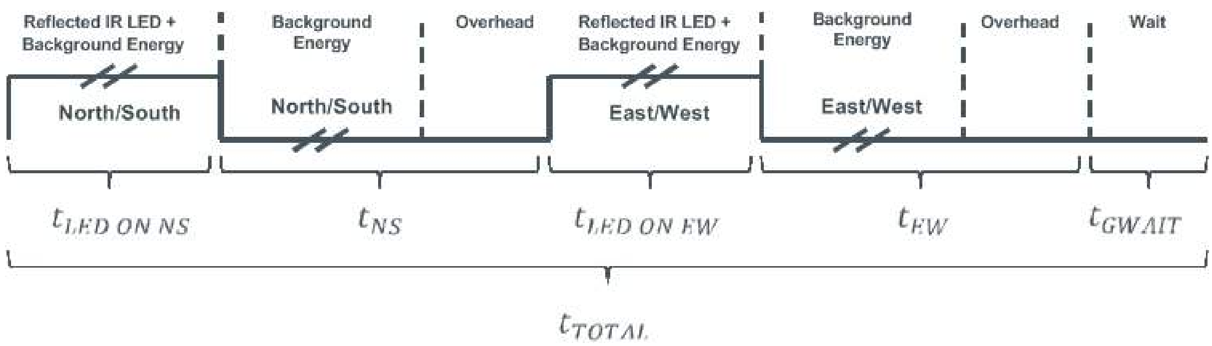
Optically, the IR emission appears as a pulse train. The number of pulses is set by the GPULSE bits and the period of each pulse is adjustable using the GPLEN bits. Pulse train repetition (I.e. the circular flow of operation inside the gesture state machine) can be delayed by setting a non-zero value in the gesture wait time bits, GWTIME. The inclusion of a wait state reduces both the power consumption and the data rate.

The intensity of the IR emission is selectable using the GLDRIVE control bits. These bits correspond to four factory calibrated current levels. If a higher intensity is required (E.g. longer detection distance or device placement beneath dark glass) then the LEDBOOST bits can be used to increase LDR current 150%, 200%, or 300% of GLDRIVE setting.

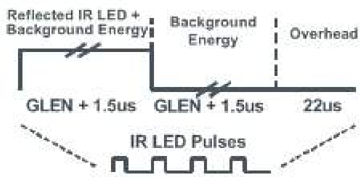
LED duty cycle and subsequent power consumption of the integrated IR LED can be calculated using the following table shown in Figure 36, and equations.

Figure 36:
Simplified Power Calculation

Nomenclature



Foreground/Background Subtraction



NS / EW With Wait State Timing

Equations

$t_{LED\ ON\ NS}$ = $t_{LED\ ON\ EW}$ = GPULSE x (GPLEN + 1.5)

t_{NS} = t_{EW} = 870 + GPULSE X (22 + 2 X (GPLEN + 1.5))

t_{GWAIT} = 2.8ms X GWTIME

t_{TOTAL} = t_{NS} + t_{EW} + t_{GWAIT}

$$t_{LED} \text{ x } dc_{\text{LED On Duty Cycle}} = LDR \times \frac{t_{LED\_ON\_NS} + t_{LED\_ON\_EW}}{t_{TOTAL}}$$

$$t_{Device} \text{ x } dc_{\text{ Device Duty Cycle}} = 0.790 \times \frac{t_{NS} + t_{EW}}{t_{TOTAL}}$$

$$t_{Wait} \text{ x } dc_{\text{ Wait Duty Cycle}} = 0.038 \times \frac{t_{GWAIT}}{t_{TOTAL}}$$

Note: The “870” value is conversion time + settling time.

Example

Conditions

32µs, 16pulses, 1 wait, 300mA

$i_{DEVICE\ ANALOG}$ = 0.79mA

$I_{DEVICE\ DRIVE}$ = 0.38mA

t_{ON} = 16 x 33.5 = 536 µs

t_{NS} = 870 + 16 x (22 +(2 x 33.5))

= 2294 µs

t_{NSEW} = 2294 + 2294 = 4586 µs

t_{GWAIT} = 2800 µs

t_{TOTAL}= 2800+4586 = 8400 µs

Duty Cycle LED ON = 536 + 536/7386 = 14.5%

*$i_{Power\ LED\ ON}$ = 14.5% * 300 = 43.5mA*

Duty Cycle Device = 4586/7386 = 62%

*$i_{Power\ Device}$ = 62% * 0.79 = 0.490mA*

Duty Cycle Wait = 2800/7386 = 38%

*$i_{POWER\ WAIT}$ =38% * 0.038 = 0.014mA*

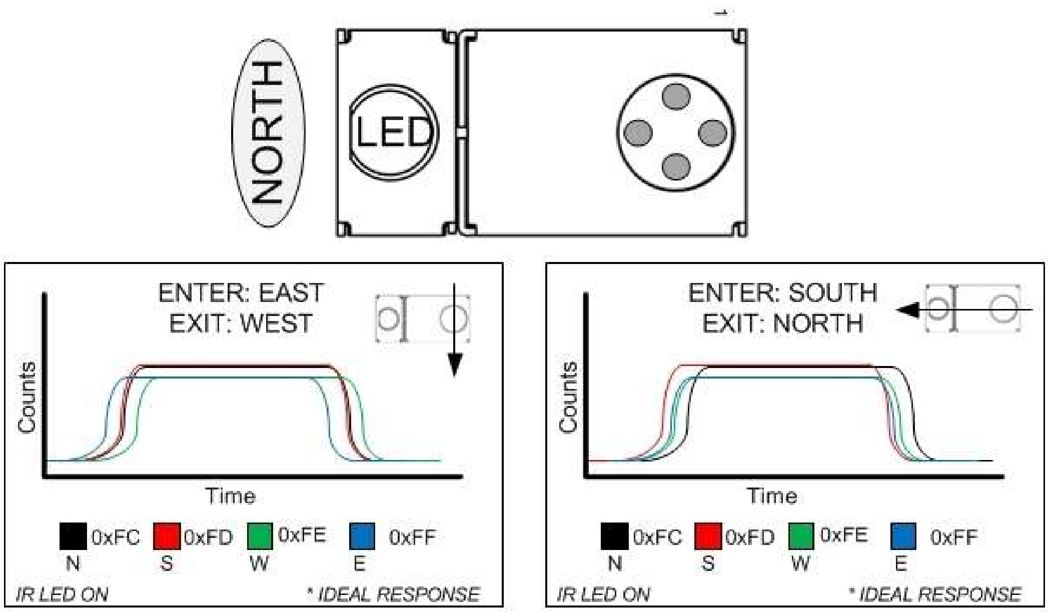
$i_{POWER\ TOTAL}$ = 43.5 + 0.49 + 0.014 = 44mA

An interrupt is generated based on the number of gesture "datasets" results placed in the FIFO. A dataset is defined as 4-byte directional data corresponding to N-S-W-E (GDIMS = 0). The FIFO can buffer up to 32 datasets before it overflows. If the FIFO overflows (host did not read quickly enough) then the most recent data will be lost. If the FIFO level, GFLVL, becomes greater or equal to the threshold value set by GFIFOTH, the GVALID bit is set indicating valid data is available, gesture interrupt bit, GINT, is asserted, and if GIEN bit is set a hardware interrupt on the INT pin will also assert. Before exit of gesture engine, indicated by GVALID transitioning from high to low, one final interrupt will always occur. This interrupt signals that data still remains in the FIFO. Gesture Interrupts and Flags: GINT, GVALID, and GFLVL are cleared by emptying FIFO (i.e. all data has been read).

The correlation of motion to FIFO data (i.e. speed and direction characteristics) is not obvious at first glance. As depicted in Figure 37, the four directional photodiode sensors are placed in an orthogonal pattern beneath an optical transparent aperture.Diodes are designated as: N', S', W', and E'. The 8-bit results corresponding to each diode are available for sequential read at the following FIFO register address locations: 0xFC, 0xFD, 0xFE, and 0xFF. After address 0xFF is read, additional reads automatically increase the FIFO pointer and effectively reset the register address to back to 0xFC. This allows for continuous transfer of FIFO data without re-issuing chip and memory addresses.

Ideally, gesture detection works by capturing and comparing the amplitude and phase difference between directional sensor results. The directional sensors are arranged such that the diode opposite to the directional motion receives a larger portion of the reflected IR signal upon entry, then a smaller portion upon exit. In the example illustration, a North-to-South motion is the result when a target enters the device field-of-view from N' (North-Prime), progresses past W' and E', then exits over S' (South-Prime).

Figure 37:
Directional Orientation



Pattern Burst Operation: IRBeam Mode

The optical pattern generation/transmission feature is primarily intended for barcode transmission over IR, however, it may be used for general purpose pattern generation in applications that require as much as1024 bits of RAM pattern depth. The following registers and control bits govern IRBeam operation and the operational flow is depicted in Figure 39 and Figure 40.

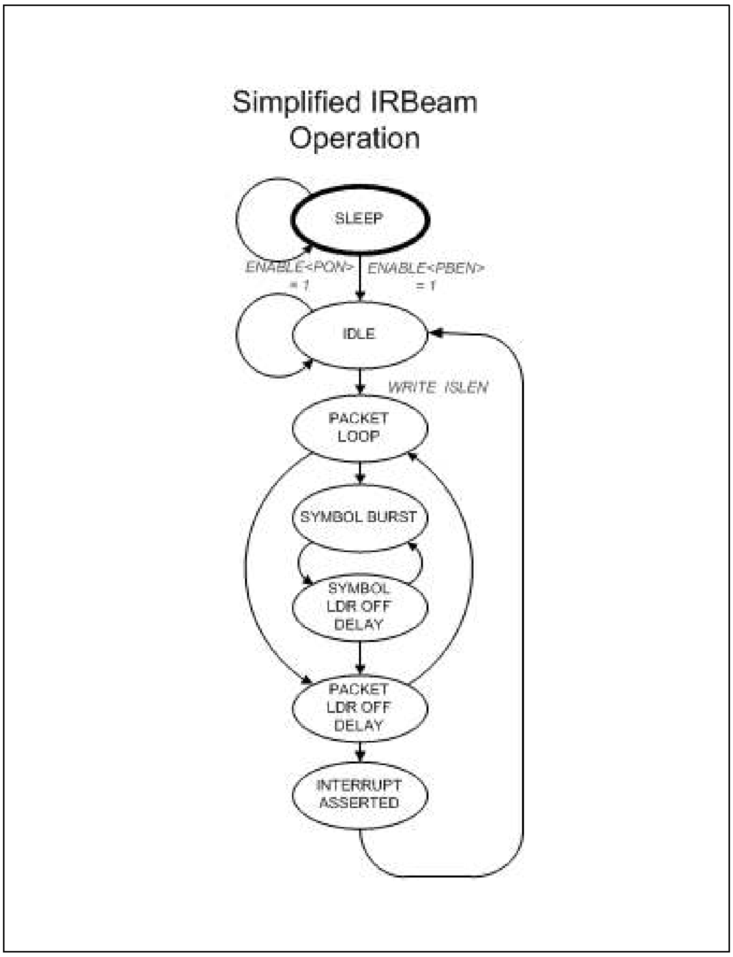
Figure 38:
IRBeam Controls

Register/Bit	Address	Description
ENABLE<PON>	0x80<0>	Power ON
ENABLE<PBEN>	0x80<7>	Pattern Burst Enable
CONFIG_A0 <PBIEN>	0xA0<5>	Pattern Burst Interrupt Enable
CONFIG_A0 <SLEW>	0xA0<4>	Slew Rate Control
CONFIG_A0 <ISQZL>	0xA0<3>	IRBeam Symbol Quiet Zone LDR State
CONFIG_A0 <ISQZT>	0xA0<2:0>	IRBeam Symbol Quiet Zone Time
CONFIG_A2 (ISNL)	0xA2	IRBeam Number of Symbol Loops
CONFIG_A3 (ISOFF)	0xA3	IRBeam LED OFF Time Between Symbols
CONFIG_A4 (IPNL)	0xA4	IRBeam Number of Packet Loops
CONFIG_A5 (IPOFF)	0xA5	IRBeam LED OFF Time Between Packets
CONFIG_A6 <IBT>	0xA6<5:0>	Pattern Bit Time
CONFIG_A7 (ISLEN)	0xA7	IRBeam Symbol bit Pattern Length
CONFIG_A8<PBINT2>	0xA8<1>	Pattern Burst Interrupt Two
STATUS<PBINT>	0x93<3>	Pattern Burst Interrupt. (mirrors CONFIG_A8<PBINT2>)
CONFIG_A8 <PBUSY>	0xA8<0>	Pattern Burst Busy
CONTROL<LDRIVE>	0x8F<7:6>	LED Drive Strength
CONFIG2<LEDBOOST>	0x90<5:4>	LED Boost
PBCLEAR	0xE3	Pattern Burst Interrupt Clear
AICLEAR	0xE7	All Non-Gesture Interrupt Clear

Note(s):

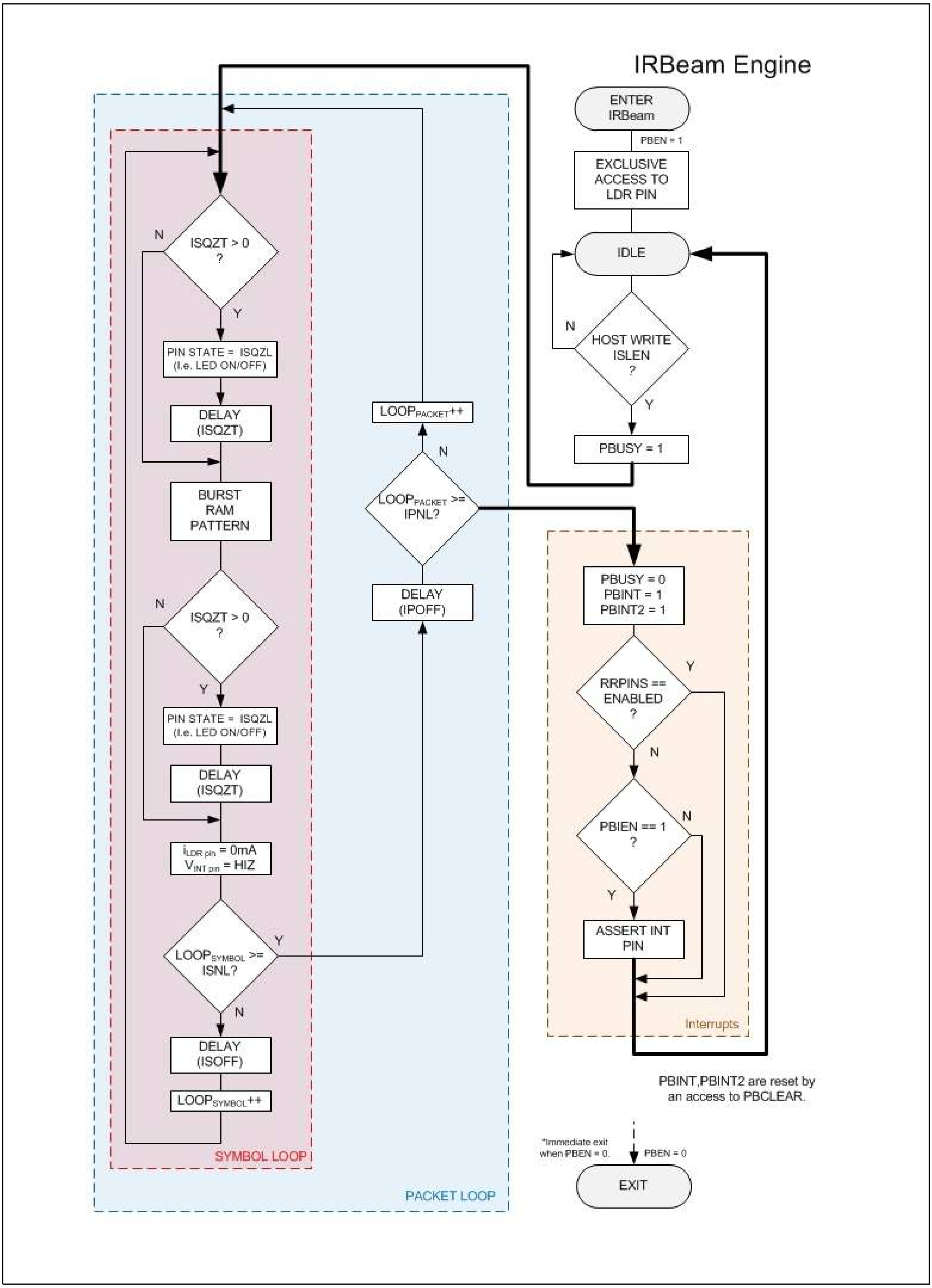
1. While ENABLE<PBEN> = 1, the Pattern Burst engine has exclusive access to the LDR pin, Proximity and Gesture operating modes must be disabled (ENABLE<PEN> = 0, ENABLE<GEN> = 0).

Figure 39:
Simplified IRBeam Operation



As depicted in Figure 39, the IRBeam operational states can be described by seven functional events: Idle, Burst Symbol/Symbol Loop, Symbol LDR OFF Delay, Packet Loop, Packet Loop LDR OFF Delay, and Interrupt. Data stored in RAM and IRBeam registers control the state machine operation as each event is executed. Figure 40 describes the IRBeam state machine in detail.

Figure 40:
Detailed IRBeam Diagram



Upon enabling the Pattern Burst engine, PON=PBEN=1, the IDLE state is entered. In this state, control of the LDR pin is removed from the Proximity/Gesture modules and is exclusively driven by the pattern stored in RAM. IR pattern emission begins when any value is written to CONFIG_A7, Symbol Length/Start Transmission register, ISLEN, or whenever PBEN bit transitions from 0 to 1. Prior to writing ISLEN or enabling PBEN bit control registers and pattern RAM must be valid (previously programmed).

Pattern data stored in the128-byte RAM defines the activation state of the LDR pin (LED ON/OFF) during an IRBeam Symbol burst event. After ISLEN is written each bit of RAM sets the state of the LDR pin with a pulse width set by bit-time control bits, IBT, located in CONFIG_A6. Bits are burst out of the LDR pin MSB first starting at address 0x00. Each integer value placed in ISLEN register corresponds to 4-bit (nibble) blocks of pattern. For example, if ISLEN = 0, the first four bits of address 0x00 (bits: 7, 6, 5, and 4) modulate the LDR current.

Immediately after writing the ISLEN, the PBUSY bit is set and a Burst Symbol event commences. During this event the LDR pin modulates LED current, bursting the bit-wise (Barcode symbol) pattern stored in RAM starting at location 0x00. Refer to Figure 41, Figure 42, and Figure 43 for a graphical representation of how the a complete pattern burst is built using the RAM and control register settings. The control register for bit-time, IBT, provides a wide range of timing options to satisfy requirements set by commonly used barcode standards. Equations for Bit Time, IBT, and other timing parameters are located in the Register Description section.

By setting a non-zero value in the Symbol Number of Loops Register, ISNL, more than one Transmit Symbol event can be executed for each write to ISLEN. Between Symbols the LDR pin is turned OFF for a period of time defined by the Symbol LDR OFF Delay register, ISOFF. This sequence of symbol transmission followed by an LDR OFF Delay, ISOFF, represents a Symbol Loop event, as depicted in Figure 42. A maximum of 256 symbol loops can be executed. After the final loop has completed the Packet Loop event commences.

A Packet Loop event, as depicted in Figure 43, is much like a Symbol Loop event except that inside a packet loop a number of entire Symbol Loop events are repeated. By setting a non-zero value in the Packet Number of Loops Register, IPNL, more than one packet loop event can be executed for each write to ISLEN. Between packets the LDR pin is turned OFF for a period of time as defined by the Packet LDR OFF Delay register, IPOFF. A minimum setting of 0 in IPNL prevents *any additional* packet loops from running; however, a packet LDR OFF delay always runs at least one time. A maximum of 256 Packet loops can be executed. After the final loop has completed, interrupts are asserted, PBUSY is cleared, and control is passed back to the IDLE state.

To reduce I^2C traffic, the CONFIG_A8<PBINT2> interrupt bit is mirrored in the STATUS register, which primary contains device interrupt bits. If the interrupt enable bit, CONFIG_A0<PBIEN>, is set, then a hardware interrupt on the INT pin will assert. IRBeam interrupts are cleared PBCLEAR or AICLEAR.

Figure 41:
IRBeam Symbol

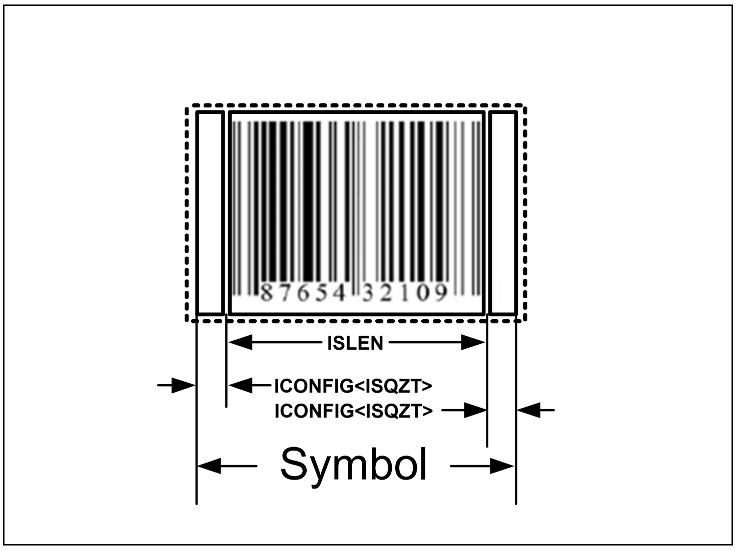


Figure 42:
IRBeam Symbol Loop

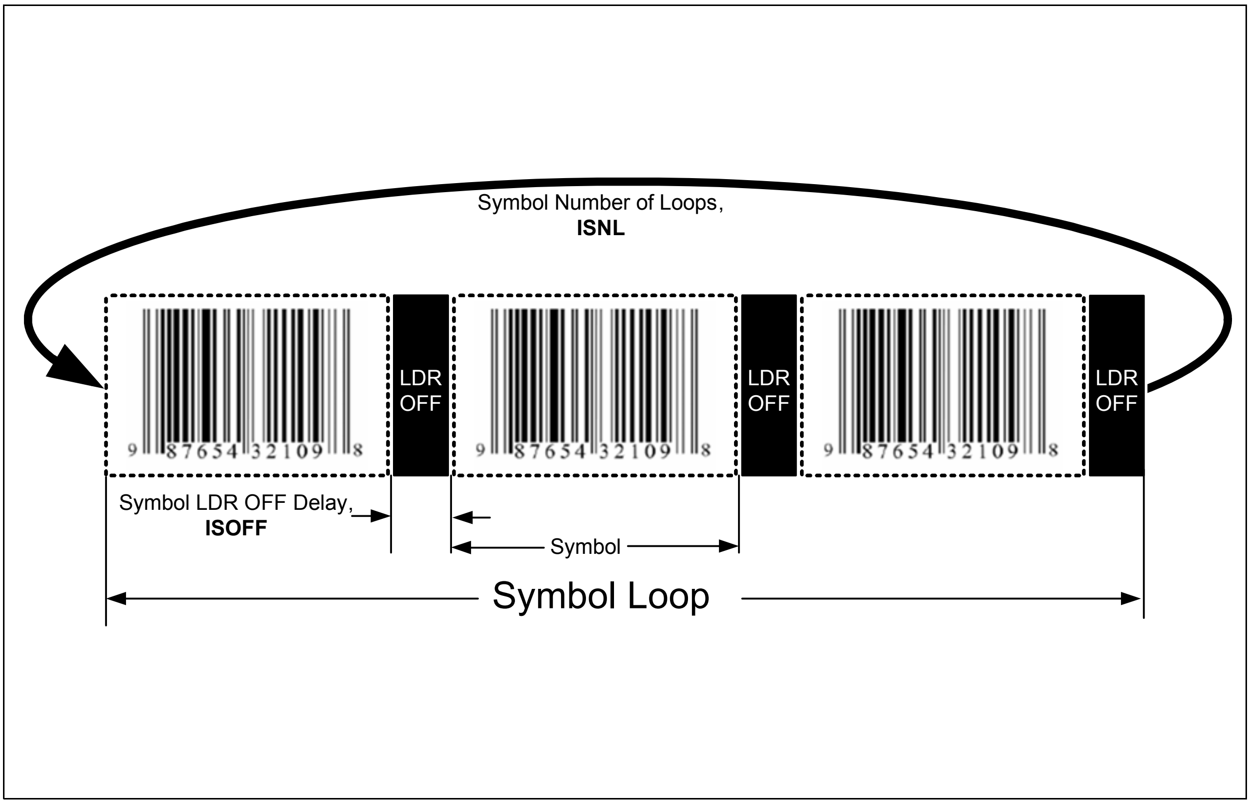
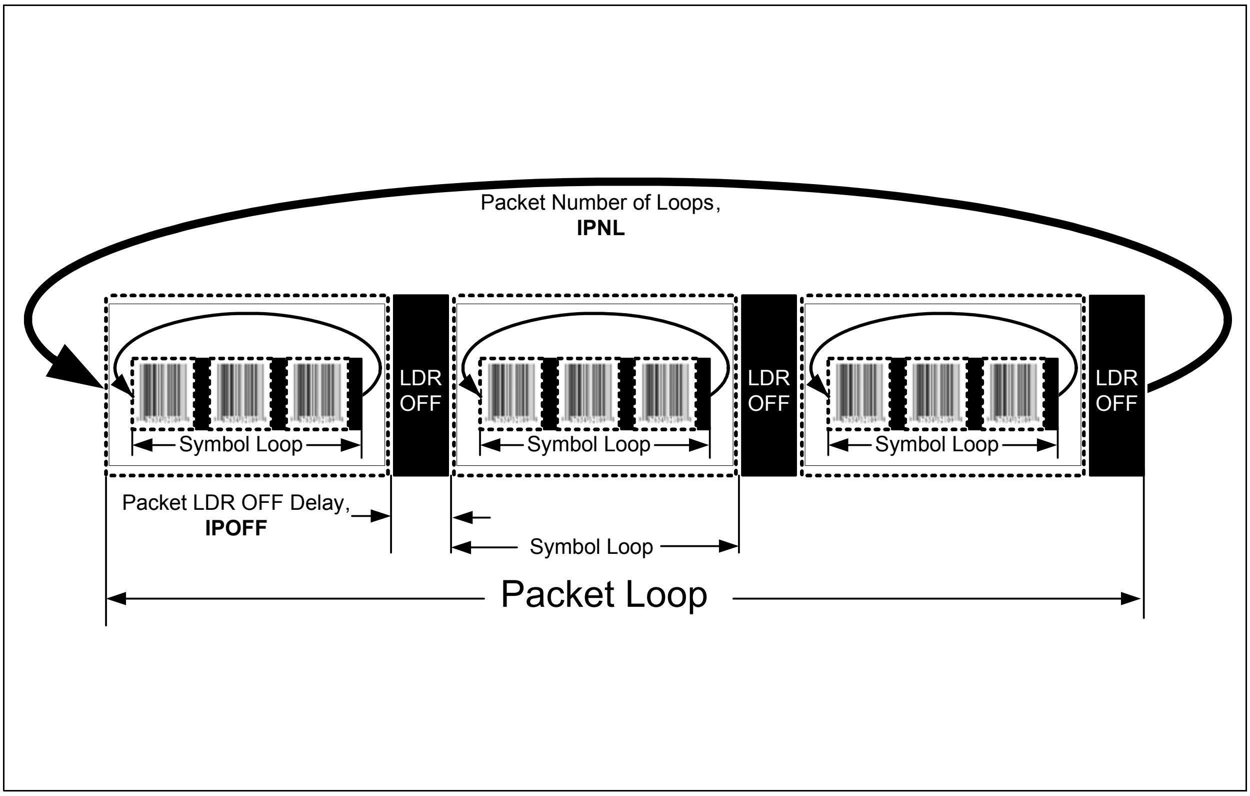


Figure 43:
IRBeam Packet Loop



Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 44.

Figure 44:
Control Register Map

Address	Register Name	R/W	Register Function	Reset Value
0x00 – 0x7F	RAM	R/W	Volatile storage for pattern data	0x00
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	ADC integration time	0xFF
0x83	WTIME	R/W	Wait time (non-gesture)	0xFF
0x84	AILTHL	R/W	ALS interrupt low threshold low byte	0xXX
0x85	AILTHH	R/W	ALS interrupt low threshold high byte	0xXX
0x86	AIHTHL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTHH	R/W	ALS interrupt high threshold high byte	0x00
0x89	PITHL	R/W	Proximity interrupt low threshold	0x00
0x8B	PITHH	R/W	Proximity interrupt high threshold	0x00
0x8C	PERS	R/W	Interrupt persistence filters (non-gesture)	0x00
0x8D	CONFIG1	R/W	Configuration register one	0x60
0x8E	PPULSE	R/W	Proximity pulse count and length	0x40
0x8F	CONTROL	R/W	Gain control register	0x00
0x90	CONFIG2	R/W	Configuration register two	0x01
0x91	REVID	R	Revision ID	Rev
0x92	ID	R	Device ID	ID
0x93	STATUS	R	Device status	0x00
0x94	CDATAL	R	Clear ADC low data register	0x00
0x95	CDATAH	R	Clear ADC high data register	0x00

Address	Register Name	R/W	Register Function	Reset Value
0x96	RDATAL	R	Red ADC low data register	0x00
0x97	RDATAH	R	Red ADC high data register	0x00
0x98	GDATAL	R	Green ADC low data register	0x00
0x99	GDATAH	R	Green ADC high data register	0x00
0x9A	BDATAL	R	Blue ADC low data register	0x00
0x9B	BDATAH	R	Blue ADC high data register	0x00
0x9C	PDATA	R	Proximity ADC data register	0x00
0x9D	POFFSET_NE	R/W	Proximity offset for north and east photodiodes	0x00
0x9E	POFFSET_SW	R/W	Proximity offset for south and west photodiodes	0x00
0x9F	CONFIG3	R/W	Configuration register three	0x00
0xA0 (1)	CONFIG_A0	R/W	Configuration register A0	0x00
0xA1 (1)	CONFIG_A1	R/W	Configuration register A1	0x00
0xA2 (1)	CONFIG_A2	R/W	Configuration register A2	0x00
0xA3 (1)	CONFIG_A3	R/W	Configuration register A3	0x00
0xA4 (1)	CONFIG_A4	R/W	Configuration register A4	0x00
0xA5 (1)	CONFIG_A5	R/W	Configuration register A5	0x00
0xA6 (1)	CONFIG_A6	R/W	Configuration register A6	0x40
0xA7 (1)	CONFIG_A7	R/W	Configuration register A7	0x00
0xA8 (1)	CONFIG_A8	R	Configuration register A8	0x00
0xA9 (1)	CONFIG_A9	R/W	Configuration register A9	0x00

Address	Register Name	R/W	Register Function	Reset Value
0xAA [(1)]	CONFIG_AA	R/W	Configuration register AA	0x00
0xAB [(1)]	CONFIG_AB	R/W	Configuration register AB	0x00
0xAE [(1)]	GFLVL	R/W	Gesture FIFO Level	0x00
0xAF [(1)]	GSTATUS	R/W	Gesture status	0x00
0xE3	PBCLEAR	R/W	Pattern burst Interrupt clear	0x00
0xE4	IFORCE	R/W	Force Interrupt	0x00
0xE5	PICLEAR	R/W	Proximity interrupt clear	0x00
0xE6	CICLEAR	R/W	ALS interrupt clear	0x00
0xE7	AICLEAR	R/W	Clear all non-gesture interrupts	0x00
0xFC	GFIFO_N	R	Gesture north FIFO	0x00
0xFD	GFIFO_S	R	Gesture south FIFO	0x00
0xFE	GFIFO_W	R	Gesture west FIFO	0x00
0xFF	GFIFO_E	R	Gesture east FIFO	0x00

Note(s):

1. Register is shared between two or more functional modules. Physically, the device contains only one buffer, addressable from 0xA0 to 0xAF, register contents become available to any engine that is simultaneously activated. Care must be taken to clear all shared register space that does not contain controls/bits for the enabled function.

RAM Registers (0x00 - 0x7F)

Pattern RAM

Integrated RAM provides 128 bytes of bit-pattern data storage which defines the activation state of the LDR pin (LED ON/OFF) during burst event. After the device receives a "start burst command", each bit of RAM sets the state of the LDR pin for a time period defined by the timing register values. Bits are burst out of the LDR pin MSB first starting at address 0x00.

RAM can be accessed (read or write) a byte at a time or in pages of any length. RAM cannot be accessed while PON=0 or if a pattern is actively transmitting. RAM content is persistent as long as V_{DD} is present on the device.

The RAM is also used for gesture FIFO storage. As a result, when the gesture engine becomes enabled the pattern RAM will be overwritten.

Figure 45:
RAM Registers

7	6	5	4	3	2	1	0
NIBBLE0				NIBBLE1			

Field	Bits	Description
NIBBLE0	7:4	First 4-bits of bit-pattern generated. Burst bit 7 to bit 4.
NIBBLE1	3:0	Second 4-bits of bit-pattern generated. Burst bit 3 to bit 0.

Enable Register (ENABLE 0x80)

The Enable Register is used to power the device ON/OFF, enable functions and interrupts.

Figure 46:
Enable Register

7	6	5	4	3	2	1	0
PBEN	GEN	PIEN	AIEN	WEN	PEN	AEN	PON

Field	Bits	Description
PBEN	7	**Pattern Burst Enable.** When asserted, control of the LED driver pin (LDR) is managed by the IRBeam state machine. When PBEN is set, the proximity pulse will not be output to the LDR pin.
GEN	6	**Gesture Enable.** When asserted, the gesture state machine can be activated. Activation is subject to the states of PEN and GMODE bits.
PIEN	5	**Proximity Interrupt Enable.** When asserted, permits proximity interrupts to be generated, subject to the persist filter.
AIEN	4	**ALS Interrupt Enable.** When asserted, permits ALS interrupts to be generated, subject to the persistence filter setting.
WEN	3	**Wait Enable.** This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	**Proximity Enable.** This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	**ALS Enable.** This bit activates the Color functionality (Ambient Light Sense). Writing a 1 enables ALS. Writing a 0 disables ALS.
PON	0	**Power ON.** This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator and puts the part into a low power sleep mode. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON.

Note(s):

1. Before enabling Gesture, Proximity, or ALS, all of the bits associated with control of the desired function must be set. Changing control register values while operating may result in invalid results.

ADC Integration Time Register (ATIME 0x81)

The ATIME Register controls the internal integration time of ALS/Color analog to digital converters. Upon power up, the ADC integration time register is set to 0xFF.

The maximum count (or saturation) value can be calculated based upon the integration time and the size of the count register (i.e. 16 bits). For ALS/Color, the maximum count will be the lesser of either:

- 65535 (based on the 16 bit register size) or
- The result of equation: $Count_{MAX} = 1024 \times CYCLES + 1$

Figure 47:
ADC Integration Time Register

7	6	5	4	3	2	1	0
ATIME							

Field	Bits	Description			
ATIME	7:0	**REGISTER VALUE**	**CYCLES**	**TIME**	**Max Count**
		0xFF	1	2.78 ms	1025
		0xF6	10	27.8 ms	10241
		0xDB	37	103 ms	37888
		$= 256 - \frac{TIME}{2.78ms}$	….	….	….
		0xC0	64	178 ms	65535
		0x00	256	712 ms	65535

Note(s):

1. The ATIME register is only applicable to ALS/Color engine (16-bit data). The integration time for the 8-bit Proximity/Gesture engine, is a factor of four less than the nominal time (2.78ms), resulting in a fixed time of 0.696ms.

Wait Time Register (WTIME 0x83)

The WTIME controls the amount of time in a low power mode between Proximity and/or ALS cycles. It is set 2.78ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

Figure 48:
Wait Time Register

7	6	5	4	3	2	1	0
WTIME							

Field	Bits	Description			
		REGISTER VALUE	**WAIT TIME**	**TIME (WLONG=0)**	**TIME (WLONG=1)**
WTIME	7:0	0xFF	1	2.78 ms	0.03 s
		0xAB	85	236 ms	2.84 s
		$= 256 - \frac{TIME}{2.78ms}$	….	….	….
		0x00	256	712 ms	8.54 s

Note(s):

1. The wait time register should be configured before AEN and/or PEN is asserted.
2. During any Proximity and/or ALS cycle, the wait state, depicted in the functional block diagram, is entered. For example, Proximity only, Proximity and ALS, or ALS only cycles always enter the WAIT state and are separated by the time defined by WTIME.

ALS Interrupt Threshold Registers (0x84 – 0x87)

ALS level detection uses data generated by the Clear Channel. The ALS Interrupt Threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CDATA values. If AIEN is enabled and CDATA is not between $AI_{L/H}THH$ and $AI_{L/H}THL$ for the number of consecutive samples specified in APERS an interrupt is asserted on the interrupt pin.

Figure 49:
ALS Interrupt Threshold Registers

Registers	Address	Bits	Description
AILTHL	0x84	7:0	ALS low threshold lower byte
AIHTHL	0x85	7:0	ALS low threshold upper byte
AILTHH	0x86	7:0	ALS high threshold lower byte
AIHTHH	0x87	7:0	ALS high threshold upper byte

Proximity Interrupt Threshold Registers (0x89, 0x8B)

The Proximity Interrupt Threshold Registers set the high and low trigger points for the comparison function which generates an interrupt. If PDATA, the value generated by proximity channel, crosses below the lower threshold specified, or above the higher threshold, an interrupt may be signaled to the host processor. Interrupt generation is subject to the value set in persistence filter (PPERS).

Figure 50:
Proximity Interrupt Threshold Registers

Registers	Address	Bits	Description
PITHL	0x89	7:0	Proximity low threshold
PITHH	0x8B	7:0	Proximity high threshold

Interrupt Persistence Register (PERS 0x8C)

The Interrupt Persistence Register sets a value which is compared with the accumulated amount of ALS or Proximity cycles in which results were outside threshold values. Any Proximity or ALS result that is inside threshold values resets the count. Separate counters are provided for proximity and ALS persistence detection.

Figure 51:
Interrupt Persistence Register

7	6	5	4	3	2	1	0
PPERS				APERS			

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="7">PPERS</td><td rowspan="7">7:4</td><td colspan="2">Proximity Interrupt Persistence. Controls rate of proximity interrupt to the host processor.</td></tr>
<tr><td>FIELD VALUE</td><td>PERSISTENCE</td></tr>
<tr><td>0000</td><td>Every proximity cycle generates an interrupt</td></tr>
<tr><td>0001</td><td>Any value outside of threshold range</td></tr>
<tr><td>0010</td><td>2 consecutive values out of range</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>1111</td><td>15 consecutive values out of range</td></tr>
</table>

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="18">APERS</td><td rowspan="18">3:0</td><td colspan="2">ALS Interrupt Persistence. Controls rate of Clear channel interrupt to the host processor.</td></tr>
<tr><td>FIELD VALUE</td><td>PERSISTENCE</td></tr>
<tr><td>0000</td><td>Every ALS cycle generates an interrupt</td></tr>
<tr><td>0001</td><td>Any value outside of threshold range</td></tr>
<tr><td>0010</td><td>2 consecutive values out of range</td></tr>
<tr><td>0011</td><td>3 consecutive values out of range</td></tr>
<tr><td>0100</td><td>5 consecutive values out of range</td></tr>
<tr><td>0101</td><td>10 consecutive values out of range</td></tr>
<tr><td>0110</td><td>15 consecutive values out of range</td></tr>
<tr><td>0111</td><td>20 consecutive values out of range</td></tr>
<tr><td>1000</td><td>25 consecutive values out of range</td></tr>
<tr><td>1001</td><td>30 consecutive values out of range</td></tr>
<tr><td>1010</td><td>35 consecutive values out of range</td></tr>
<tr><td>1011</td><td>40 consecutive values out of range</td></tr>
<tr><td>1100</td><td>45 consecutive values out of range</td></tr>
<tr><td>1101</td><td>50 consecutive values out of range</td></tr>
<tr><td>1110</td><td>55 consecutive values out of range</td></tr>
<tr><td>1111</td><td>60 consecutive values out of range</td></tr>
</table>

Configuration Register One (CONFIG1 0x8D)

The CONFIG1 Register sets the wait long time.

Figure 52:
Configuration Register One

7	6	5	4	3	2	1	0
Reserved						WLONG	Reserved

Field	Bits	Description
Reserved	7	**Reserved.** Bits must be set to 0.
Reserved (1)	6	**Reserved.** Bit must be set to 1.
Reserved (2)	5	**Reserved.** Bit must be set to 1.
Reserved	4:2	**Reserved.** Bits must be set to 0.
WLONG	1	**Wait Long Enable**. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	**Reserved.** Bits must be set to 0.

Note(s):

1. Bit 6 is reserved, and is automatically set to 1 at POR.
2. Bit 5 is reserved, and is automatically set to 1 at POR. If this bit is not set, power consumption will increase during wait states.

Proximity Pulse Count and Length Register (PPULSE 0x8E)

The Proximity Pulse Count Register sets Pulse Width modified current during a Proximity Pulse. The proximity pulse count register bits set the number of pulses to be output on the LDR pin. The Proximity Length register bits set the amount of time the LDR pin is sinking current during a proximity pulse.

Figure 53:
Proximity Pulse Count and Length Register

7	6	5	4	3	2	1	0
PPLEN		PPULSE					

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">PPLEN</td><td rowspan="6">7:6</td><td colspan="2">Proximity Pulse Length. Sets the LED-ON pulse width during a Proximity LDR Pulse.</td></tr>
<tr><td>FIELD VALUE</td><td>LED ON</td></tr>
<tr><td>00</td><td>4µs</td></tr>
<tr><td>01</td><td>8µs</td></tr>
<tr><td>10</td><td>16µs</td></tr>
<tr><td>11</td><td>32µs</td></tr>
<tr><td>PPULSE</td><td>5:0</td><td colspan="2">Proximity Pulse Count. Specifies the number of Proximity pulses to be generated on LDR. Number of pulses is set by PPULSE value plus 1.</td></tr>
</table>

Note(s):

1. The time described by PPLEN is the actual signal integration time. The LED will be activated slightly longer (typically 1.36 µs) than the integration time.

Control Register (CONTROL 0x8F)

Figure 54:
Control Register

7	6	5	4	3	2	1	0
LDRIVE		RPINS	RINTPOL	PGAIN		AGAIN	

Field	Bits	Description	
LDRIVE	7:6	**LED Drive Strength** (Proximity, Pattern Burst modes)	
		FIELD VALUE	**LED Strength**
		00	100% (100mA typical)
		01	50%
		10	25%
		11	12.5%
RPINS	5	**LDR signal to INT**. Enabling this bit transfers pattern burst output from the LDR pin to the INT pin. While set, the LDR pin is deactivated.	
RINTPOL	4	**INT Pin Polarity.** With RPINS set, enabling this bit inverts the bit pattern output of the INT pin.	
PGAIN	3:2	**Proximity Gain Control**.	
		FIELD VALUE	**Proximity GAIN VALUE**
		00	1x Gain
		01	2x Gain
		10	4x Gain
		11	8x Gain
AGAIN	1:0	**ALS and Color Gain Control**.	
		FIELD VALUE	**RGBC GAIN VALUE**
		00	1x Gain
		01	4x Gain
		10	16x Gain
		11	64x Gain

Configuration Register Two (CONFIG2 0x90)

The Configuration Register Two independently enables or disables the saturation interrupts for Proximity and Clear channel. Saturation Interrupts are cleared by accessing the Clear Interrupt registers at 0xE5, 0xE6 and 0xE7. The LEDBOOST bits allow the LDR pin to sink more current above the maximum setting by LDRIVE and GLDRIVE.

Figure 55:
Configuration Register Two

7	6	5	4	3	2	1	0
PSIEN	CPSIEN	LEDBOOST		Reserved	Reserved	Reserved	Reserved

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>PSIEN</td><td>7</td><td colspan="2">Proximity Saturation Interrupt Enable.
0 = Proximity saturation interrupt disabled
1 = Proximity saturation Interrupt enabled</td></tr>
<tr><td>CPSIEN</td><td>6</td><td colspan="2">Clear Photodiode Saturation Interrupt Enable.
0 = ALS saturation interrupt disabled
1 = ALS saturation interrupt enabled</td></tr>
<tr><td rowspan="6">LEDBOOST</td><td rowspan="6">5:4</td><td colspan="2">LED Boost. Provides additional LDR current during LED pulses. Current value, set by LDRIVE, is increased by the percentage of LEDBOOST.</td></tr>
<tr><td>FIELD VALUE</td><td>LED ON</td></tr>
<tr><td>00</td><td>100%</td></tr>
<tr><td>01</td><td>150%</td></tr>
<tr><td>10</td><td>200%</td></tr>
<tr><td>11</td><td>300%</td></tr>
<tr><td>Reserved</td><td>3</td><td colspan="2">Reserved. Bit must be set to 0.</td></tr>
<tr><td>Reserved</td><td>2</td><td colspan="2">Reserved. Bit must be set to 0.</td></tr>
<tr><td>Reserved</td><td>1</td><td colspan="2">Reserved. Bit must be set to 0.</td></tr>
<tr><td>Reserved</td><td>0</td><td colspan="2">Reserved. Bit must be set to 1 and is set high by default during POR.</td></tr>
</table>

Note(s):

1. A LEDBOOST value of 00 results in 100% of the current as set by LDRIVE (i.e. No additional current).

Revision ID Register (REVID 0x91)

The read-only ID Register provides the die revision level.

Figure 56:
Revision Identification Register

7	6	5	4	3	2	1	0
Reserved					RevID		

Field	Bits	Description
Reserved	7:3	**Reserved.**
RevID	2:0	Wafer die revision level

ID Register (ID 0x92)

The read-only ID Register provides the device identification.

Figure 57:
Device Identification Register

7	6	5	4	3	2	1	0
ID						VID	

Field	Bits	Description
ID	7:2	**Device Identification** = 100111
VID	1:0	I^2C Bus Voltage ($V_{BUS} = V_{DD}$: 00, V_{BUS} = 1.8V : 10)

Status Register (STATUS 0x93)

The read-only Status Register provides the status of the device.

Figure 58:
Status Register

7	6	5	4	3	2	1	0
CPSAT	PGSAT	PINT	AINT	PBINT	GINT	PVALID	AVALID

Field	Bits	Description
CPSAT	7	**Clear Photodiode Saturation.** Assertion indicates that the analog sensor signal reached the upper end of its dynamic range. The bit can be de-asserted by sending a Clear channel interrupt command (0xE6 CICLEAR) or by disabling the ADC (AEN=0). This bit triggers an interrupt if CPSIEN is set.
PGSAT	6	**Proximity/Gesture Saturation.** Assertion indicates that an analog saturation event occurred during a previous proximity or gesture cycle. Once set, this bit remains set until cleared by the clear proximity interrupt command (0xE5 PICLEAR) or by disabling Proximity (PEN=0). This bit triggers an interrupt if PSIEN is set.
PINT	5	**Proximity Interrupt.** This bit triggers an interrupt if PIEN in ENABLE is set.
AINT	4	**ALS Interrupt.** This bit triggers an interrupt if AEN in ENABLE is set.
PBINT	3	**Pattern Burst Interrupt.** This bit triggers an interrupt if PBIEN in ICONFIG is set. (Mirrors PBINT2 bit in CONFIG_A8 register)
GINT	2	**Gesture Interrupt.** Assertion indicates that GFVLV has become greater than GFIFOTH or GVALID has become asserted when GMODE transitioned to zero. The bit is reset when FIFO is completely emptied (read).
PVALID	1	**Proximity Valid.** Indicates that a proximity cycle has completed since PEN was asserted or since PDATA was last read. A read of PDATA automatically clears PVALID.
AVALID	0	**ALS Valid.** Indicates that an ALS cycle has completed since AEN was asserted or since a read from any of the ALS/Color data registers.

RGBC Data Registers (0x94 – 0x9B)

Red, green, blue, and clear data is stored as 16-bit values. The read sequence must read byte pairs (low followed by high) starting on an even address boundary (0x94, 0x96, 0x98, or 0x9A) inside the RGBC Data Register block. When the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 59:
RGBC Data Registers

Registers	Address	Bits	Description
CDATAL	0x94	7:0	Clear Data Low Byte
CDATAH	0x95	7:0	Clear Data High Byte
RDATAL	0x96	7:0	Red Data Low Byte
RDATAH	0x97	7:0	Red Data High Byte
GDATAL	0x98	7:0	Green Data Low Byte
GDATAH	0x99	7:0	Green Data High Byte
BDATAL	0x9A	7:0	Blue Data Low Byte
BDATAH	0x9B	7:0	Blue Data High Byte

Note(s):

1. When reading register contents, a read of the lower byte data automatically latches the corresponding higher byte data (16 bit latch). This feature guarantees that the high byte value has not been updated by the ADC between I^2C reads. In addition, reading CDATAL register not only latches CDATAH but also latches all eight RGBC register simultaneously (64 bit latch).

Proximity Data Registers (PDATA 0x9C)

Proximity data is stored as an 8-bit value.

Figure 60:
Proximity Data Registers

7	6	5	4	3	2	1	0
PDATA							

Registers	Address	Bits	Description
PDATA	0x9C	7:0	Proximity Data Byte

Proximity North/East Offset (POFFSET_NE 0x9D)

In Proximity mode, the North and East photodiodes are connected forming a diode pair. The POFFSET_NE is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

Figure 61:
Proximity North/East Offset

7	6	5	4	3	2	1	0
POFFSET_NE							

Field	Bits	Description	
		Field Value	**Offset Correction Factor**
POFFSET_NE	7:0	01111111	127
		….	….
		00000001	1
		00000000	0
		10000001	-1
		10000010	-2
		….	….
		11111111	-127

Proximity South/West Offset (POFFSET_SW 0x9E)

In Proximity mode, the South and West photodiodes are connected forming a diode pair. The POFFSET_SW is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

Figure 62:
Proximity South/West Offset Register

7	6	5	4	3	2	1	0
POFFSET_SW							

Field	Bits	Description	
		Field Value	**Offset Correction Factor**
POFFSET_SW	7:0	01111111	127
		….	….
		00000001	1
		00000000	0
		10000001	-1
		10000010	-2
		….	….
		11111111	-127

Configuration Three Register (CONFIG3 0x9F)

The CONFIG3 register is used to select which photodiodes are used for proximity. Two photodiodes are paired to provide signal. In proximity mode, North and East photodiodes are connected forming a diode pair; similarly the South and West photodiodes form a diode pair.

Figure 63:
Configuration Three Register

7	6	5	4	3	2	1	0
Reserved		PCMP	SAI	PMSK_N	PMSK_S	PMSK_W	PMSK_E

Field	Bits	Description
Reserved	7:6	**Reserved.** Bits must be set to 0.
PCMP	5	**Proximity Gain Compensation Enable.** This bit provides gain compensation when proximity photodiode signal is reduced as a result of sensor masking. If only one diode of the diode pair is contributing, then only half of the signal is available at the ADC; this results in a maximum ADC value of 127. Enabling PCMP enables an additional gain of 2x, resulting in a maximum ADC value of 255. PMSK_X (N, S, E, W) → PCMP: 0,1,1,1 → 1 1,0,1,1 → 1 1,1,0,1 → 1 1,1,1,0 → 1 0,1,0,1 → 1 1,0,1,0 → 1 All Others → 0
SAI	4	**Sleep After Interrupt.** When enabled, the device will automatically enter low power mode when the INT pin is asserted and the state machine has progressed to the SAI decision block (Refer to Figure 28). Normal operation is resumed when INT pin is cleared over I²C.
PMSK_N	3	**Proximity Mask North Enable.** Writing a 1 disables this photodiode.
PMSK_S	2	**Proximity Mask South Enable.** Writing a 1 disables this photodiode.
PMSK_W	1	**Proximity Mask West Enable.** Writing a 1 disables this photodiode.
PMSK_E	0	**Proximity Mask East Enable.** Writing a 1 disables this photodiode.

Configuration Register A0 (CONFIG_A0), IRBeam Mode

While IRBeam is enabled, PBEN =1, the CONFIG_A0 register is used for IRBeam control bit configuration.

Figure 64:
Configuration Register A0

7	6	5	4	3	2	1	0
Reserved		PBIEN	SLEW	ISQZL	ISQZT		

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>Reserved</td><td>7:6</td><td colspan="2">Reserved. Bits must be set to 0 in IRBeam mode.</td></tr>
<tr><td>PBIEN</td><td>5</td><td colspan="2">Pattern Burst interrupt enable. When PBIEN = 1 the IRBeam interrupt is enabled.</td></tr>
<tr><td>SLEW</td><td>4</td><td colspan="2">Slew Rate Control. Always =0, unless in IRBeam mode with IBT register value less than 0x02. Slew is used to maintain LED pulse symmetry.</td></tr>
<tr><td>ISQZL</td><td>3</td><td colspan="2">IRBeam Symbol Quiet Zone LDR Logic state. When ISQZL = 1 and ISQZT > 0, LDR pin drives low with each “0” RAM pattern bit.</td></tr>
<tr><td rowspan="9">ISQZT</td><td rowspan="9">2:0</td><td colspan="2">IRBeam Symbol Quiet Zone Time. This time period represents the number of bit-times of quiet zone before and after the RAM bit pattern (symbol) is run.</td></tr>
<tr><td>FIELD VALUE</td><td>IRBeam Symbol Quiet Zone Time</td></tr>
<tr><td>000</td><td>0 bit-times (Not activated)</td></tr>
<tr><td>001</td><td>5 bit-times</td></tr>
<tr><td>010</td><td>9 bit-times</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>….</td><td>$\textit{Number of Bit Times} = 2 \times 2^{ISQZT} + 1$</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>111</td><td>257 bit-times</td></tr>
</table>

The ISQZT bit field defines the length of time between symbols pin. The LDR pin is set to the level defined by the ISQZL bit. The following equation governs the time delay:

(EQ4) $$t_{ISQZT} = (2 \times 2^{ISQZT} + 1) \cdot t_{IBT}$$

Configuration Register A1 (CONFIG_A1), IRBeam Mode

While in IRBeam mode, this register must be reset to 0x00. The value of this register will be overwritten during Gesture operation.

Figure 65:
Configuration Register A1

7	6	5	4	3	2	1	0
CONFIG_A1							

Register	Address	Bits	Description
CONFIG_A1	0xA1	7:0	Must be reset to 0x00

Note(s):

1. CONFIG_A1 must be set to 0x00 during IRBeam operation

Configuration Register A2 (CONFIG_A2), IRBeam Mode

While IRBeam is enabled, this register defines the number of times a complete Symbol is burst out of the LDR pin. A Symbol can be conceptualized as a "container" a single IRBeam data transmission.

The following equation describes the calculation of the Number of Symbol Loops:

(EQ5) $$\text{Number of Symbol Loops} = INSL + 1$$

Figure 66:
Configuration Register A2

7	6	5	4	3	2	1	0
ISNL							

Field	Bits	Description
ISNL	7:0	**IRBeam Number of Symbol Loops.** Number of Loops.

Configuration Register A3 (CONFIG_A3), IRBeam Mode

While IRBeam is enabled, this register defines the length of time that the LDR pin is disabled (I.e. LED is turned OFF) between consecutive symbol loops.

The following equation governs the time delay:

(EQ6) $$t_{ISDT} = [(2 \times ISOFF) + 1] \times t_{IBT}$$

The minimum *typical* Inter-Symbol LED OFF time is 0.54 µs. The maximum *typical* Inter-Symbol LED OFF time is 8.8 ms.

Figure 67:
Configuration Register A3

7	6	5	4	3	2	1	0
ISOFF							

Field	Bits	Description
ISOFF	7:0	**Sets the amount of LED Off time between Symbols.** Sets the delay between symbol bursts.

Configuration Register A4 (CONFIG_A4), IRBeam Mode

While IRBeam is enabled, this register defines the number of times a complete Packet is burst out of the LDR pin. A Packet can be conceptualized as a “container” for a number of complete Symbol Loops. The following equation describes the calculation of the Number of Packet Loops as a function of register setting value:

(EQ7) Number of Packet Loops = IPNL + 1

Figure 68:
Configuration Register A4

7	6	5	4	3	2	1	0
IPNL							

Field	Bits	Description
IPNL	7:0	**IRBeam Number of Packet Loops.** Number of Loops.

Configuration Register A5 (CONFIG_A5), IRBeam Mode

While IRBeam is enabled, this register defines the length of time that the LDR pin is disabled (i.e. LED is turned OFF) between consecutive Packet loops. The following equation governs the time delay:

(EQ8) $$t_{IPDT} = 4 \times (IPOFF + 1) \times t_{IBT}$$

The minimum *typical* inter-Packet LED OFF time is 1.0 µs. The maximum *typical* inter-Packet LED OFF time 17.7ms.

Figure 69:
Configuration Register A5

7	6	5	4	3	2	1	0
IPOFF							

Field	Bits	Description
IPOFF	7:0	**IRBeam Packet OFF Delay Time.** Sets the amount of LED OFF time between Packets.

Configuration Register A6 (CONFIG_A6), IRBeam Mode

While in IRBeam mode, this register selects the pulse width of one bit-time. This is fundamental time period for pattern generation.

The minimum *typical* bit-time 0.27µs (IBT = 0). The maximum *typical* bit-time is 17.28µs (IBT = 0x3F).

Figure 70:
Configuration Register A6

7	6	5	4	3	2	1	0
Reserved		IBT					

Field	Bits	Description
Reserved	7:6	**Reserved.** Bits must be set to 0 in IRBeam mode.
IBT	5:0	**IRBeam Bit Time.** Defines the pulse width for one bit-time.

The IRBeam bit time is set by the following equation:

(EQ9) $$t_{IBT} = (IBT + 1) \times 0.27\mu s$$

Configuration Register A7 (CONFIG_A7), IRBeam Mode

While IRBeam is enabled, this register defines the number of nibbles in Symbol bit-pattern RAM (0x00 to 0x7F) that will be processed to modulate a bit-pattern on the LDR during a single symbol transmission. Each bit stored in a RAM location corresponds to a single Bit-time. Since ILEN is measured in nibbles (half-bytes) the smallest burst out of the LDR pin is four bit-times. The largest burst time is 1024 bit-times. The following equation describes the number of nibbles processed as a function of register setting value:

(EQ10) ISLEN = Number of Nibbles - 1

Figure 71:
Configuration Register A7

7	6	5	4	3	2	1	0
ISLEN							

Field	Bits	Description
ISLEN	7:0	**IRBeam Symbol bit-pattern Length in nibbles.** Any write to this register initiates an IRBeam event. ISLEN is the number of nibbles to burst out of LDR/LED.

Configuration Register A8 (CONFIG_A8), IRBeam Mode

While IRBeam is enabled, this register provides the status of the IRBeam state machine. This register is read only.

Figure 72:
Configuration Register A8

7	6	5	4	3	2	1	0
Reserved						PBINT2	PBUSY

Field	Bits	Description
Reserved	7:2	**Reserved.**
PBINT2	1	**Pattern Burst Interrupt Two.** A high logic level indicates that an IRBeam event has run to completion. This bit is reset using the PBCLEAR register is written. The same bit can also be accessed in STATUS register to permit the CPU detection of interrupt cause with a single I^2C read transaction.
PBUSY	0	**Pattern Burst Busy.** Indicates a Pattern burst (IRBeam transmission) is in progress.

Configuration Register A0 (CONFIG_A0), Gesture Mode

This register value is compared with Proximity value, PDATA, to determine if the gesture state machine is entered. The proximity persistence filter, PPERS, is not used to determine gesture state machine entry.

Figure 73:
Configuration Register A0

7	6	5	4	3	2	1	0
GPENTH							

Field	Bits	Description
GPENTH	7:0	**Gesture Proximity Entry Threshold.** This register sets the Proximity threshold value used to determine a "gesture start" and subsequent entry into the gesture state machine.

Configuration Register A1 (CONFIG_A1), Gesture Mode

The Gesture Exit Threshold Register value is compared all non-masked gesture detection photodiodes (NSWE). Gesture state machine exit is also governed by the value in the Gesture Exit Persistence register, GEPERS.

Figure 74:
Configuration Register A1

7	6	5	4	3	2	1	0
GEXTH							

Field	Bits	Description
GEXTH	7:0	**Gesture Exit Threshold.** This register sets the threshold value used to determine a "gesture end" and subsequent exit of the gesture state machine. Setting GEXTH to 0x00 will prevent gesture exit until GMODE is set to 0.

Configuration Register A2 (CONFIG_A2), Gesture Mode

This register contains settings that govern gesture detector masking, FIFO interrupt generation, and gesture exit persistence filter.

Figure 75:
Configuration Register A2

7	6	5	4	3	2	1	0
GFIFIOTH		GEXMSK				GEXPERS	

Field	Bits	Description	
GFIFOTH	7:6	**Gesture FIFO Threshold.** This value is compared with the FIFO Level (i.e. the number of NSWE datasets) to generate an interrupt (if enabled).	
		Field Value	**THRESHOLD**
		00	Interrupt is generated after 1 dataset is added to FIFO
		01	Interrupt is generated after 4 dataset is added to FIFO
		10	Interrupt is generated after 8 dataset is added to FIFO
		11	Interrupt is generated after 16 dataset is added to FIFO
GEXMSK	5:2	**Gesture Exit Mask.** Controls which of the gesture detector photodiodes (NSWE) will be included to determine a "gesture end" and subsequent exit of the gesture state machine. Unmasked NSWE data will be compared with the value in GEXTH. Field value bits correspond to NSWE detectors.	
		Field Value	**EXIT MASK**
		0000	All NSWE detector data will be included in sum.
		0001	E detector data will not be included in sum.
		0010	W detector data will not be included in sum.
		0100	S detector data will not be included in sum.
		1000	N detector data will not be included in sum.
		0101	….
		0110	W & S detector data will not be included in the sum.
		1111	….

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">GEXPERS</td><td rowspan="6">1:0</td><td colspan="2">Gesture Exit Persistence. When a number of consecutive “gesture end” occurrences become equal or greater to the GEXPERS value, the Gesture state machine is exited.</td></tr>
<tr><td>Field Value</td><td>PERSISTENCE</td></tr>
<tr><td>00</td><td>First “gesture end” occurrence results in gesture state machine exit.</td></tr>
<tr><td>01</td><td>Second “gesture end” occurrence results in gesture state machine exit.</td></tr>
<tr><td>10</td><td>Fourth “gesture end” occurrence results in gesture state machine exit.</td></tr>
<tr><td>11</td><td>Seventh “gesture end” occurrence results in gesture state machine exit.</td></tr>
</table>

Configuration Register A3 (CONFIG_A3), Gesture Mode

This register contains settings that govern wait time, LDR drive current strength and Gesture gain control. The GWTIME controls the amount of time in a low power mode between gesture detection cycles. GPDRIVE sets the LDR drive current strength governing LED intensity. GGAIN sets the analog gain associated with the photodiode output.

Figure 76:
Configuration Register A3

7	6	5	4	3	2	1	0
GENAL	GGAIN		GLDRIVE		GWTIME		

Field	Bits	Description	
GENAL	7	**Gesture Enter Always.** With Gesture enabled, If GENAL= 1, any PDATA result (including 0) will always cause entry into the gesture state machine. If GENAL = 0, entry into the gesture state machine is conditional based on PDATA and GPENTH.	
GGAIN	6:5	**Gesture Gain.** Gesture Gain Control.	
		Field Value	**GESTURE GAIN VALUE**
		00	1x Gain
		01	2x Gain
		10	4x Gain
		11	8x Gain
GLDRIVE	4:3	**Gesture LED Drive Strength.** Sets LED Drive Strength in gesture mode.	
		FIELD VALUE	**LED Strength**
		00	100% (100mA typical)
		01	50%
		10	25%
		11	12.5%

Field	Bits	Description	
GWTIME	2:0	**Gesture Wait Time.** The GWTIME controls the amount of time in a low power mode between gesture detection cycles	
		Field Value	**WAIT TIME**
		000	0ms
		001	2.8ms
		010	5.6ms
		011	8.4ms
		100	14ms
		101	22.4ms
		110	30.8ms
		111	39.2ms

Note(s):

1. The wait time register should be configured before GEN is asserted.
2. The time described by GWTIME is the actual signal integration time. The LED will be activated slightly longer (typically 1.33 µs) than the integration time.

Configuration Register A4 (CONFIG_A4), Gesture Mode

The GOFFSET_N is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

Figure 77:
Configuration Register A4

7	6	5	4	3	2	1	0
GOFFSET_N							

Field	Bits	Description	
GOFFSET_N	7:0	**Field Value**	**OFFSET CORRECTION FACTOR**
		01111111	127
		….	….
		00000001	1
		00000000	0
		10000001	-1
		10000010	-2
		….	….
		11111111	-127

Configuration Register A5 (CONFIG_A5), Gesture Mode

The GOFFSET_S is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

Figure 78:
Configuration Register A5

7	6	5	4	3	2	1	0
GOFFSET_S							

Field	Bits	Description	
GOFFSET_S	7:0	**Field Value**	**OFFSET CORRECTION FACTOR**
		01111111	127
		….	….
		00000001	1
		00000000	0
		10000001	-1
		10000010	-2
		….	….
		11111111	-127

Configuration Register A6 (CONFIG_A6), Gesture Mode

GPLEN Register sets Pulse Width Modified current during a Gesture Pulse. The Gesture pulse count register bits set the number of pulses to be output on the LDR pin. The Gesture Length register bits set the amount of time the LDR pin is sinking current during a gesture pulse.

Figure 79:
Configuration Register A6

7	6	5	4	3	2	1	0
GPLEN		GPULSE					

Field	Bits	Description	
GPLEN	7:6	**Gesture Pulse Length.** Sets the LED-ON pulse width during a Gesture LDR Pulse.	
		Field Value	**LED ON**
		00	4µs
		01	8µs
		10	16µs
		11	32µs
GPULSE	5:0	**Gesture Pulse Count.** Specifies the number of pulses to be generated on LDR. Number of pulses is set by GPULSE value plus 1.	

Configuration Register A7 (CONFIG_A7), Gesture Mode

The GOFFSET_W is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

Figure 80:
Configuration Register A7

7	6	5	4	3	2	1	0
GOFFSET_W							

Field	Bits	Description	
GOFFSET_W	7:0	**Field Value**	**OFFSET CORRECTION FACTOR**
		01111111	127
		….	….
		00000001	1
		00000000	0
		10000001	-1
		10000010	-2
		….	….
		11111111	-127

Configuration Register A9 (CONFIG_A9), Gesture Mode

The GOFFSET_E is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

Figure 81:
Configuration Register A9

7	6	5	4	3	2	1	0
GOFFSET_E							

Field	Bits	Description	
GOFFSET_E	7:0	**Field Value**	**OFFSET CORRECTION FACTOR**
		01111111	127
		....	....
		00000001	1
		00000000	0
		10000001	-1
		10000010	-2
		....	....
		11111111	-127

Configuration Register AA (CONFIG_AA), Gesture Mode

This register contains settings that govern which gesture photodiode pair: North-South and/or East-West will be enabled (have valid data in FIFO) while the gesture state machine is collecting directional data. Normal mode enables all four gesture photodiodes and places data into FIFO as expected. Disabling a photodiode pair, essentially allows the enabled pair to collect data twice as fast. Data stored in the FIFO for a disabled pair is not valid. This feature is useful to improve reliability and accuracy of gesture detection when only North-South or East-West gestures are expected.

Figure 82:
Configuration Register AA

7	6	5	4	3	2	1	0
Reserved						GDIMS	

Field	Bits	Description	
Reserved	7:2	**Reserved.** Bits must be set to 0.	
GDIMS	1:0	**Gesture Dimension Select.** Selects which gesture photodiode pairs are enabled to gather results during gesture.	
		Field Value	**PERSISTENCE**
		00	Both Pairs active. NS and WE FIFO data is valid.
		01	Only the NS pair is active. Ignore WE data in FIFO.
		10	Only the WE pair is active. Ignore NS data in FIFO.
		11	Both Pairs active. NS and WE FIFO data is valid.

Configuration Register AB (CONFIG_AB), Gesture Mode

This register contains settings that govern Gesture interrupts as well as operation mode control.

Figure 83:
Configuration Register AB

7	6	5	4	3	2	1	0
Reserved						GIEN	GMODE

Field	Bits	Description
Reserved	7:2	**Reserved.** Bits must be set to 0.
GIEN	1	**Gesture Interrupt Enable.** When asserted, all gesture related interrupts are unmasked.
GMODE	0	**Gesture Mode.** Reading this bit reports if the gesture state machine is actively running, 1 = Gesture, 0= ALS, Proximity, Color, and Pattern Burst. Writing a 1 to this bit causes immediate entry in to the gesture state machine (as if GPENTH had been exceeded). Writing a 0 to this bit causes exit of gesture when current analog conversion has finished (as if GPEXTH had been exceeded).

Configuration Register AE (CONFIG_AE), Gesture Mode

This indicates the number of datasets that are currently available in the FIFO for read. Reading a complete FIFO dataset (from address 0xFC to 0xFF) constitutes the reduction of the GPENTH register by one.

Figure 84:
Configuration Register AE

7	6	5	4	3	2	1	0
GFLVL							

Field	Bits	Description
GFLVL	7:0	**Gesture FIFO Level.** This register indicates how many four byte data points—NSWE are ready for read over I^2C. One four-byte dataset is equivalent to a single count in GFLVL.

Configuration Register AF (CONFIG_AF), Gesture Mode

This register indicates the operational condition of the gesture state machine.

Figure 85:
Configuration Register AF

7	6	5	4	3	2	1	0
Reserved						GFOV	GVALID

Field	Bits	Description
Reserved	7:2	**Reserved.**
GFOV	1	**Gesture FIFO Overflow.** A setting of 1 indicates that the FIFO has filled to capacity and that new gesture detector data has been lost.
GVALID	0	**Gesture Valid.** GVALID bit is set when GFLVL becomes greater than GFIFOTH (i.e. FIFO has enough data to set GINT). GVALID is reset when GMODE = 0 and the GFLVL=0 (i.e. All FIFO data has been read).

Note(s):

1. If GINT (irrespective of GVALID) remains set after the FIFO has been read GFLVL times, this indicates that new data has been added to FIFO during the last FIFO read.

Clear Interrupt Registers (0xE3, 0xE7)

Interrupts are cleared by read or write access to the appropriate register. IFORCE is used to manually assert the INT pin.

Figure 86:
Clear Interrupt Registers

Registers	Address	Bits	Description
PBCLEAR	0xE3	7:0	Pattern Burst interrupt clear
IFORCE	0xE4	7:0	Forces an interrupt
PICLEAR	0xE5	7:0	Proximity interrupt clear
CICLEAR	0xE6	7:0	ALS interrupt clear
AICLEAR	0xE7	7:0	Clears all non-gesture interrupts

Gesture FIFO Access Registers (0xFC − 0xFF)

In Gesture mode, the RAM area is repurposed as a 128 byte FIFO. Data is stored in four byte blocks. Each block, called a dataset, contains one integration cycle of North, South, West, & East gesture data. Thirty-two separate datasets are stored within the FIFO before wrap-around overflow. If the FIFO overflows (i.e. 33 datasets before host/system can empty FIFO) new datasets will not replace existing datasets; instead an overflow flag will be set and new data will be lost.

Host/Systems acquire gesture data by reading addresses: 0xFC, 0xFD, 0xFE, & 0xFF, which directly correspond to North, South, West, and East data points. Data can be read a single byte at a time (four consecutive I^2C transactions) or by using a page read. The internal FIFO read pointer and the FIFO Level register, GFIFOLVL, values are updated when address 0xFF is accessed (single byte transactions) or when every fourth byte, corresponding to address 0xFF, is accessed in page mode. If the FIFO continues to be accessed after GFIFOLVL register is zero, dataset will be read as zero values.

The recommended procedure for reading data stored in the FIFO begins when a gesture interrupt is generated (GFIFOLVL > GFIFOTH). Next, the host reads the FIFO Level register, GFIFOLVL, to determine the amount of valid data in the FIFO. Finally, the host begins to read address 0xFC (page read), and continues to read (clock-out data) until the FIFO is empty (Number of bytes is 4x GFIFOLVL). For example, if GFIFOLVL = 2, then the host should initiate a read at address 0xFC, and sequentially read all eight bytes. As the four-byte blocks are read, GFIFOLVL register is decremented and the internal FIFO pointers are updated.

Figure 87:
Gesture FIFO Access Registers

Registers	Address	Bits	Description
GFIFO_N	0xFC	7:0	Gesture North FIFO
GFIFO_S	0xFD	7:0	Gesture South FIFO
GFIFO_W	0xFE	7:0	Gesture West FIFO
GFIFO_E	0xFF	7:0	Gesture East FIFO

Application Information

Power Supply Considerations

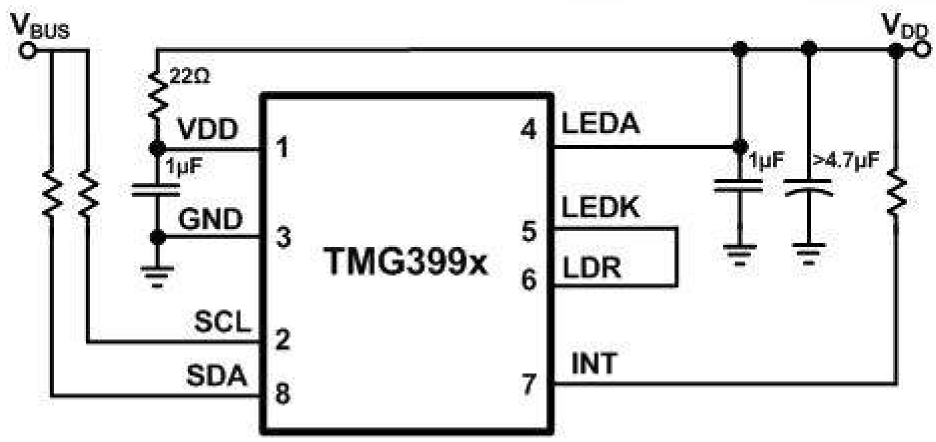
Systems using Proximity detection are capable of driving the integrated LED with as much as 300mA of pulsed current; however typical systems require much lower settings of 100mA or less. As a result of the rapidly switching current on LDR pin, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Systems where battery voltage does not exceed the maximum specified LDR pin voltage (including battery recharge conditions), the LEDA may be directly connected to the battery. This is beneficial because noise generated by LED pulsing is not couple into the supply of the optical device. Another advantage for this configuration, depending on system design, may be a reduction or removal of additional bulk capacitance connected to LEDA.

In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LED, the key goal can be meet.

Place a 1µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, along with a bulk storage capacitor, 4.7µF or larger, (as needed) somewhere along the trace to supply surge currents when the LED is pulsed.

If operating from a single supply, use a 22-Ω resistor in series with the V_{DD} supply line and a 1µF low ESR capacitor to filter any power supply noise. The previous capacitor placement recommendations apply.

Figure 88:
Typical Application Hardware Circuit



Communications Considerations

VBUS in the above figures refers to the I^2C bus voltage. Separate part numbers are assigned to each of the I^2C VBUS options: VBUS = V_{DD}, or VBUS=1.8 V.

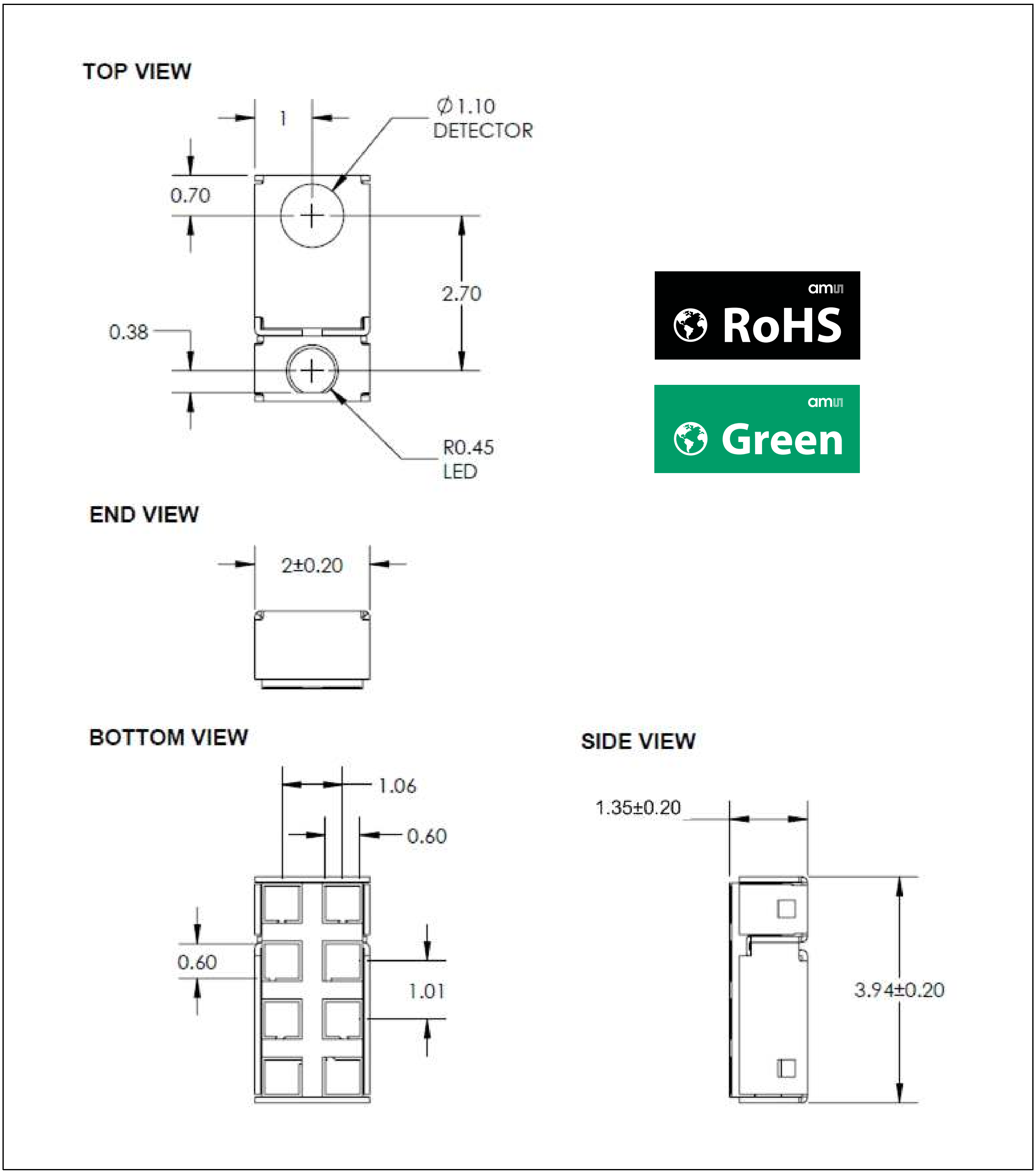
The I^2C signals and the Interrupt are open-drain outputs and require pull−up resistors. The pull-up resistor (RP) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. For example, **ams** EVM hardware communicates at 400 kbit/s and uses 1.5 kΩ pull-up resistors. The **ams** EVM hardware uses a 10 kΩ pull-up resistor (RPI) on interrupt pin.

LED Drive Considerations

The LED cathode is connected to the LDR pin which functions as a regulated current sink. When selecting the power supply for the LED, that is, the voltage placed on the LEDA pin, it is important to choose a supply capable of supplying a sufficient amount of current and voltage. LEDA voltage must be larger than the sum of the LED forward voltage drop and the voltage on the LDR/ LEDA current sink regulator.

Package Drawings & Markings

Figure 89:
Package Mechanical Drawing & Marking



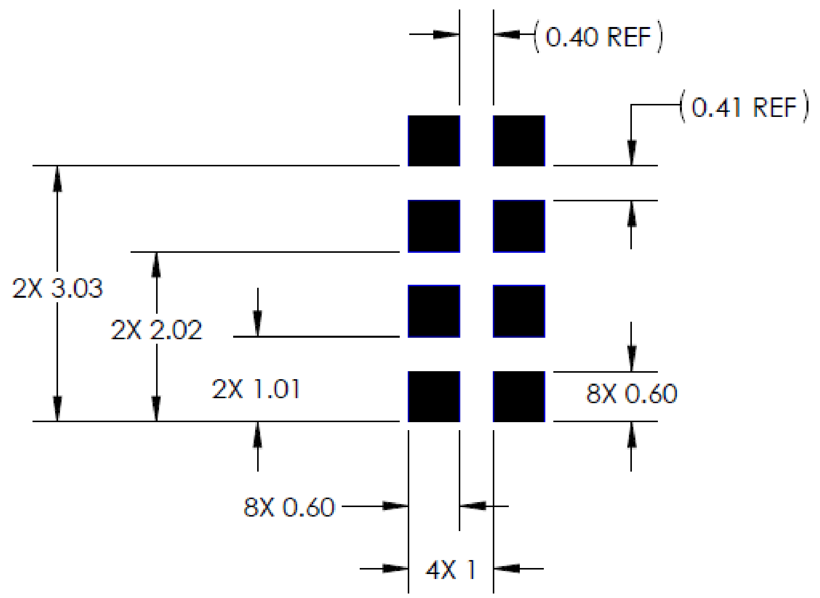
Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerance is ±0.05mm unless otherwise noted.
3. Contacts are copper with NiPdAu plating.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 90:
Recommended PCB Pad Layout

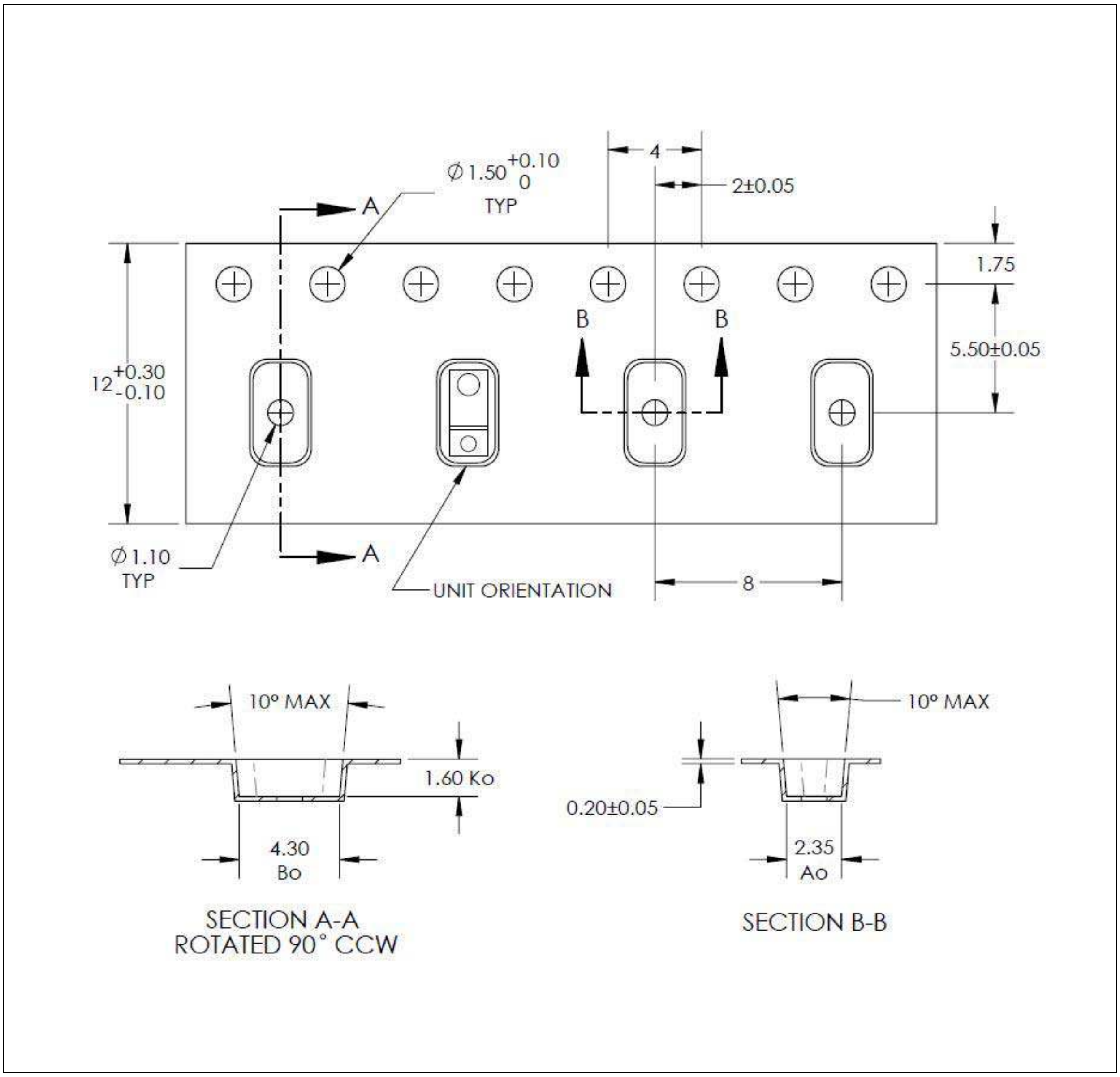


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Packaging Mechanical Data

Figure 91:
Tape & Reel Mechanical Drawing



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_O, B_O, and K_O are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is 330 millimeters in diameter and contains 5000 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering & Storage Information

Soldering Information

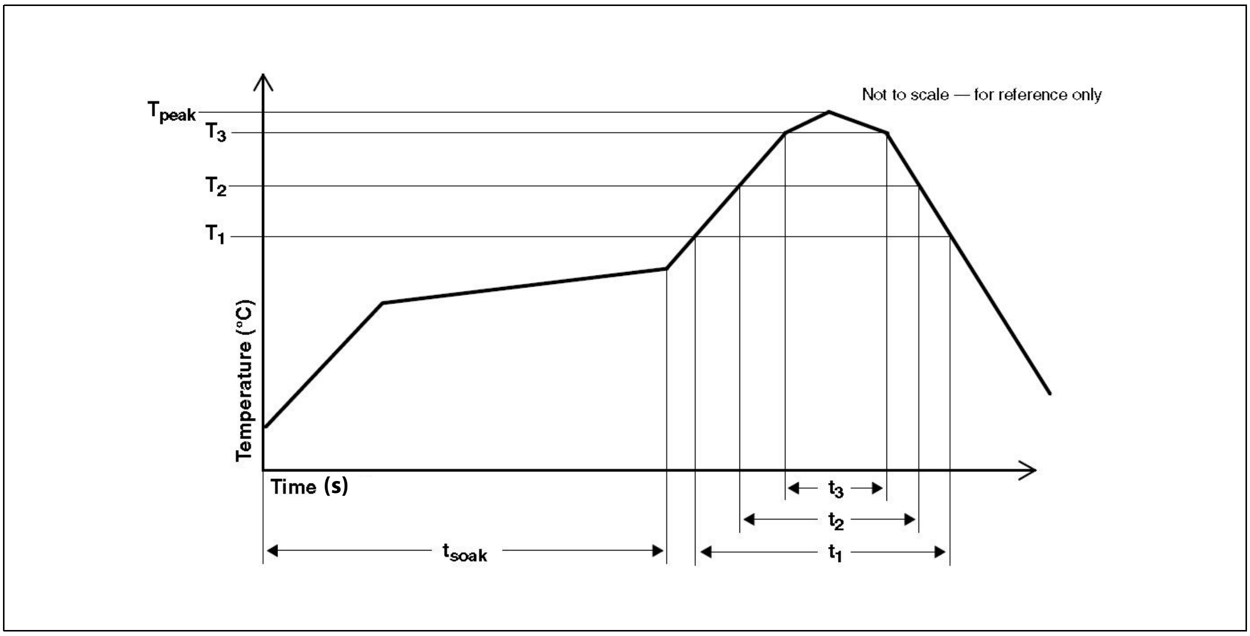
The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 92:
Soldering Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T_1)	t_1	Max 60 s
Time above 230 °C (T_2)	t_2	Max 50 s
Time above T_{peak} - 10 °C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/s

Figure 93:
Soldering Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 94:
Ordering Information

Ordering Code	Address	Interface	Delivery Form
TMG39921 [(1)]	0x39	I^2C Vbus = V_{DD} Interface	Module-8, 2.0mm Width
TMG39923	0x39	I^2C Vbus = 1.8V Interface	Module-8, 2.0mm Width
TMG39925 [(1)]	0x29	I^2C Vbus = V_{DD} Interface	Module-8, 2.0mm Width
TMG39927 [(1)]	0x29	I^2C Vbus = 1.8V Interface	Module-8, 2.0mm Width

Note(s):

1. Contact **ams** for availability.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
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Revision Information

Changes from 1-04 (2014-Oct-24) to current revision 1-06 (2018-Feb-27)	Page
1-04 (2014-Oct-24) to 1-05 (2017-Apr-13)	
Updated EQ6	65
1-05 (2017-Apr-13) to 1-06 (2018-Feb-27)	
Updated Figure 94	89

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide