

PNP SILICON POWER TRANSISTOR ARRAY HIGH SPEED SWITCHING USE INDUSTRIAL USE

DESCRIPTION

The μPA1453 is PNP silicon epitaxial Power Transistor Array that built in 4 circuits designed for driving solenoid, relay, lamp and so on.

FEATURES

- Easy mount by 0.1 inch of terminal interval.
- High h_{FE} . Low $V_{CE(sat)}$.
 $h_{FE} = 100$ to 400 (at $I_C = -2$ A)
 $V_{CE(sat)} = -0.3$ V MAX. (at $I_C = -2$ A)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPA1453H	10 Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25$ °C)

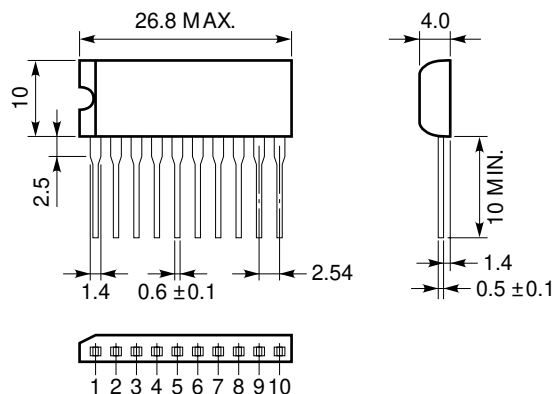
Collector to Base Voltage	V_{CBO}	-60	V
Collector to Emitter Voltage	V_{CEO}	-60	V
Emitter to Base Voltage	V_{EBO}	-7	V
Collector Current (DC)	$I_{C(DC)}$	-5	A/unit
Collector Current (pulse)	$I_{C(pulse)^*}$	-10	A/unit
Base Current (DC)	$I_{B(DC)}$	-1.0	A/unit
Total Power Dissipation	P_{T1}^{**}	3.5	W
Total Power Dissipation	P_{T2}^{***}	28	W
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

* $PW \leq 300$ μs, Duty Cycle ≤ 10 %

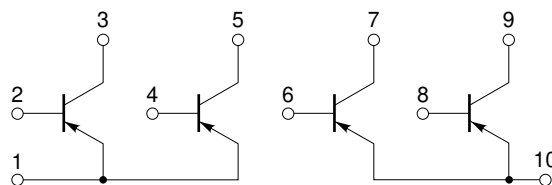
** 4 Circuits, $T_a = 25$ °C

*** 4 Circuits, $T_c = 25$ °C

PACKAGE DIMENSION (in millimeters)



CONNECTION DIAGRAM



PIN No.

- 2, 4, 6, 8: Base (B)
- 3, 5, 7, 9: Collector (C)
- 1, 10 : Emitter (E)

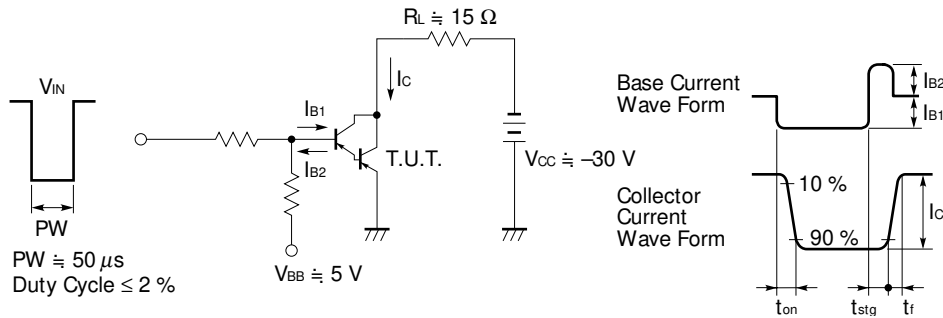
The information in this document is subject to change without notice.

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

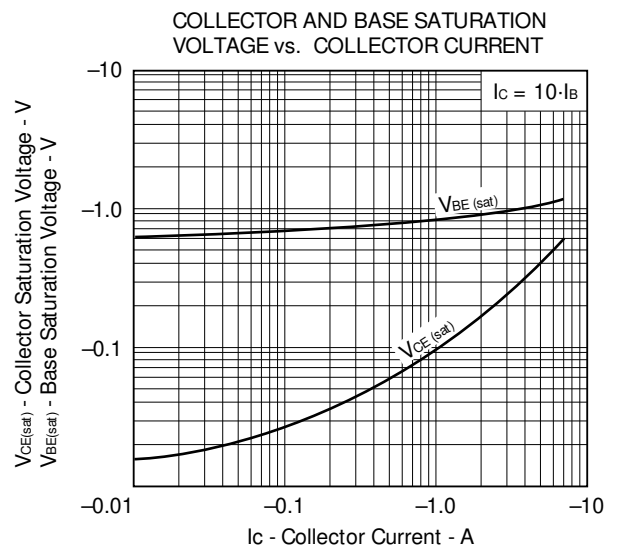
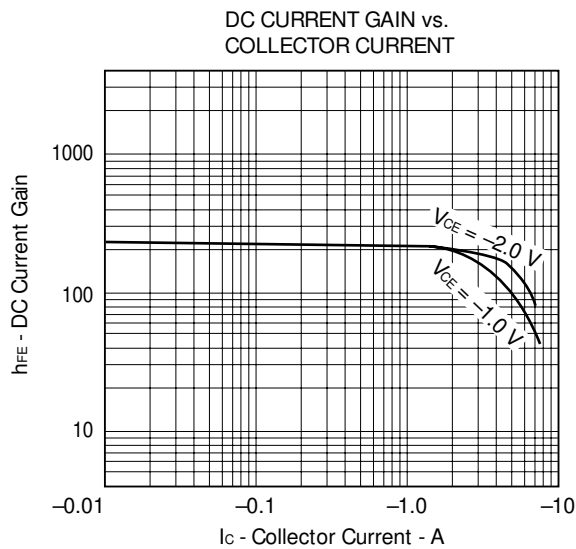
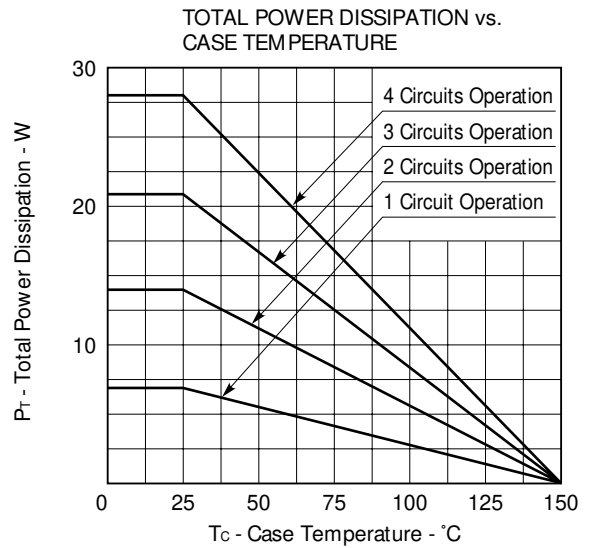
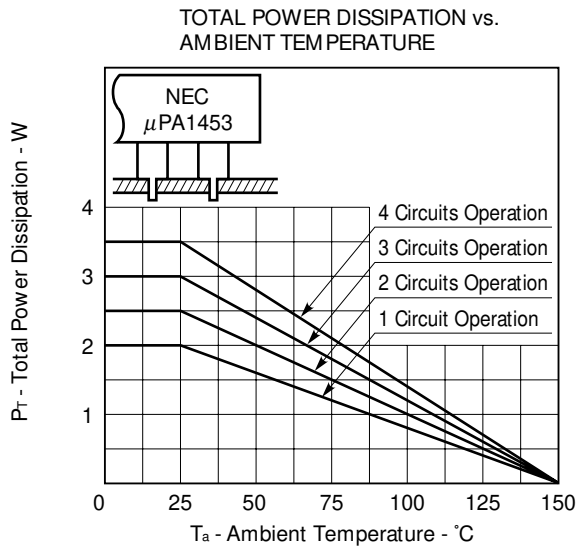
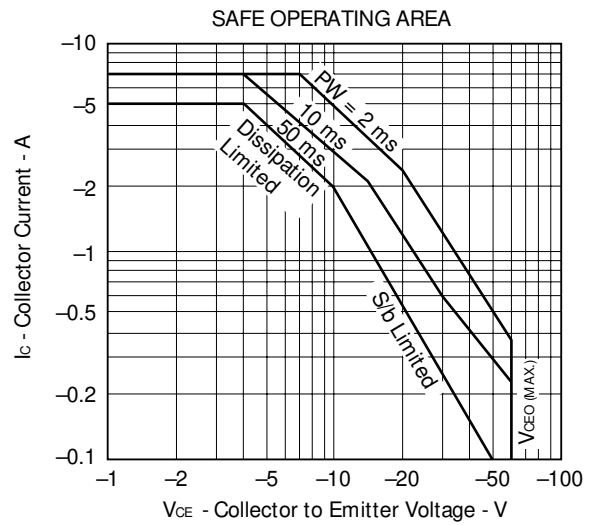
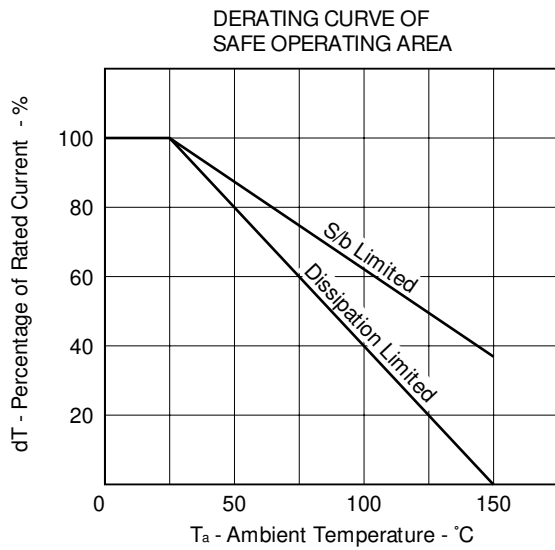
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Leakage Current	I_{CBO}			-10	μA	$V_{CB} = -50\text{ V}, I_E = 0$
Emitter Leakage Current	I_{EBO}			-10	μA	$V_{EB} = -5\text{ V}, I_C = 0$
DC Current Gain	h_{FE1} *	60	220		—	$V_{CE} = -1\text{ V}, I_C = -0.1\text{ A}$
DC Current Gain	h_{FE2} *	100	220	400	—	$V_{CE} = -1\text{ V}, I_C = -2\text{ A}$
DC Current Gain	h_{FE3} *	50	100			$V_{CE} = -2\text{ V}, I_C = -5\text{ A}$
Collector Saturation Voltage	$V_{CE(sat)}$ *		-0.2	-0.3	V	$I_C = -2\text{ A}, I_B = -0.2\text{ A}$
Base Saturation Voltage	$V_{BE(sat)}$ *		-0.9	-1.2	V	$I_C = -2\text{ A}, I_B = -0.2\text{ A}$
Turn On Time	t_{on}			1	μs	$I_C = -2\text{ A}$
Storage Time	t_{stg}			2.5	μs	$I_{B1} = -I_{B2} = -0.2\text{ A}$
Fall Time	t_f			1	μs	$V_{CC} \approx -30\text{ V}, R_L \approx 15\ \Omega$ See test circuit

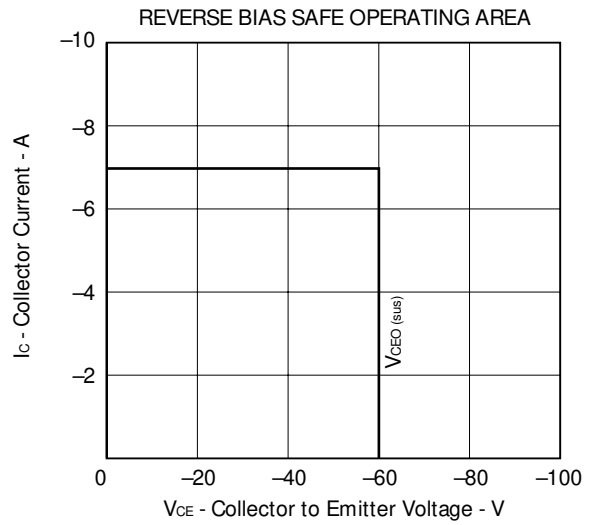
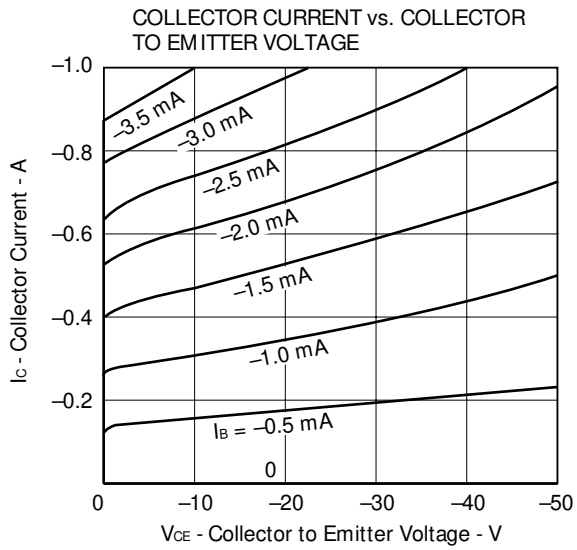
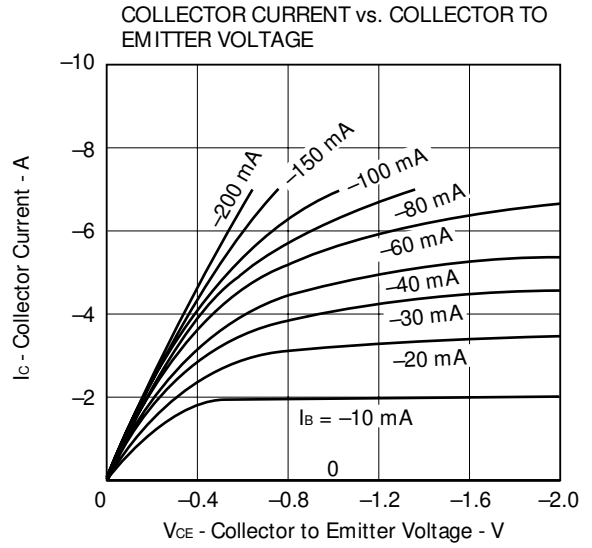
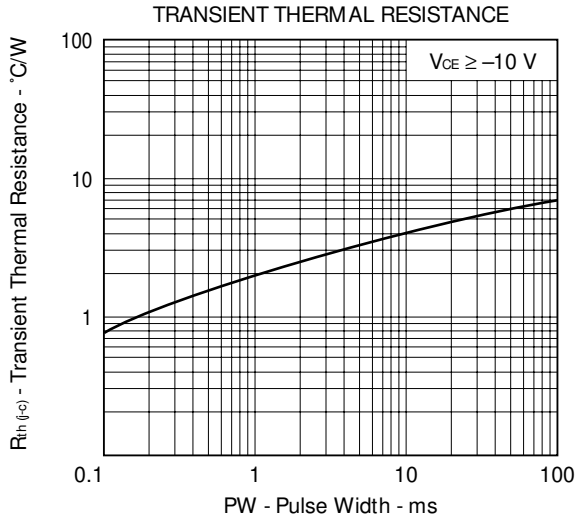
* $PW \leq 350\ \mu s$, Duty Cycle $\leq 2\%$ / pulsed

SWITCHING TIME TEST CIRCUIT



TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134

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