CSD83325L 12-V Dual N-Channel NexFET™ Power MOSFET

1 Features

- Common Drain Configuration
- Low-On Resistance
- Small Footprint of 2.2 mm × 1.15 mm
- Lead Free
- RoHS Compliant
- Halogen Free
- Gate ESD Protection

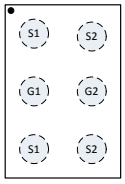
2 Applications

- Battery Management
- Battery Protection

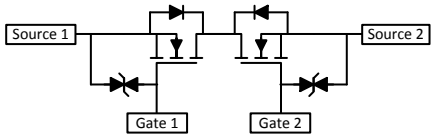
3 Description

This 12-V, 9.9-mΩ, 2.2-mm × 1.15-mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance and gate charge in a small footprint. Its small footprint and common drain configuration make the device ideal for battery pack applications in small handheld devices.

Top View



Configuration



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{S1S2}	Source-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	8.4		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.9		nC
$R_{S1S2(on)}$	Source-to-Source On Resistance	V_{GS} = 2.5 V	17.5	mΩ
		V_{GS} = 3.8 V	10.9	mΩ
		V_{GS} = 4.5 V	9.9	mΩ
$V_{GS(th)}$	Threshold Voltage	0.95		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD83325L	3000	7-Inch Reel	2.20-mm × 1.15-mm Land Grid Array (LGA) Package	Tape and Reel
CSD83325LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

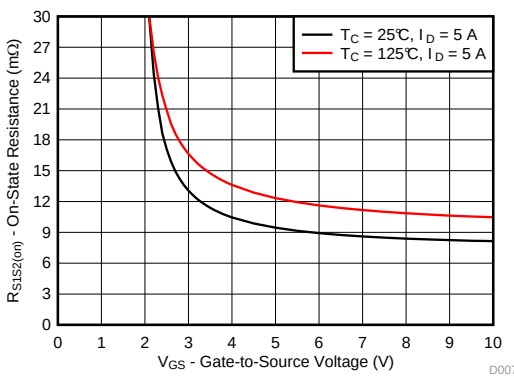
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_S	Continuous Source Current(1)	8	A
I_{SM}	Pulsed Source Current(2)	52	A
P_D	Power Dissipation	2.3	W
$V_{(ESD)}$	Human-Body Model (HBM)	2000	V
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C

(1) Device operating at a temperature of 105ºC.

(2) Typical min Cu $R_{\theta JA}$ = 150°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

$R_{DS(on)}$ vs V_{GS}



Gate Charge

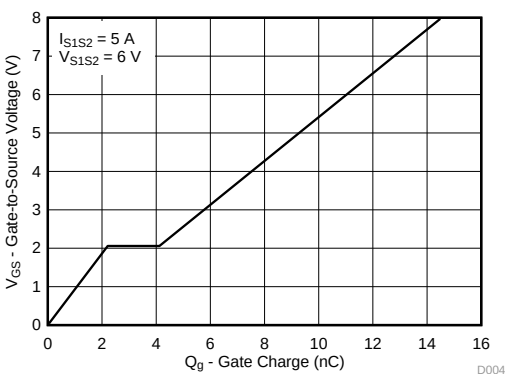


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2016) to Revision B **Page**

- Added Diode Characteristics ($V_{F(S-S)}$) in the *Electrical Characteristics* table ... 3
- Added Figure 9 to *Typical MOSFET Characteristics* section ... 4
- Added *Receiving Notification of Documentation Updates* section to *Device and Documentation Support* section ... 7

Changes from Original (November 2014) to Revision A **Page**

- Improved graph setup for readability ... 4
- Added *Community Resources* ... 7

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-source voltage	V_{GS} = 0 V, I_S = 250 µA	12			V
I_{S1S2}	Source-to-source leakage current	V_{GS} = 0 V, V_{S1S2} = 9.6 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 10 V			10	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_S = 250 µA	0.75	0.95	1.25	V
$R_{S1S2(on)}$	Source-to-source on resistance	V_{GS} = 2.5 V, I_S = 5 A	14.0	17.5	23.0	mΩ
		V_{GS} = 3.8 V, I_S = 5 A	8.8	10.9	13.0	mΩ
		V_{GS} = 4.5 V, I_S = 5 A	7.9	9.9	11.9	mΩ
g_{fs}	Transconductance	V_{S1S2} = 1.2 V, I_S = 5 A		36		S
DYNAMIC CHARACTERISTICS(1)						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 6 V, f = 1 MHz		902	1170	pF
C_{oss}	Output capacitance			187	243	pF
C_{rss}	Reverse transfer capacitance			111	144	pF
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 6 V, I_S = 5 A		8.4	10.9	nC
Q_{gd}	Gate charge gate-to-drain			1.9		nC
Q_{gs}	Gate charge gate-to-source			2.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.6		nC
Q_{oss}	Output charge	V_{S1S2} = 6 V, V_{GS} = 0 V		2.9		nC
$t_{d(on)}$	Turnon delay time	V_{S1S2} = 6 V, V_{GS} = 4.5 V, I_{S1S2} = 5 A, R_G = 0 Ω		205		ns
t_r	Rise time			353		ns
$t_{d(off)}$	Turnoff delay time			711		ns
t_f	Fall time			589		ns
DIODE CHARACTERISTICS						
$V_{F(S-S)}$	Source-to-source diode forward voltage	I_{SS} = 5 A, V_{G1S1} = 0 V, V_{G2S2} = 4.5 V		0.79	1.0	V

(1) Dynamic characteristics values specified are per single FET.

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		150		°C/W
	Junction-to-ambient thermal resistance(2)		55		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

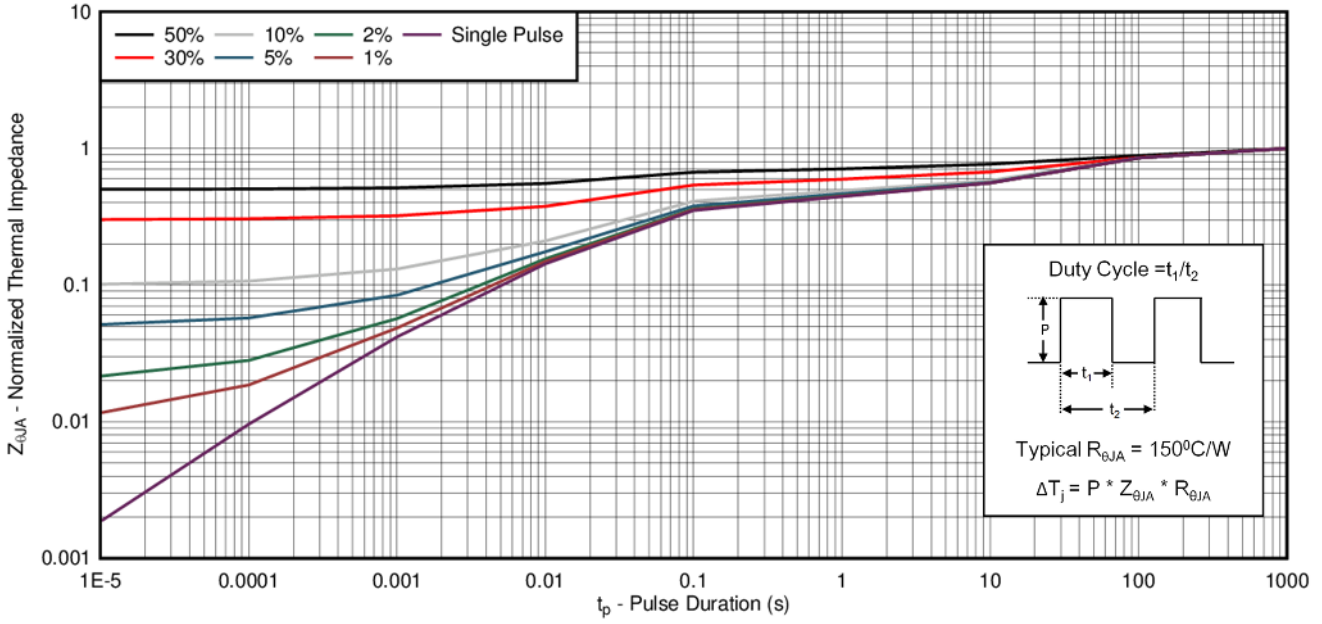


Figure 1. Transient Thermal Impedance

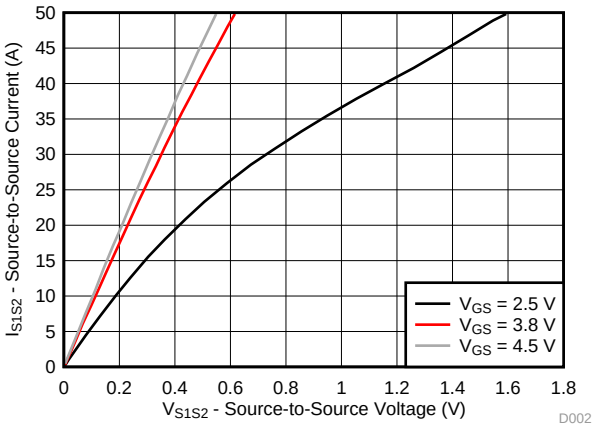


Figure 2. Saturation Characteristics

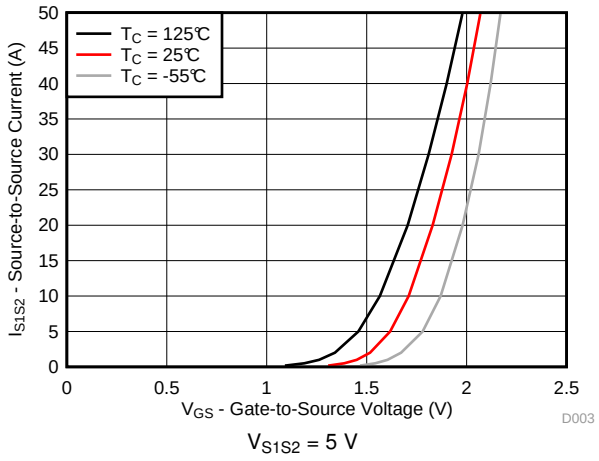


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

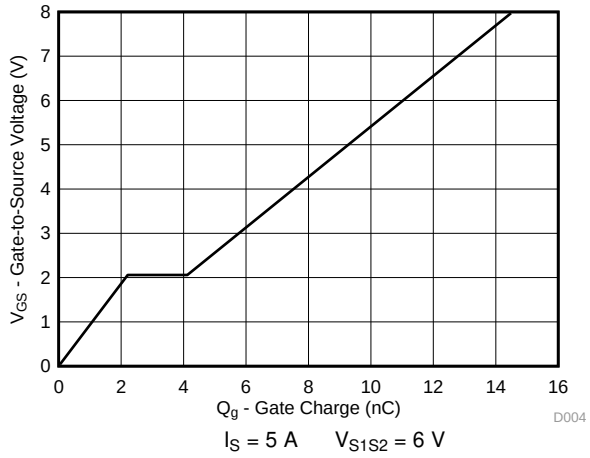


Figure 4. Gate Charge

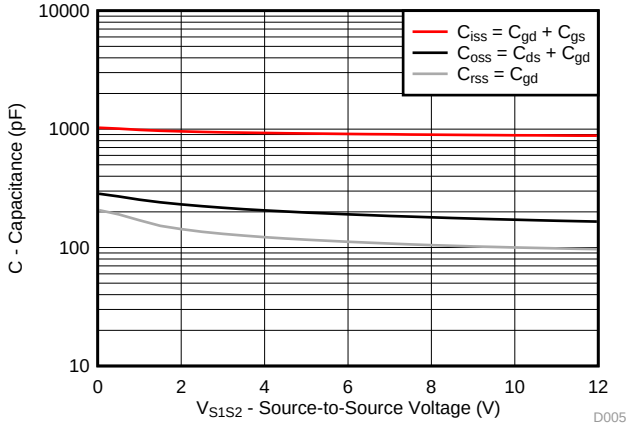


Figure 5. Capacitance

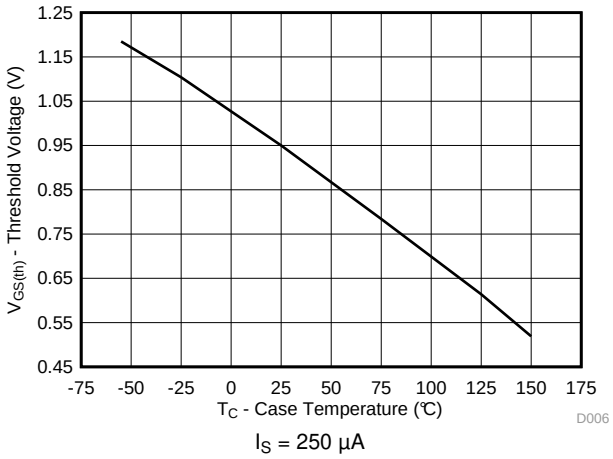


Figure 6. Threshold Voltage vs Temperature

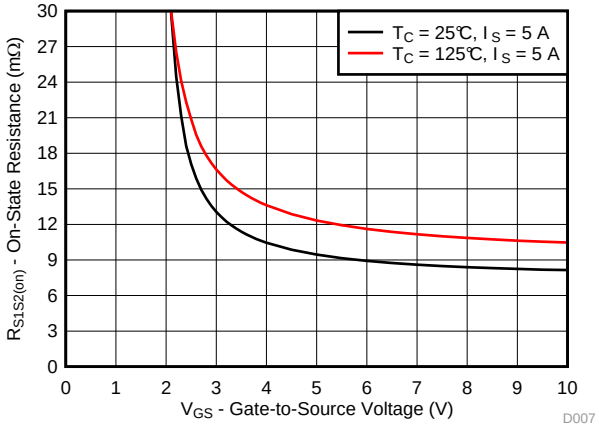


Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

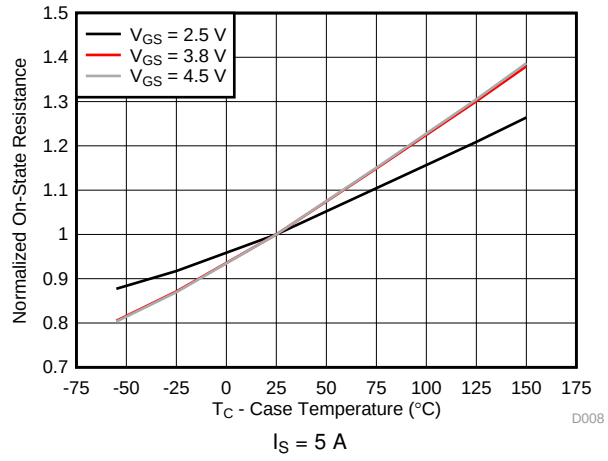


Figure 8. Normalized On-State Resistance vs Temperature

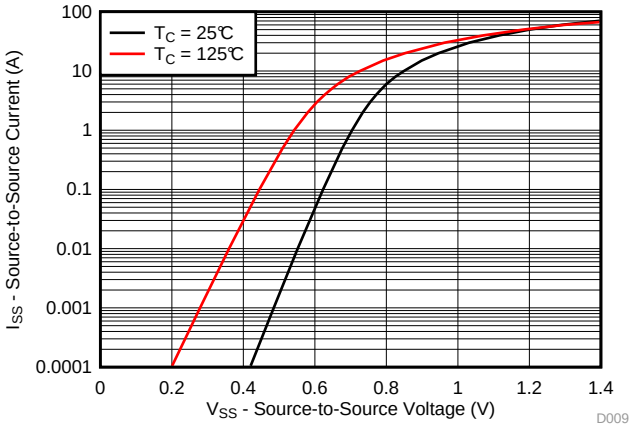


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

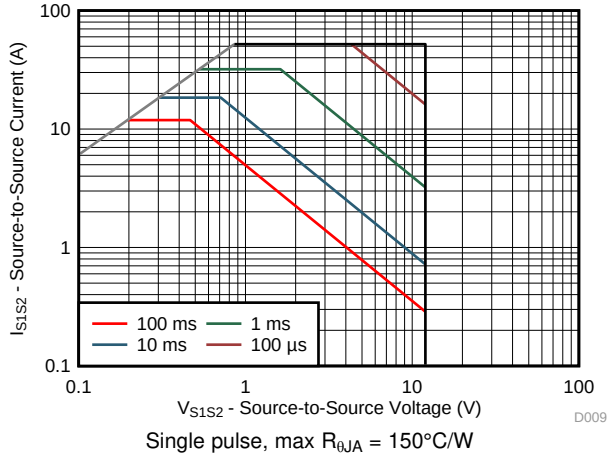


Figure 10. Maximum Safe Operating Area

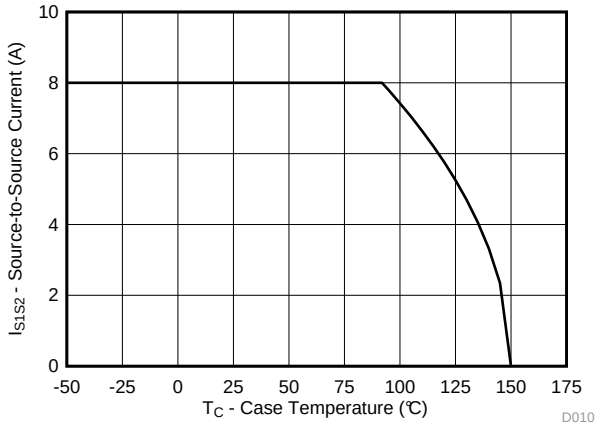


Figure 11. Maximum Source Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

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6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

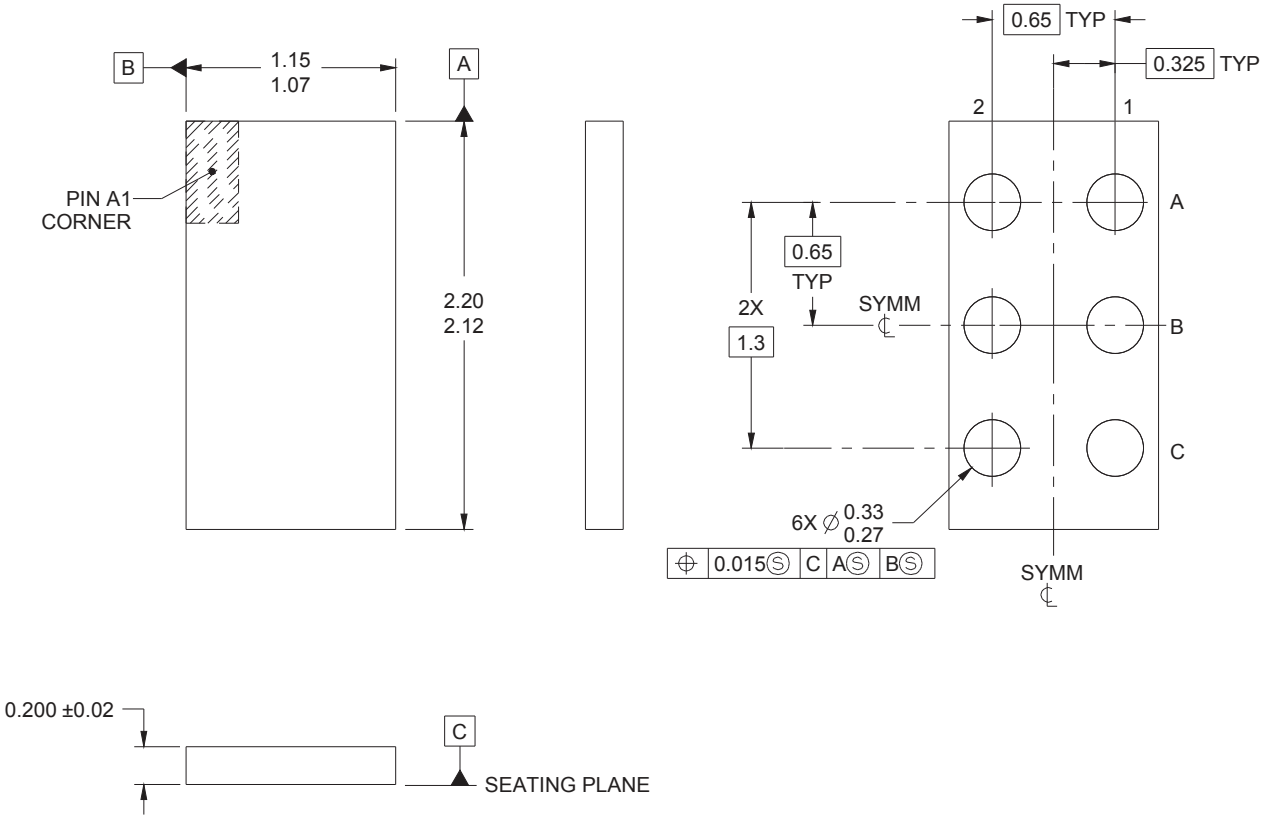
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

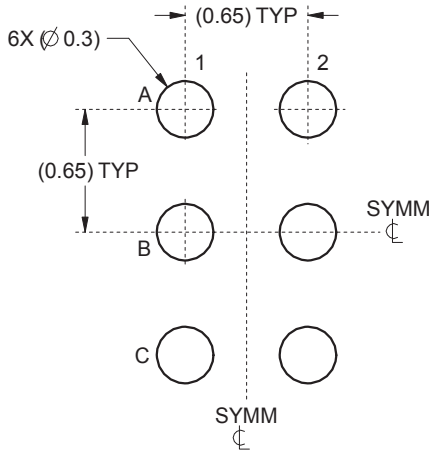
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions

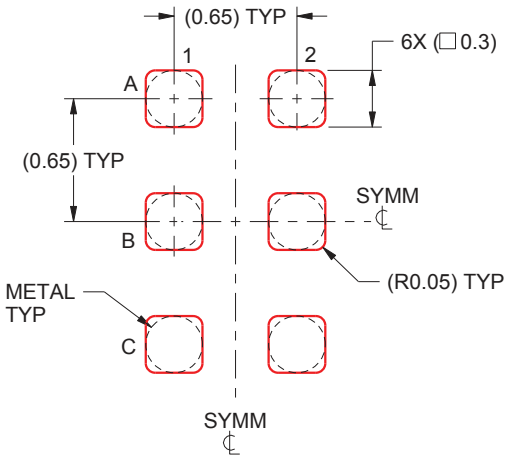


All dimensions in millimeters.

7.2 Recommended PCB Pattern



7.3 Recommended Stencil Pattern



All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD83325L	ACTIVE	PICOSTAR	YJE	6	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM		83325L	Samples
CSD83325LT	ACTIVE	PICOSTAR	YJE	6	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	83325L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

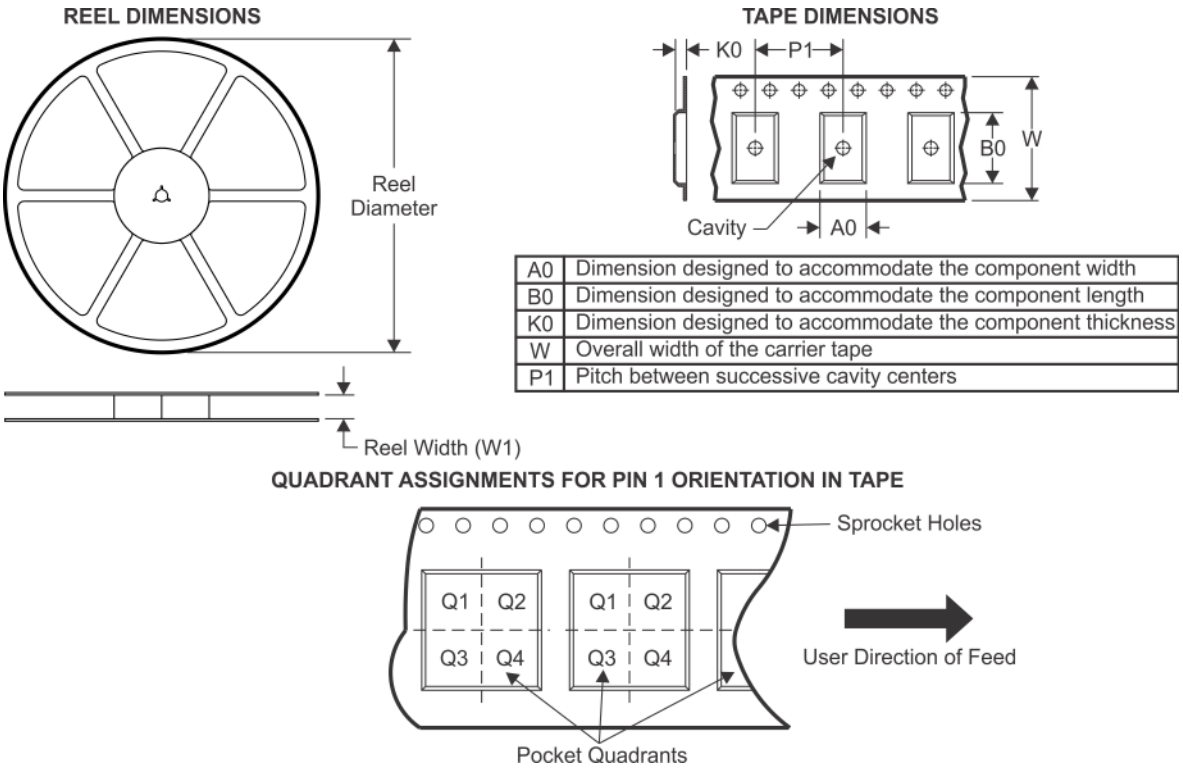
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

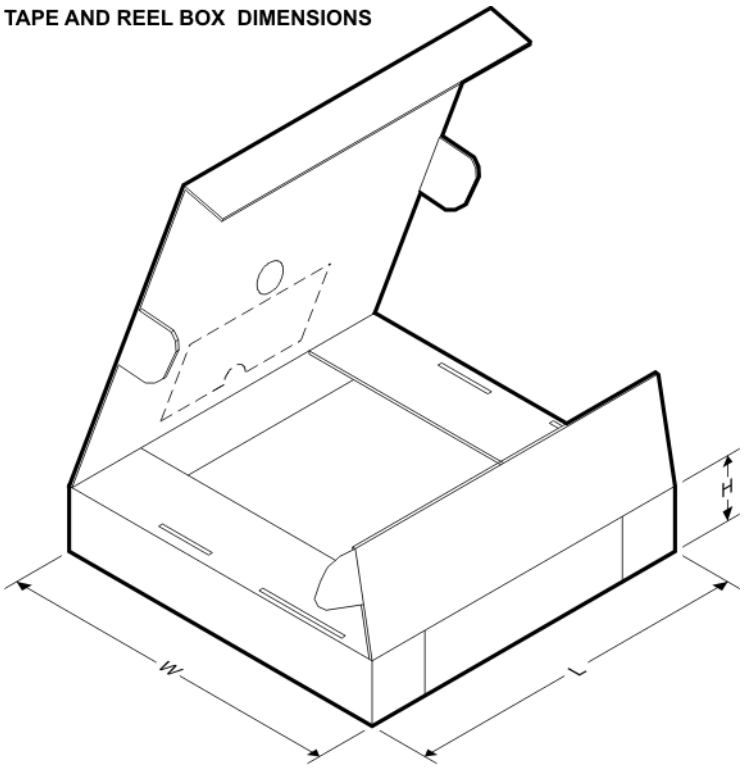


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

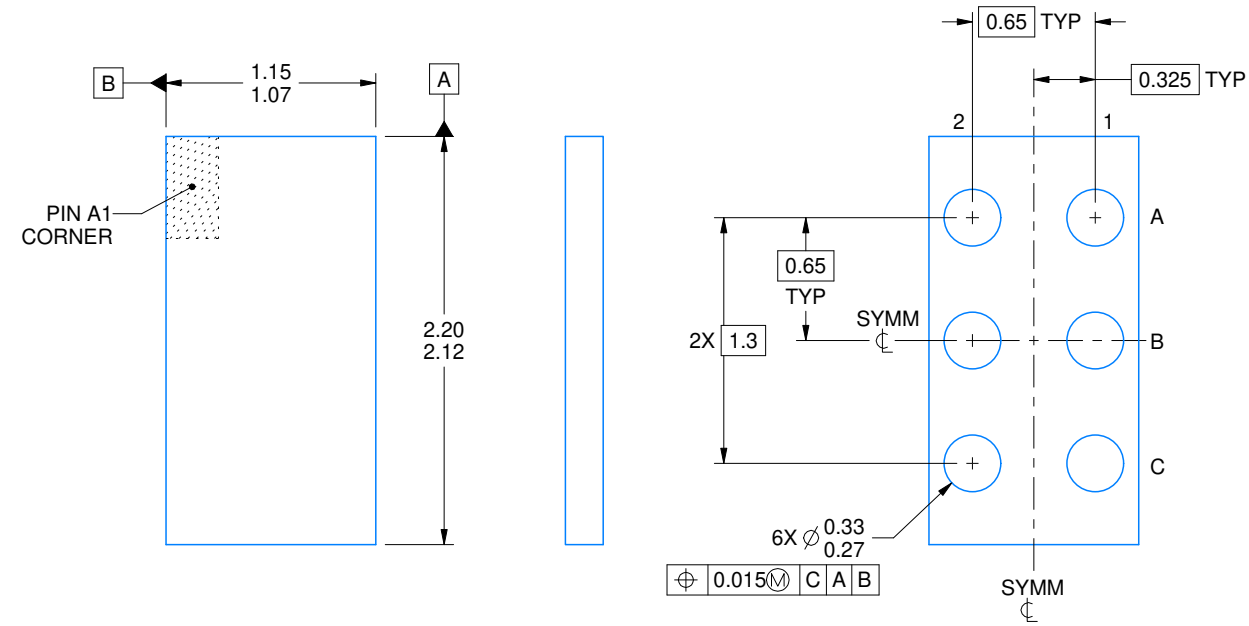
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD83325L	PICOSTAR	YJE	6	3000	178.0	8.4	1.25	2.34	0.32	4.0	8.0	Q1
CSD83325LT	PICOSTAR	YJE	6	250	178.0	8.4	1.25	2.34	0.32	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD83325L	PICOSTAR	YJE	6	3000	220.0	220.0	35.0
CSD83325LT	PICOSTAR	YJE	6	250	220.0	220.0	35.0



D: Max = 2.09 mm, Min = 2.03 mm

E: Max = 1.14 mm, Min = 1.08 mm

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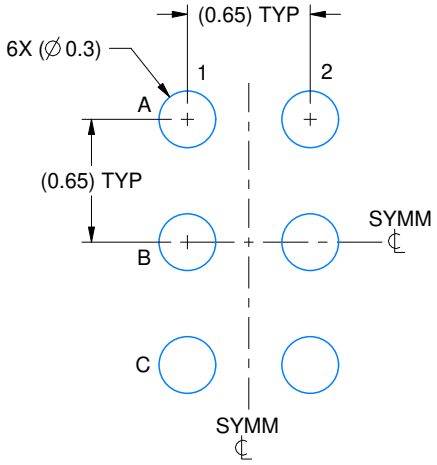
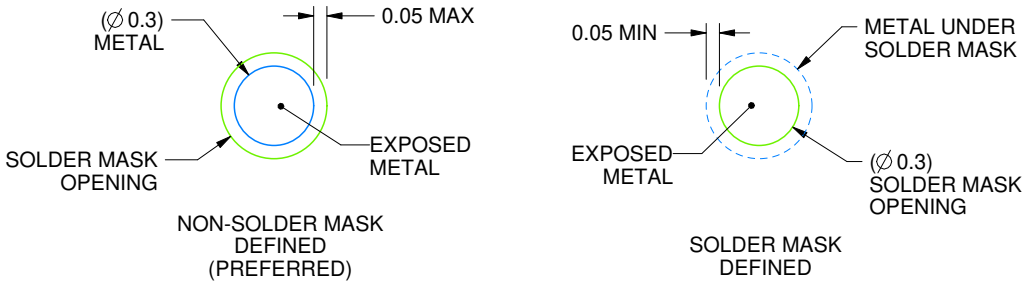
PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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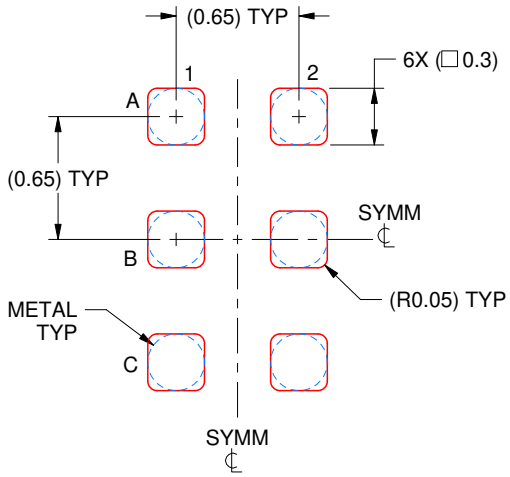
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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