GX414 Monolithic 4x1 Video Multiplexer

DATA SHEET

FEATURES

- **low differential gain: 0.03% typ. at 4.43 MHz**
- **low differential phase: 0.012 deg. typ. at 4.43 MHz**
- **low insertion loss: 0.05 dB max at 100 kHz**
- **low disabled power consumption: 5.2 mW typ.**
- **high off isolation: 110 dB at 10 MHz**
- **all hostile crosstalk @ 5 MHz, 97 dB typ.**
- **bandwidth (-3dB) with 30 pF load, 100 MHz typ.**
- **fast make-before-break switching: 200 ns typ.**
- **TTL and 5 volt CMOS compatible logic inputs**
- **low cost 14 pin DIP and16 pin SOIC packages**
- **optimised performance for NTSC, PAL and SECAM applications**

APPLICATIONS

Glitch free analog switching for...

- High quality video routing
- A/D input multiplexing
- Sample and hold circuits

* TV/ CATV/ monitor switching

AVAILABLE PACKAGING

14 pin DIP and 16 pin SOIC

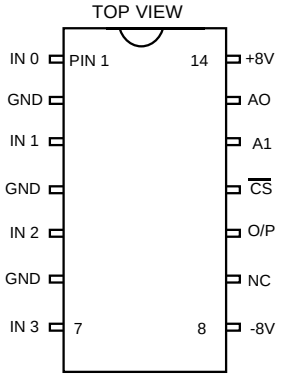
CIRCUIT DESCRIPTION

The GX414 is a high performance low cost monolithic 4x1 video multiplexer incorporating four bipolar switches with a common output, a 2 to 4 address decoder and fast chip select circuitry. The chip select input allows for multi-chip paralleled operation in routing matrix applications. The chip is selected by applying a logic 0 on the chip select input.

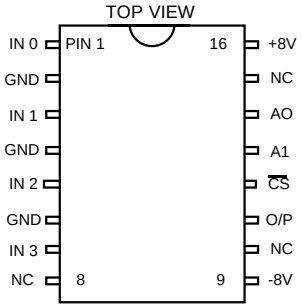
Unlike devices using MOS bilateral switching elements, these bipolar circuits represent fully buffered, unilateral transmission paths when selected. This results in extremely high output to input isolation. They also feature fast make-before-break switching action. These features eliminate such problems as switching 'glitches' and output-to-input signal feedthrough.

The GX414 operates from ±7 to ± 13.2 volt DC supplies. They are specifically designed for video signal switching which requires extremely low differential phase and gain. Logic inputs are TTL and 5 volt CMOS compatible providing address and chip select functions. When the chip is not selected, the output goes to a high impedance state.

PIN CONNECTIONS

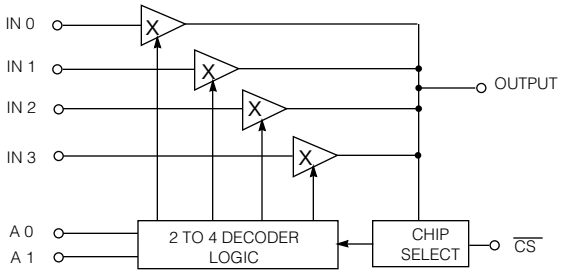


PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	±13.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70° C
Storage Temperature Range	-65°C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	-4V ≤ V_{IN} ≤ +2.4V
Analog Input Current	50µA AVG, 10 mA peak
Logic Input Voltage	-4V ≤ V_L ≤ +5.5V

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX414 – – CDB	14 Pin DIP	0° to 70° C
GX414 – – CKC	16 Pin SOIC	0° to 70° C
GX414 – – CTC	Tape 16 Pin SOIC	0° to 70° C

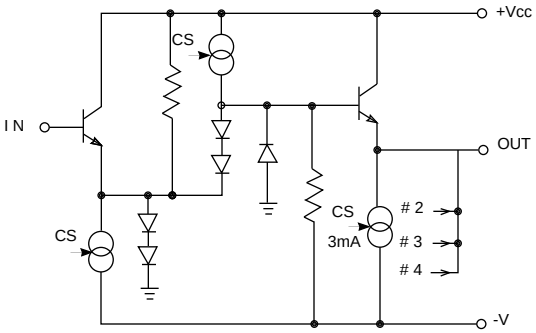


Fig.1 Crosspoint Equivalent Circuit

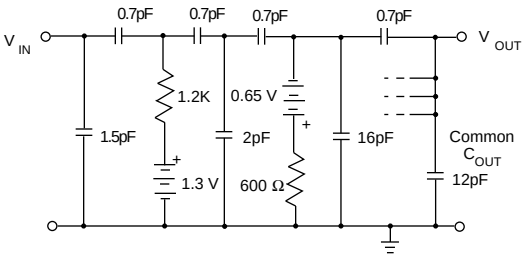


Fig. 2 Disabled Crosspoint Equivalent Circuit

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, C_L = 30 pF, R_L = 10kΩ unless otherwise shown.)

				GX414			
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	±V_S		7	8	13.2	V
	Supply current	I+	Chip selected ($\overline{CS}$=0)	-	11	14	mA
			Chip not selected ($\overline{CS}$=1)	-	0.4	0.58	mA
		I-	Chip selected ($\overline{CS}$=0)	-	10.5	14	mA
			Chip not selected ($\overline{CS}$=1)	-	0.25	0.38	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs.	- -	+2 -1.2	- -	V
	Analog Input Bias Current	I_{BIAS}		-	22		µA
	Output Offset Voltage	V_{OS}	T_A = 25°C, 75 Ω resistor on each input to gnd	-2	5	12	mV
	Output Offset Voltage Drift	Δ V_{OS}/ΔT		-	+50	+200	µV/°C

ELECTRICAL CHARACTERISTICS continued

(V_S = ±8V DC, 0°C < T_A < 70°C,C_L = 30pF, R_L = 10kΩ unless otherwise shown.)

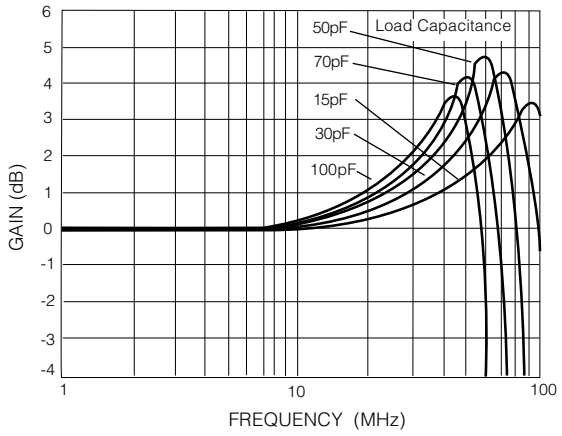
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	Crosspoint Selection Turn-On Time	t_{ADR-ON}	Control input to appearance of signal at the output.	130	200	270	ns
	Crosspoint Selection Turn-Off Time	$t_{ADR-OFF}$	Control input to disappearance of signal at output.	390	600	800	ns
	Chip Selection Turn-On Time	t_{CS-ON}	Control input to appearance of signal at output.	200	300	400	ns
	Chip Selection Turn-Off Time	t_{CS-OFF}	Control input to disappearance of signal at output.	460	700	940	ns
LOGIC	Logic Input Thresholds	V_{IH}	1	2.0	-	-	V
		V_{IL}	0	-	-	1.1	V
	Address Input Bias Current	$I_{BIAS(ADR)}$	Chip selected A0, A1 = 1	-	-	5.0	µA
			Chip selected A0, A1 = 0	-	-	0.1	nA
	Chip Select Bias Current	$I_{BIAS(CS)}$	$\overline{CS}$ = 1	-	-	1.0	nA
			$\overline{CS}$ = 0	-	-	30	µA
	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	dB
	Bandwidth (-3 dB)	B.W.		90	100	-	MHz
	Gain Spread at 8 MHz			-	-	±0.1	dB
	Input to Output Signal Delay	Δt_P	T_A = 25°C, R_S = 75Ω f = 3.579545 MHz	-	-	±0.3 5	deg.
	Matching (chip to chip)		0°C < T_A < 70°C, R_S as above, f as above.	-	-	±0.7	deg.
	Input Resistance	R_{IN}	Chip selected ($\overline{CS}$ = 0)	900	-	-	kΩ
DYNAMIC	Input Capacitance	C_{IN}	Chip selected ($\overline{CS}$ = 0)	-	2.0	-	pF
			Chip not selected ($\overline{CS}$ = 1)	-	2.4	-	pF
	Output Resistance	R_{OUT}	Chip selected ($\overline{CS}$ = 0)	-	14	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected ($\overline{CS}$ = 1)	-	15	-	pF
	Differential Gain	dg	at 3.579545 MHz,	-	0.03	0.05	%
	Differential Phase	dp	V_{IN} = 40 IRE, (Fig. 7)	-	0.012	0.025	deg.
	All Hostile Crosstalk (see graph)	$X_{TALK (AH)}$	Sweep on 3 inputs 1V p-p 4th input has 10 Ω resistor gnd. f = 5 MHz (Fig. 6)	94	97	-	dB
	Chip Disabled Crosstalk (see graph)	$X_{TALK(CD)}$	f = 10 MHz (Fig. 5)	100	110	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	84	120	-	V/µs
		-SR		70	100	-	V/µs

CAUTION

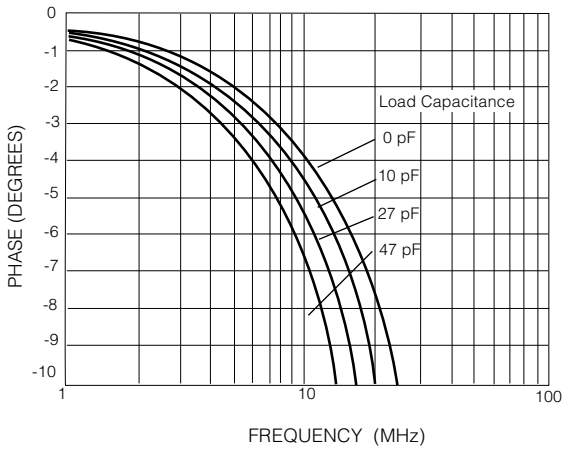
ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE DEVICES EXCEPT AT A STATIC-FREE WORKSTATION

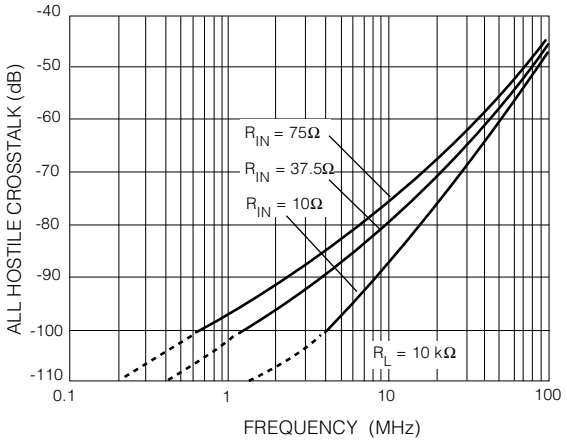
TYPICAL PERFORMANCE CURVES OF THE GX414



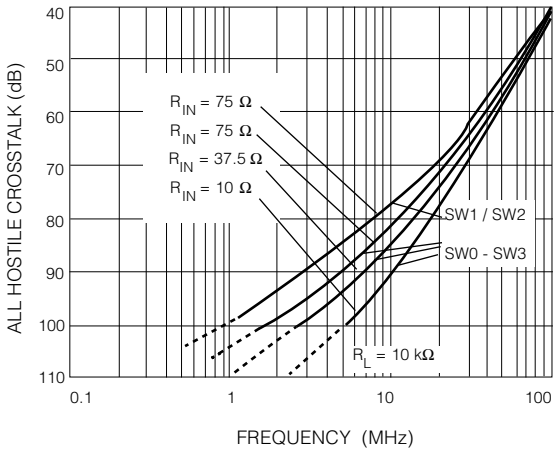
Gain vs Frequency



Phase vs Frequency

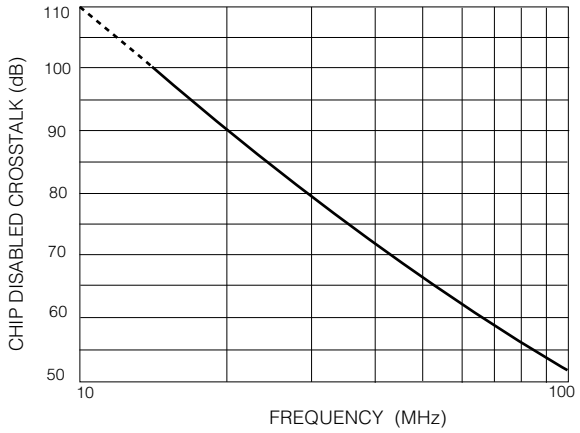


All Hostile Crosstalk (14 pin DIP)

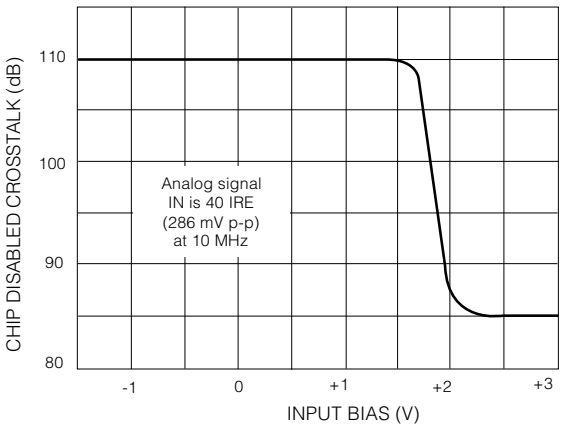


All Hostile Crosstalk (16 pin SOIC)

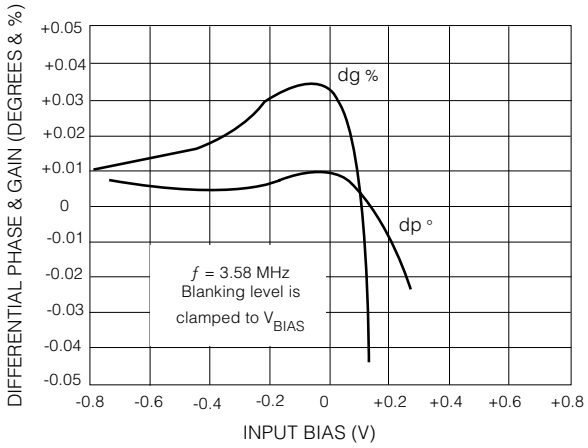
For all graphs, $V_S = \pm 8$ V DC and $T_A = 25°C$. The curves shown above represent typical batch sampled results.



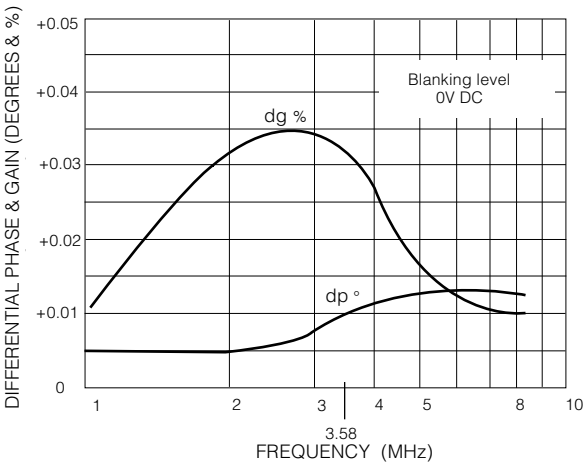
Chip Disabled Crosstalk vs Frequency



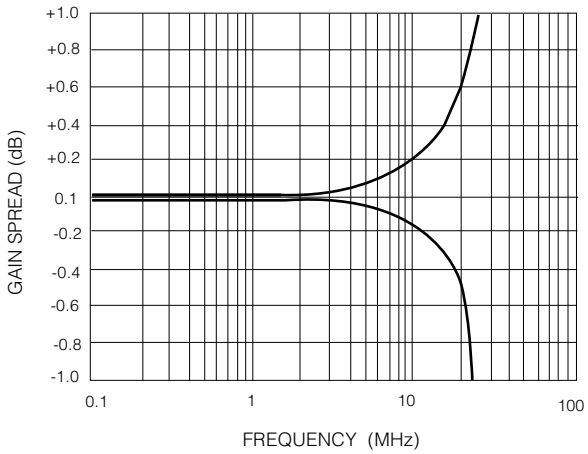
Chip Disabled Crosstalk vs Input Bias (V)



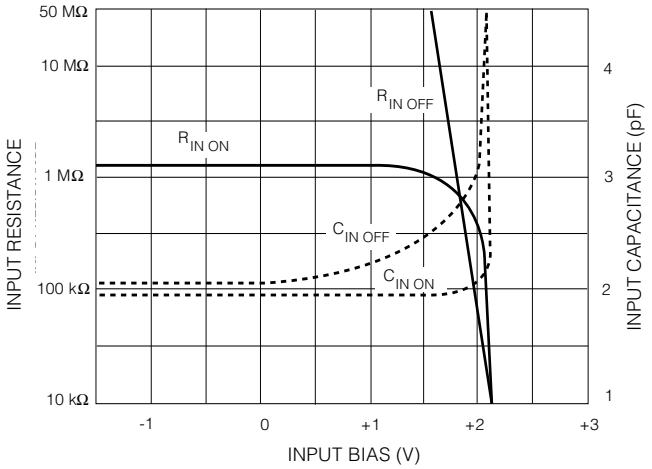
dg/dp vs Input Bias



dg/dp vs Frequency



Normalized Gain Spread C_L = 30pF



Input Impedance

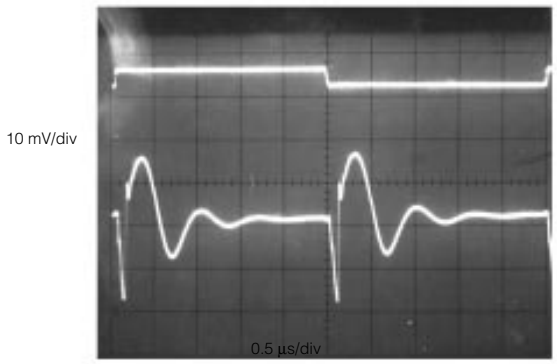


Fig.3 Switching Transient (crosspoint to crosspoint)

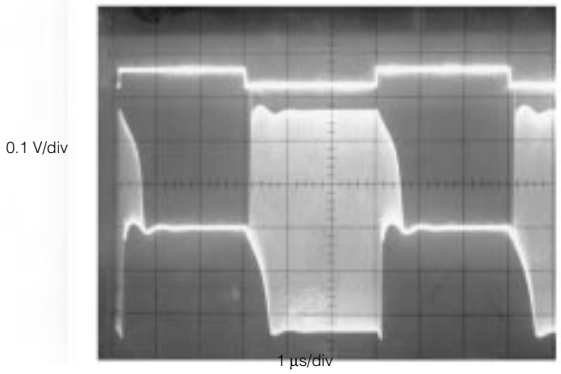


Fig. 4 Switching Envelope (crosspoint to crosspoint)

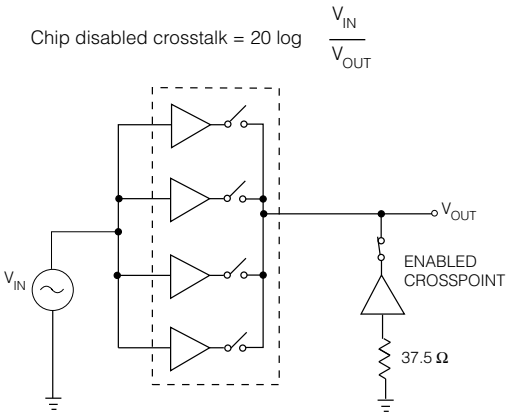


Fig. 5 Chip Disabled Crosstalk Test Circuit

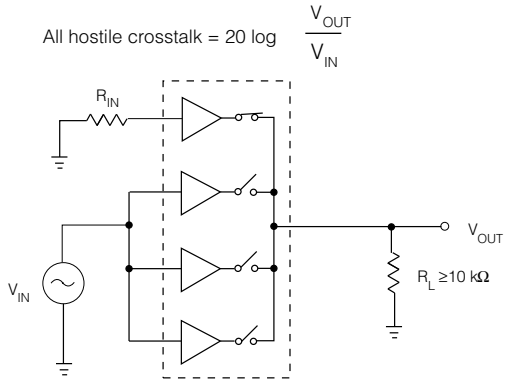


Fig. 6 All Hostile Crosstalk Test Circuit

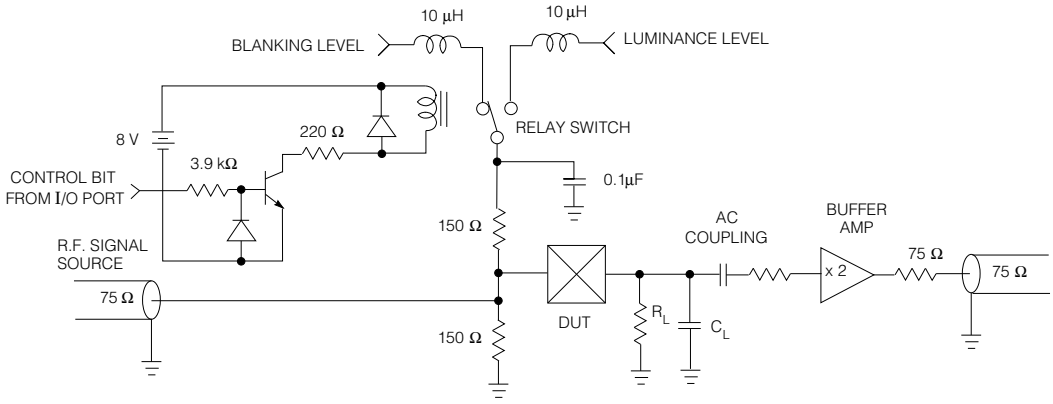


Fig. 7 Differential Phase and Gain Test Circuit

DIFFERENTIAL GAIN AND PHASE TEST CIRCUIT

The test circuit of Figure 7 allows two DC bias levels, set by the user, to be superimposed on a high frequency signal source. A computer controlled relay selects either the preset blanking or luminance level. One measurement is taken at each level and the change in gain or phase is calculated. This procedure is repeated one hundred times to provide a reasonably large sample.

The results are averaged to reduce the standard deviation and therefore improve the accuracy of the measurement.

The output from the device under test is AC coupled to a buffer amplifier which allows the buffer to operate at a constant luminance level so that it does not contribute any dg or dp to the measurement.

OPTIMISING THE PERFORMANCE OF THE GX414

1. Power Supply Considerations

Table 1 shows the effect on differential gain (dg) and differential phase (dp) of various power supply voltages that may be used. A nominal supply voltage of ±8 volts result in parameter values as shown in the top row of the table. By using other power supply voltage combinations, improvements to these parameters are possible at the sacrifice of increased chip power dissipation. Maximum degradation of the differential gain and phase occurs for the last combination of +12 , -7 volts along with an increase in power dissipation; these voltages are not recommended.

Supply Voltage	Differential Gain % (Typical)	Differential Phase degrees (Typical)
±8	0.030	0.012
+8/ -12	0.010	0.007
±12	0.010	0.007
+12/ -7	0.084	0.080

Table 2 shows the general characteristic variations of the GX414 when different combinations of power supply voltages are used. These changes are relative to a circuit using ± 8 volts Vcc.

Supply Voltage	Characteristic Changes
± 7	- lower logic thresholds - max logic I/P (≈ 4.5V) - loss of off isolation (≈20 dB) - poorer dg and dp
+8/ -12	- slight increase in negative supply current - slight decrease in offset - very similar frequency response - better dg and dp
±12	- increase in supply current (10%) - increase in offset (≈ 2-4 mV) - very similar frequency response - better dg and dp
+12/ -7	- loss in off isolation (≈20 dB) - poorer dg and dp

The GX414 does not require input DC biasing to optimise dg or dp nor does it need switching transient suppression at the output. Furthermore, both the analog signal and logic circuits within the chip use one common power supply, making power supply configurations relatively simple and straightforward. Several of the input characteristic graphs on pages 4-5 show that for best operation, the input bias should be 0 volts. The switching transient photographs on page 6 show how small the actual transients are and clearly show the make-before-break action of the GX414 video multiplexer switch.

2. Frequency Response Considerations

At frequencies higher than1 MHz, the output impedance of the multiplexer switches can be modelled as a voltage generator having a series resistance and a series inductance. The gain/frequency characteristics exhibit peaking above 10 MHz due to the internal equivalent series inductance combined with any load capacitance. The peaking can be reduced by adding external series resistance to the output of the multiplexer. Figure 8 shows the effect of adding a 33Ω resistor to the output of a circuit having 47 pF effective load capacitance. This amount of load capacitance represents the equivalent of a 16 x1 multiplexer configuration using four ICs. Even though the frequency response has been flattened, the differential phase and gain have now changed as shown in Figure 9.

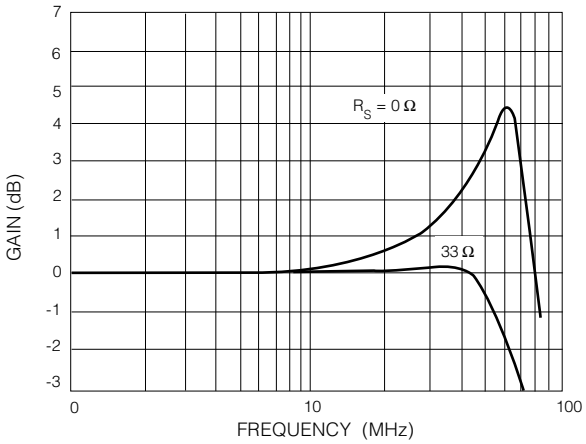


Fig. 8 Gain vs Frequency

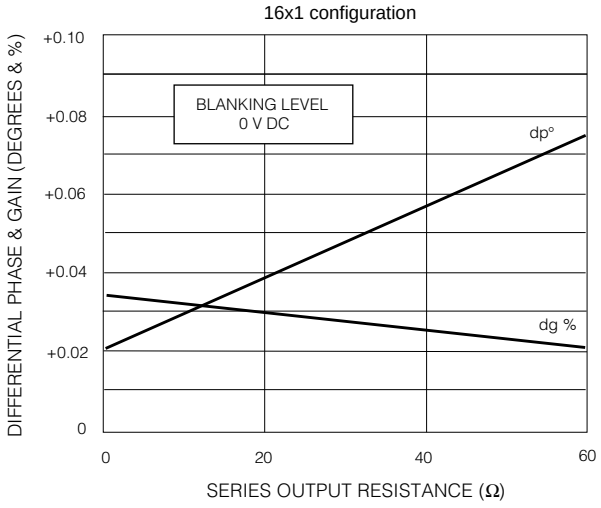


Fig. 9 Phase and Gain vs Resistance

3. Load Resistance Considerations

The GX414 multiplexer switch is optimised for load resistances equal to or greater than 3 kΩ. Figure 10 shows the effect on the differential gain and phase when the load resistance is varied from 100 Ω to 100 kΩ.

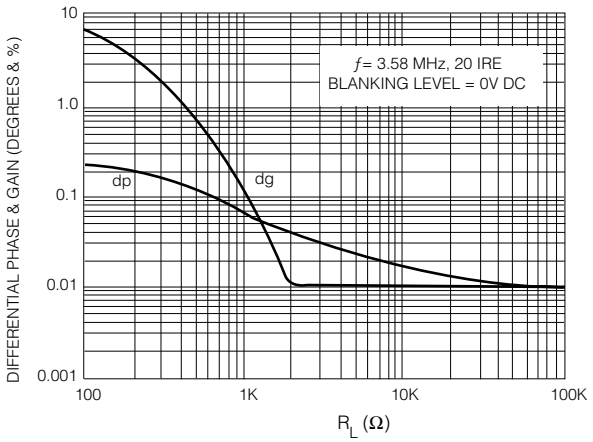


Fig. 10 dg/dp vs R_L

The negative slew rate is dependant upon the output current and load capacitance as shown below.

$$-SR = \frac{I + 3\,mA}{C_L} \qquad I \leq 8\,mA$$

The current I is determined from the following equation:

$$I = \frac{-V_{EE}}{R} \qquad R \geq 1\,k\Omega$$

It is possible to increase the negative slew rate (-S.R.) and thus the large signal bandwidth, by adding a resistance from the output to - V_{EE}. This resistor increases the output current above the 3 mA provided by the internal current generator and increases the negative slew rate. The additional slew rate improving resistance must not be less than 1kΩ in order to prevent excessive currents in the output of the device. An adverse effect of utilising this negative slew rate improving resistor, is the increase in differential phase from typically 0.009° to 0.014°. Under these same conditions, the differential gain drops from typically 0.033 % to 0.021 %.

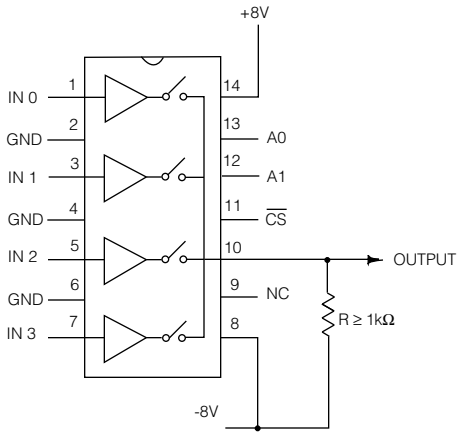


Fig.11 Negative Slew Rate (-SR) Improvement

4. Multi-chip Considerations

Whenever multi-chip bus systems are to be used, the total input and output capacitance must be carefully considered. The input capacitance of an enabled crosspoint (chip selected), is typically only 2 pF and increases slightly to 2.4 pF when the chip is disabled. The total output capacitance when the chip is disabled is approximately 15 pF per chip.

Usually the GX414 multiplexer switch is used in a matrix configuration of (n x 1) crosspoints perhaps combined in an (n x m) total routing matrix. This means for example, that four ICs produce a 16 x 1 configuration and have a total output capacitance of 4 x15 pF or 60 pF if all four chips are disabled. For any one enabled crosspoint, the effective load capacitance will be 3 x15 pF or 45 pF.

In a multi-input/multi-output matrix, it is important to consider the total input bus capacitance. The higher the bus capacitance and the more it varies from the ON to OFF condition, the more difficult it is to maintain a wide frequency response and constant drive from the input buffer. A 16 x 16 matrix using 64 ICs (16 x 4), would have a total input bus capacitance of 16 x 2.4 pF or 40 pF.

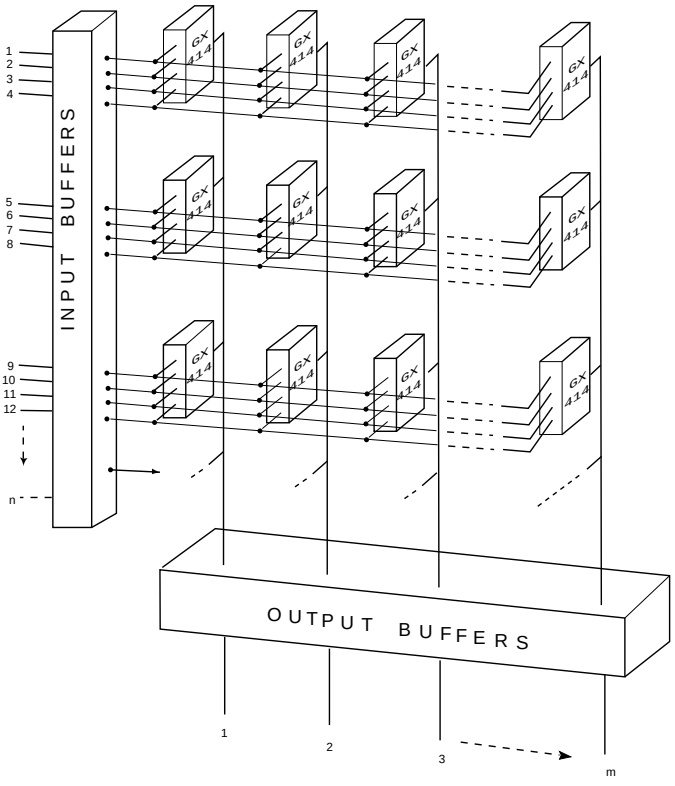


Fig.12 Multi-chip Connections

APPLICATIONS INFORMATION

The GX414 video switch is a very high performance, wideband circuit requiring careful external circuit design. Good power supply regulation and decoupling are necessary to achieve optimum results. The circuit designer must use proper lead dress, component placement and PCB layout as in any high frequency circuit.

Functionally, the video switches are non-inverting, unity gain bipolar switches with buffered inputs requiring DC coupling and 75Ω line terminating resistors when directly driven from 75Ω cable. The output must be buffered to drive 75Ω lines. This is usually accomplished with the addition of an operational amplifier/ buffer which also allows adjustments to be made to the gain, offset and frequency response of the overall circuit.

A typical video routing application is shown in Figure 13. Four ICs are used in a 16 x 1 multiplexer switching circuit.

An external address decoder is shown which generates the 16 address and chip enable codes from a binary number. The address inputs to each chip are active high while the chip select inputs are active low. Depending on the application and speed of the logic family used, latches may be required for synchronization where timing and delays are critical. Since the individual crosspoint switching circuits are unidirectional bipolar elements, low crosstalk and high isolation are inherent. The make-before-break switching characteristics of the GX414 means virtually 'glitch' free switching.

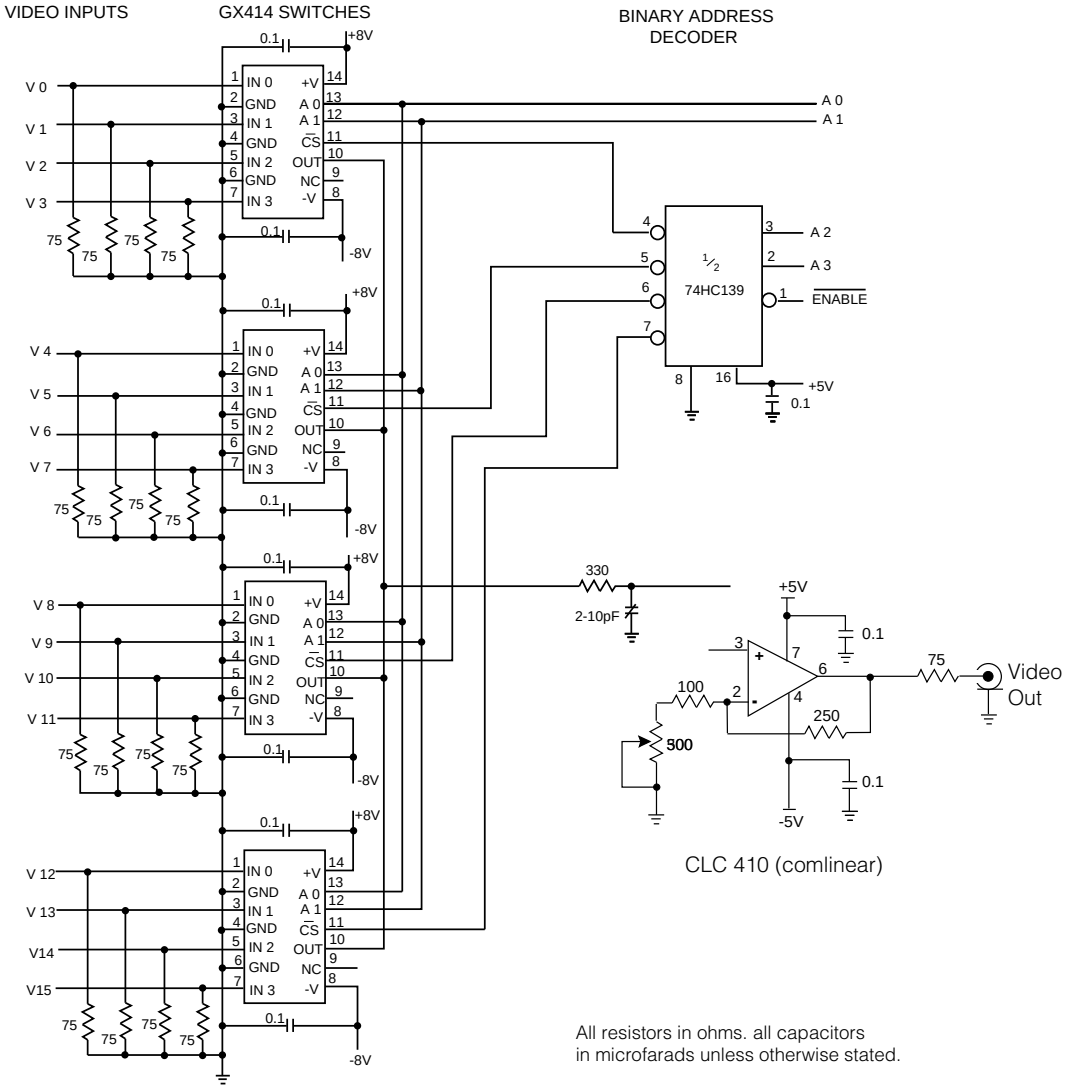


Fig.13 16 x 1 Video Multiplexer Circuit

REVISION NOTES
Layout changes