MMDF1N05E, MVDF1N05E

Power MOSFET
2 A, 50 V, N−Channel SO−8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain−to−source diode has a low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc−dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

Features

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive − Can Be Driven by Logic ICs
- Miniature SO−8 Surface Mount Package − Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO−8 Package Provided
- I_{DSS} Specified at Elevated Temperature
- This is a Pb−Free Device
- MVDF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DS}	50	V
Gate−to−Source Voltage − Continuous	V_{GS}	± 20	V
Drain Current − Continuous − Pulsed	I_D I_{DM}	2.0 10	A
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, I_L = 2 Apk)	E_{AS}	300	mJ
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Total Power Dissipation @ T_A = 25°C	P_D	2.0	W
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	62.5	°C/W
Maximum Temperature for Soldering, Time in Solder Bath	T_L	260 10	°C Sec

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

ON Semiconductor®

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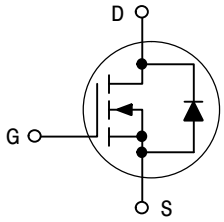
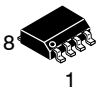
2 AMPERE, 50 VOLTS
$R_{DS(on)}$ = 300 mΩ

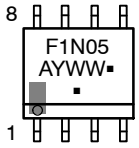
N−Channel



MARKING DIAGRAM



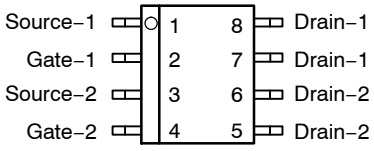
SO−8
CASE 751
STYLE 11



F1N05 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
MMDF1N05ER2G	SO−8 (Pb−Free)	2,500/Tape & Reel
MVDF1N05ER2G	SO−8 (Pb−Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	50	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)		I_{DSS}	–	–	2	μAdc
Gate−Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	–	3.0	Vdc
Drain−to−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 0.6 Adc)		$R_{DS(on)}$ $R_{DS(on)}$	– –	– –	0.30 0.50	Ω
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{FS}	–	1.5	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	330	–	pF
Output Capacitance		C_{oss}	–	160	–	
Reverse Transfer Capacitance		C_{rss}	–	50	–	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = 10 V, I_D = 1.5 A, R_L = 10 Ω, V_G = 10 V, R_G = 50 Ω)	$t_{d(on)}$	–	–	20	ns
Rise Time		t_r	–	–	30	
Turn−Off Delay Time		$t_{d(off)}$	–	–	40	
Fall Time		t_f	–	–	25	
Total Gate Charge	(V_{DS} = 10 V, I_D = 1.5 A, V_{GS} = 10 V)	Q_g	–	12.5	–	nC
Gate−Source Charge		Q_{gs}	–	1.9	–	
Gate−Drain Charge		Q_{gd}	–	3.0	–	
SOURCE−DRAIN DIODE CHARACTERISTICS (T_C = 25°C)						
Forward Voltage (Note 2)	(I_S = 1.5 A, V_{GS} = 0 V) (dI_S/dt = 100 A/μs)	V_{SD}	–	–	1.6	V
Reverse Recovery Time		t_{rr}	–	45	–	ns

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

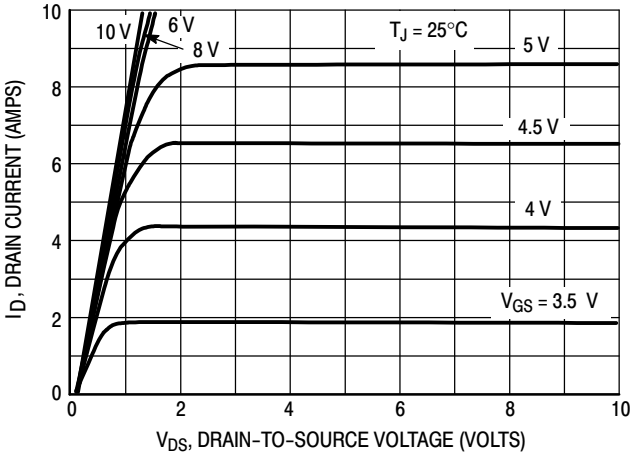


Figure 1. On−Region Characteristics

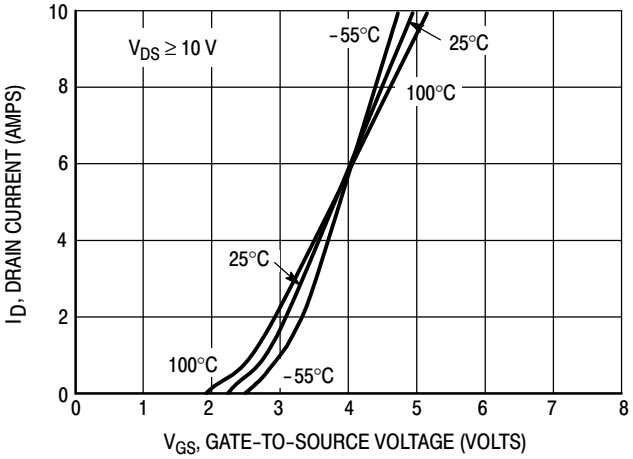


Figure 2. Transfer Characteristics

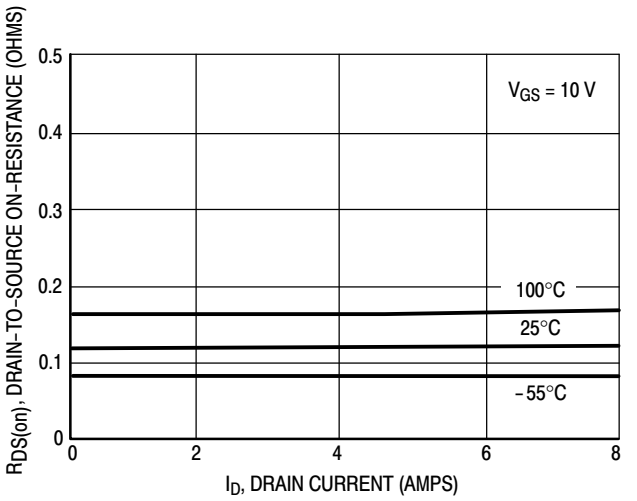


Figure 3. On−Resistance versus Drain Current

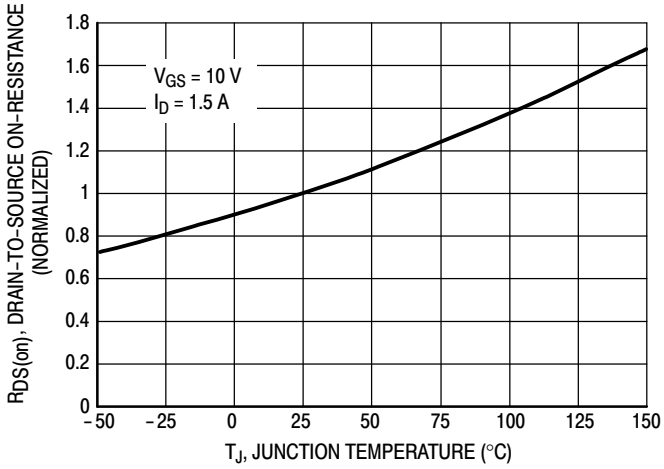


Figure 4. On−Resistance Variation with Temperature

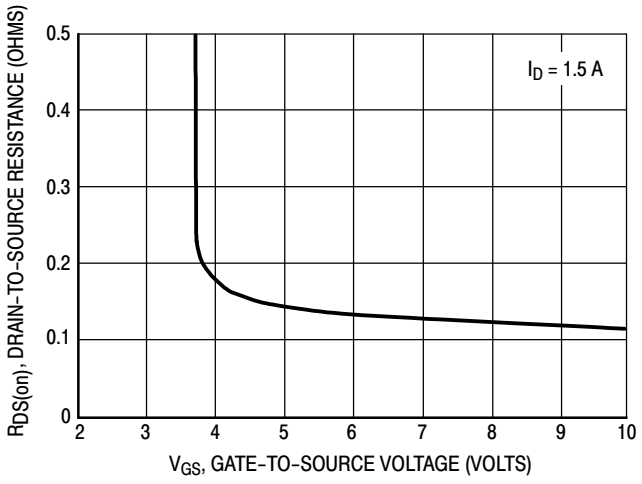


Figure 5. On Resistance versus Gate−To−Source Voltage

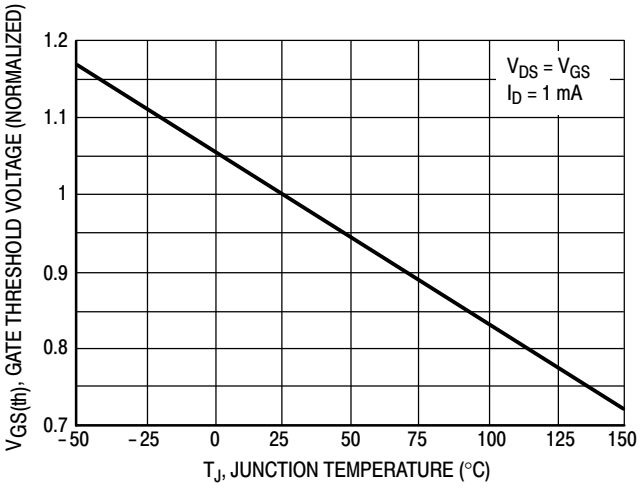


Figure 6. Gate Threshold Voltage Variation with Temperature

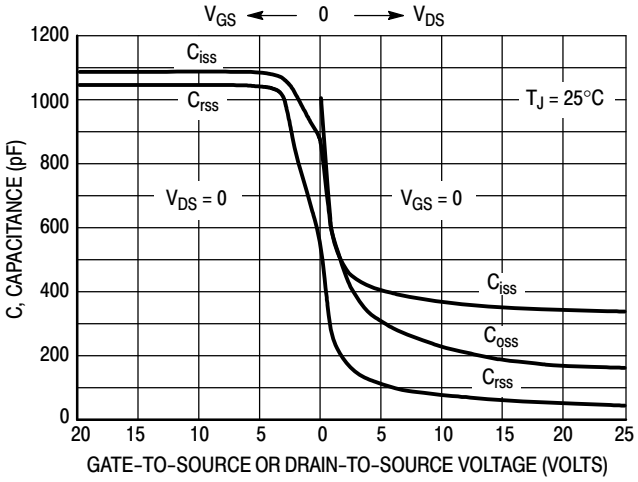


Figure 7. Capacitance Variation

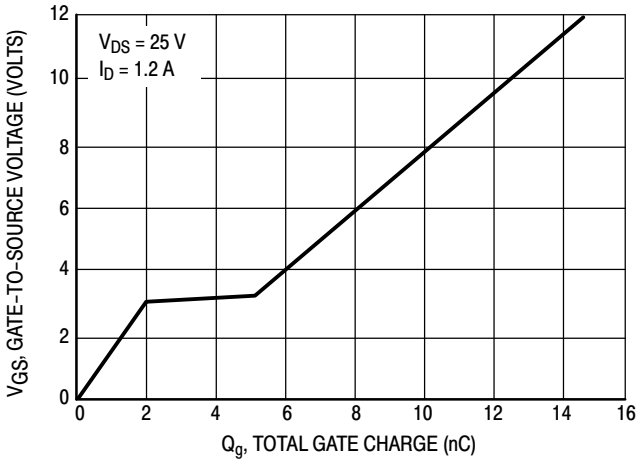


Figure 8. Gate Charge versus Gate−To−Source Voltage

SAFE OPERATING AREA INFORMATION

Forward Biased Safe Operating Area

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance − General Data and Its Use” provides detailed instructions.

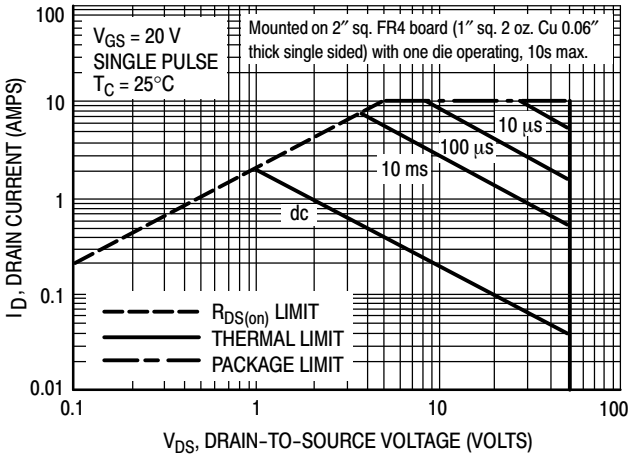


Figure 9. Maximum Rated Forward Biased Safe Operating Area

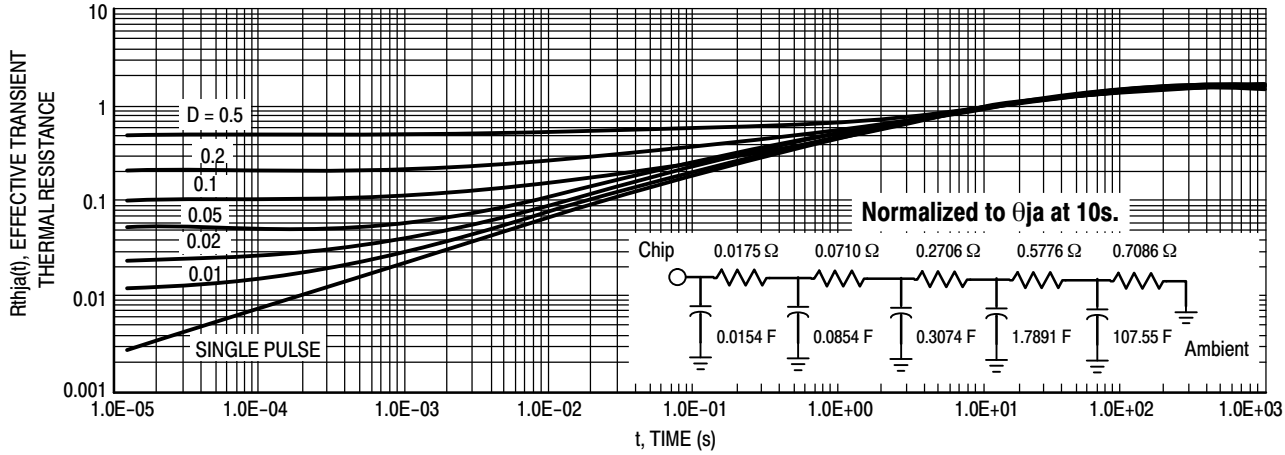


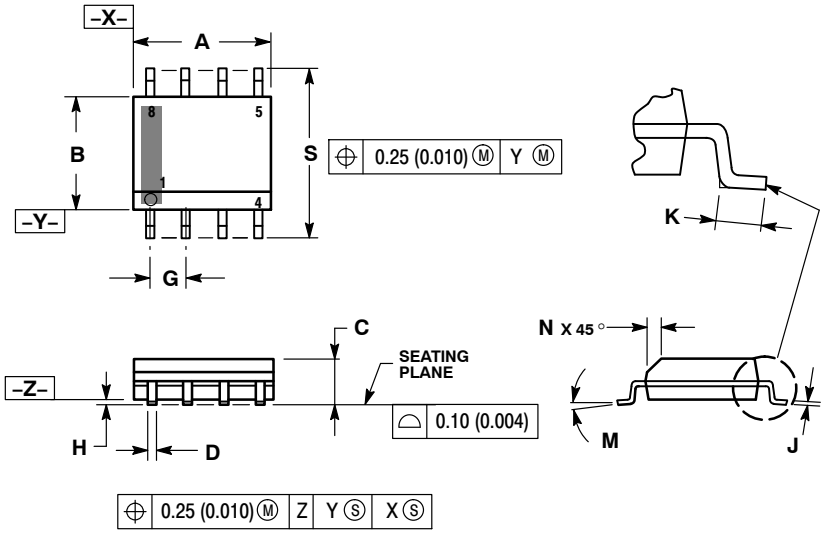
Figure 10. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

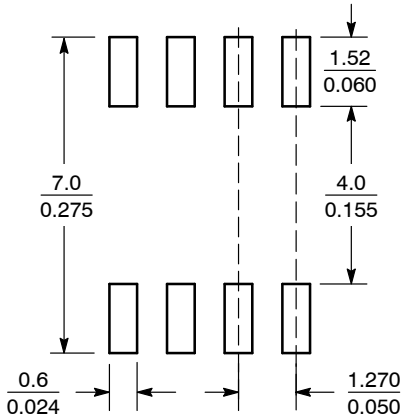
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

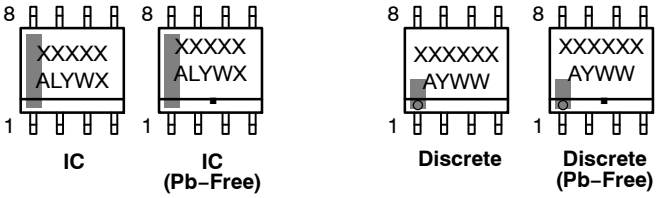
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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