Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ML9272

40-Bit Vacuum Fluorescent Display Tube Grid/Anode Driver

GENERAL DESCRIPTION

The ML9272 is a monolithic IC designed for directly driving the grids and anodes of the vacuum fluorescent display tube. The device contains a 40-bit bidirectional shift register, a 40-bit latch circuit, and 40-output circuit on a single chip.

Display data is serially stored in the shift register at the rising edge of a CLOCK pulse.

Setting the $\overline{CL}$ pin low allows all the driver outputs to be driven low, which makes it possible to set the display blanking.

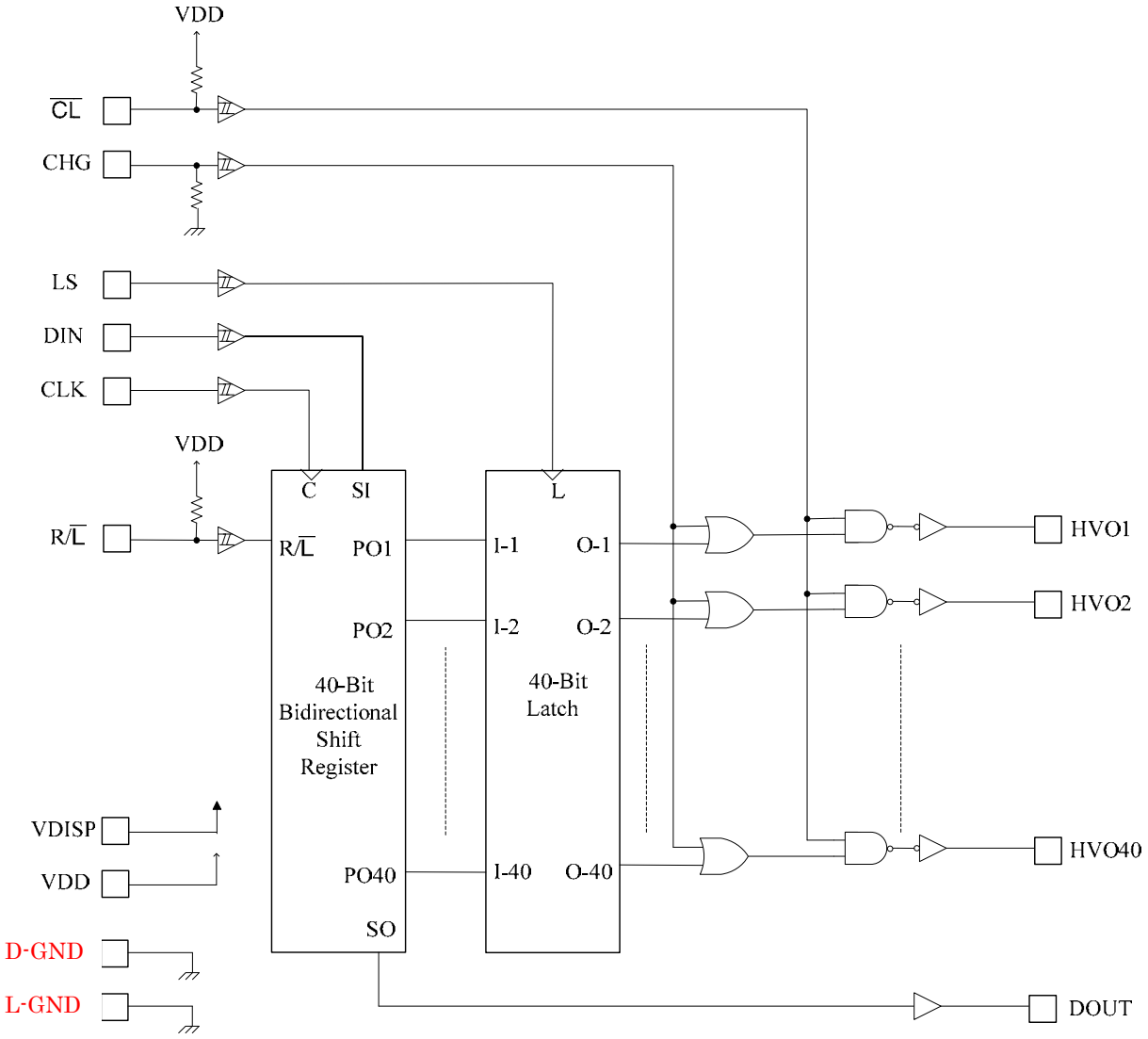
Also, setting both of the $\overline{CL}$ and CHG pins high allows all the driver outputs to be driven high, which provides the easy testing of all lights after final assembly of a VFD tube panel.

The ML9272 is compatible with the MSC1162A.

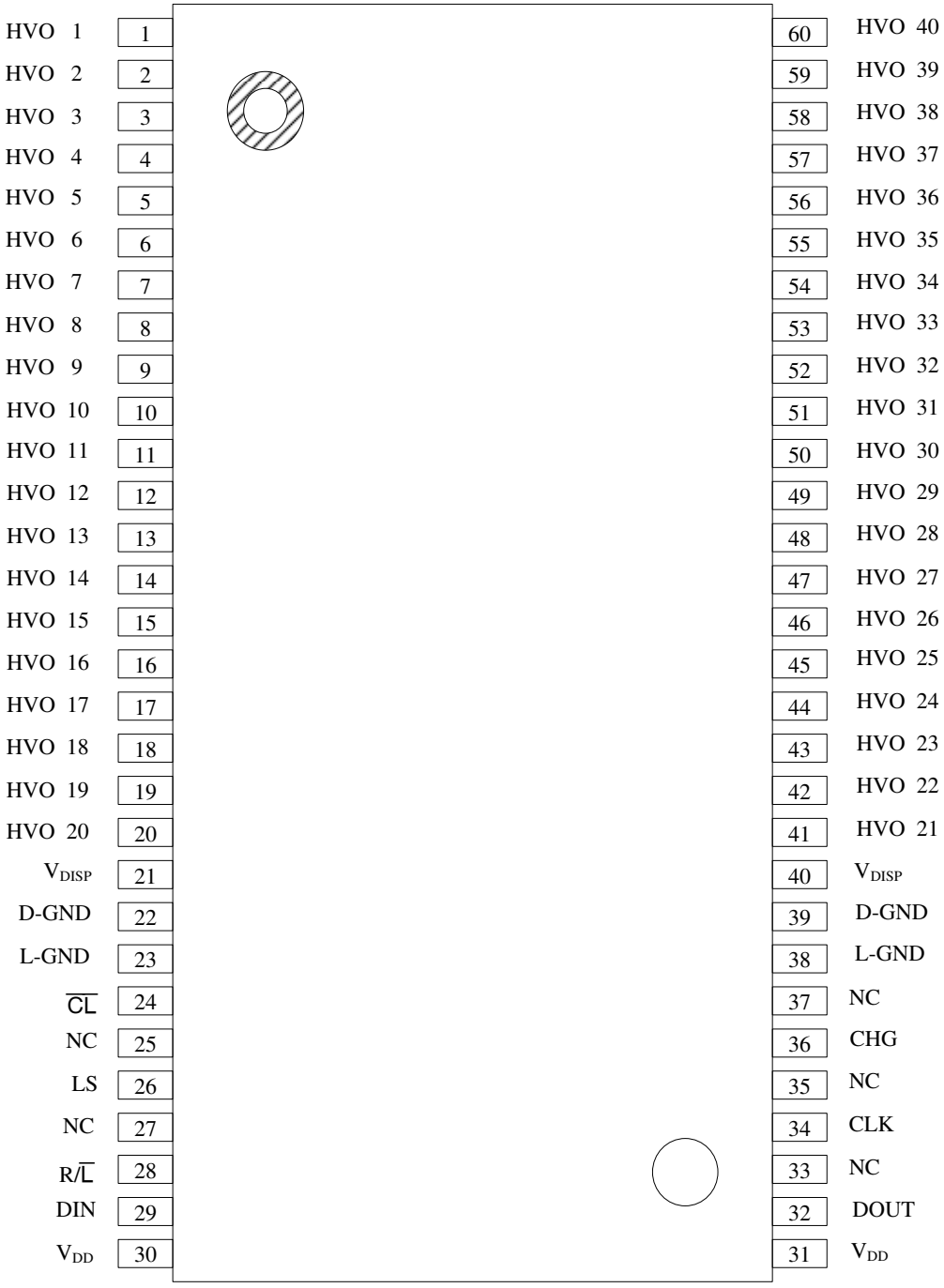
FEATURES

- Logic Supply Voltage (V_{DD}) : 3.3V±10%or5V±10%
- Driver Supply Voltage (V_{DISP}) : 65V
- Driver Output Current : I_{OHVH1} (Only one driver output: “H”) : –40mA
  I_{OHVH2} (All the driver outputs:“H”) : –2mA
  I_{OHVL} : 1mA
- Directly connected to VFD tube without pull-down resistors
- Data transfer speed : 5MHz
- Package:
  60-pin plastic SSOP (SSOP60-P-700-0.65-BK)(Product name: ML9272MB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

60-Pin Plastic SSOP

PIN DESCRIPTION

Symbol	Type	Description
CLK	I	Shift register clock input pin. Shift register reads data through DIN while the CLK pin is in a low state and the data in the shift register is shifted from one stage to the next stage at the rising edge of the clock.
DIN	I	Serial data input pin of the shift register. Display data (positive logic) is input through the DIN pin in synchronization with clock.
DOUT	O	Serial data output pin of the shift register. Data is output through the DOUT pin in synchronization with the CLK signal. When R/$\overline{L}$ = High, the data of PO40 in the shift register is output through the DOUT pin. When R/$\overline{L}$ = Low, the data of PO1 in the shift register is output through the DOUT pin.
LS	I	Latch strobe input pin When LS is high, the parallel output data (PO1-40) of the shift register read out. When LS goes from high to low, the parallel output data (PO1-40) of the shift register is held.
$\overline{CL}$	I	Clear input pin with a built-in pull-up resistor The $\overline{CL}$ pin is normally being set high. If the $\overline{CL}$ pin is high and the CHG pin is low, the driver outputs (HV01 to HV40) are in phase with the corresponding latch outputs (O1 to O40). If the $\overline{CL}$ pin is high and the CHG pin is high, the driver outputs (HV01 to HV40) are high irrespective of the states of the latch outputs. If the $\overline{CL}$ pin is set low, the driver outputs are driven low irrespective of the states of the CHG pin and latch outputs. This allows display blanking to be set.
CHG	I	Input for testing (with a pull-down resistor) The CHG pin is normally being set low. If the CHG pin is low and the $\overline{CL}$ pin is high, the driver outputs (HV01 to HV40) are in phase with the corresponding latch outputs (O1 to O40). If the CHG pin is low and the $\overline{CL}$ pin is low, the driver outputs (HV01 to HV40) are low irrespective of the states of the latch outputs. If the CHG pin is set high and the $\overline{CL}$ pin is high, the driver outputs are driven high irrespective of the states of the latch outputs. This provides the easy testing of all lights after final assembly.
HVO1-40	O	High voltage driver outputs for driving a VFD tube The driver outputs are in phase with the corresponding latch outputs (O1 to O40). The direct connection to the grid or anode of a VFD tube eliminates pull-down resistors.
V_{DISP}	—	Power supply pin for driver circuits of VFD tube
V_{DD}	—	Power supply pin for logic
D-GND	—	GND pin for driver circuits of a VFD tube. (D-GND) Since the D-GND is not connected to L-GND, connect this pin to the external L-GND.
L-GND	—	GND pin for logic circuits. (L-GND) Since the L-GND pin is not connected to D-GND, connect this pin to the external D-GND.
R/$\overline{L}$	I	Data shift direction control pin with a built-in pull-up resistor. When R/$\overline{L}$ = High, the data shifts from shift register PO1 to shift register PO40. When R/$\overline{L}$ = Low, the data shifts from shift register PO40 to shift register PO1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic Supply Voltage *1	V_{DD}	Applicable to the logic supply pin	–0.3 to +6.5	V
Driver Supply Voltage *1, *2	V_{DISP}	Applicable to the driver supply pin	–0.3 to +70	V
Input Voltage	V_{IN}	Applicable to all input pins	–0.3 to V_{DD}+0.3	V
Data Output Voltage	V_{O1}	Applicable to the data output pin	–0.3 to V_{DD}+0.3	V
Driver Output Voltage	V_{O2}	Applicable to the driver output pin	–0.3 to V_{DISP}+0.3	V
Power Dissipation	P_D	Ta ≤ 105°C	266	mW
Package Thermal Resistance *3	Rj-a	—	75	°C/W
Storage Temperature	T_{STG}	—	–55 to +150	°C
Output Current	I_{O1}	HVO1 to HVO40	–50.0 to 2.0	mA
	I_{O2}	DOUT	–2.0 to 2.0	

Notes: *1 Maximum Supply Voltage with respect to L-GND and D-GND

*2 Permanent damage may be caused if the voltage is supplied over the rating value.

*3 Package Thermal Resistance (between junction and ambient)

The junction temperature (Tj) expressed by the equation indicated below should not exceed 150°C.

Tj=P×Rj-a + Ta (P: Maximum power dissipation)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	When the power supply voltage is 5.0 V (typ.)	4.5	5.0	5.5	V
		When the power supply voltage is 3.3 V (typ.)	3.0	3.3	3.6	V
Supply Voltage (2)	V_{DISP}	Applicable to the driver supply voltage pin	10	—	65	V
CLOCK Frequency	f_{CLK}	See the timing diagram	—	—	5	MHz
Operating Temperature	Ta	—	–40	—	105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 3.0 to 3.6V or 4.5 to 5.5V, V_{DISP} = 10 to 65V, Ta = –40 to +105°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	All inputs	V_{DD} = 5.0 V ± 10 %		0.8 V_{DD}	—	—	V
			V_{DD} = 3.3 V ± 10 %		0.8 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All inputs	V_{DD} = 5.0 V ± 10 %		—	—	0.2V_{DD}	V
			V_{DD} = 3.3 V ± 10 %		—	—	0.2V_{DD}	V
High Level Input Current	I_{IH1}	V_I = V_{DD}	CHG pin	V_{DD} = 5.0V	5	—	120	µA
				V_{DD} = 3.3V	2.5		40	µA
	I_{IH2}		Other input pins		–1	—	1	µA
Low Level Input Current	I_{IL1}	V_I = 0V	$\overline{CL}$, R/$\overline{L}$ pin	V_{DD} = 5.0V	–80	—	-5	µA
				V_{DD} = 3.3V	–40	—	-2.5	µA
	I_{IL2}		Other input pins		–1	—	1	µA
Driver High Level Output Voltage	V_{OH1-1}	HVO1 to HVO40	I_{OH1-1} = –40mA, VDISP= 65V Only one output is high		V_{DISP}-5.0	—	—	V
	V_{OH1-2}	HVO1 to HVO40	I_{OH1-2} = –2.0mA, VDISP= 65V All outputs are high		V_{DISP}-0.7	—	—	V
	V_{OH2}	DOUT	I_{OH2} = –0.1mA		V_{DD}-1.0	—	—	V
Driver Low Level Output Voltage	V_{OL1}	HVO1 to HVO40	I_{OL1} = 1.0mA		—	—	3.0	V
	V_{OL2}	DOUT	I_{OL2} = 0.1mA		—	—	1.0	V
Supply Current (1) (Dynamic Mode)	I_{DD}	V_{DD}	V_{DD} = 5.0±10% Input Data = “1” “0” “1”..		—	—	2.5	mA
			V_{DD} = 3.3±10% Input Data = “1” “0” “1”..		—	—	2.0	mA
	I_{DISP}	V_{DISP}	Input Data = “1” “0” “1”..		—	—	0.5	mA
Supply Current (2) (Static Mode)	I_{DDS1}	V_{DD}	No Operation Ta = 25°C		—	—	1.0	µA
	I_{DDS2}		No Operation Ta = 85°C		—	—	10.0	µA
	I_{DISPS1}	V_{DISP}	No Operation Ta = 25°C		—	—	1.0	µA
	I_{DISPS2}		No Operation Ta = 85°C		—	—	20.0	µA

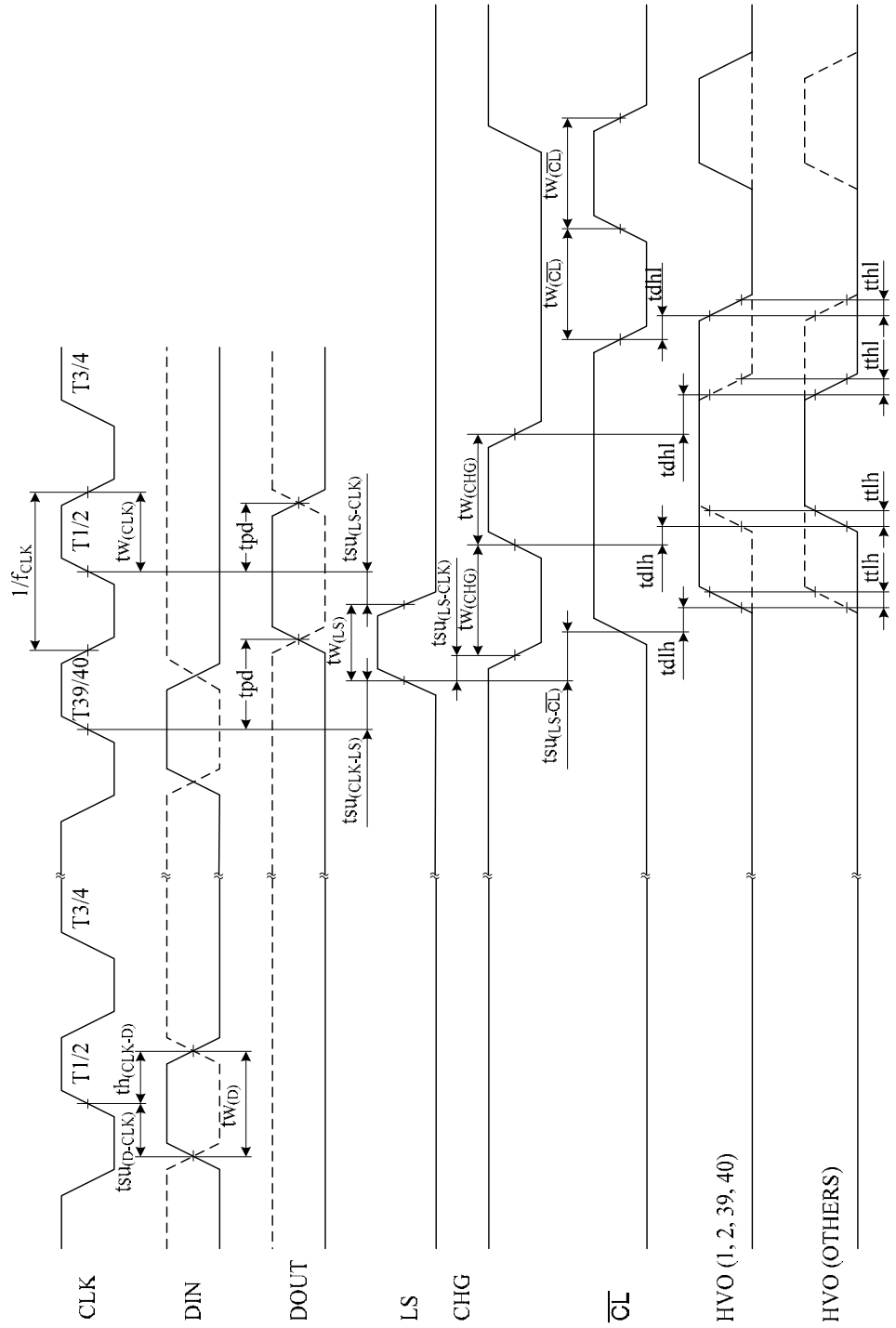
AC Characteristics

(V_{DD} = 3.0 to 3.6V or 4.5 to 5.5V, V_{DISP} = 10 to 65V, Ta = –40 to +105°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLOCK Pulse Width	$t_{W(CLK)}$	—	75	—	—	ns
DATA Setup Time	$t_{SU(D-CLK)}$	—	80	—	—	ns
DATA Hold Time	$t_{H(CLK-D)}$	—	50	—	—	ns
Latch Probe Pulse Width	$tw_{(LS)}$	—	80	—	—	ns
CHG Pulse Width	$tw_{(CHG)}$	—	6	—	—	µs
$\overline{CL}$ Pulse Width	$tw_{(\overline{CL})}$	—	6	—	—	µs
CLK-LS Delay Time	$tsu_{(CLK-LS)}$	—	50	—	—	ns
LS-CLK Delay Time	$tsu_{(LS-CLK)}$	—	0	—	—	ns
LS-CHG Delay Time	$tsu_{(LS-CHG)}$	—	0	—	—	µs
LS-$\overline{CL}$ Delay Time	$tsu_{(LS-\overline{CL})}$	—	0	—	—	µs
DATA OUT Delay Time	t_{PD}	$C_{l\,l}$ = 30 pF	—	—	300	ns
All Output Delay Time	t_{DLH}	$C_{l\,d}$ = 100 pF t_R = 20 to 80% t_F = 80 to 20%	—	0.3	1.0	µs
	t_{DHL}		—	2.0	5.0	µs
All Output Slew Rate	t_{TLH}	$C_{l\,d}$ = 100 pF t_R = 20 to 80% t_F = 80 to 20%	—	0.3	1.0	µs
	t_{THL}		—	2.0	5.0	µs

TIMING DIAGRAM

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH} / V_{IL}	0.8 V_{DD} / 0.2 V_{DD}	0.7 V_{DD} / 0.3 V_{DD}
V_{OH} / V_{OL}	0.8 V_{DISP} / 0.2 V_{DISP}	0.8 V_{DISP} / 0.2 V_{DISP}
	0.8 V_{DD} / 0.2 V_{DD}	0.8 V_{DD} / 0.2 V_{DD}



FUNCTIONAL DESCRIPTION

Function Table

Shift register

Input			Shift Register Parallel Out					Output
CLK	R/$\overline{L}$	DIN	PO1	PO2		PO39	PO40	DOUT
↓	X	X	Not changed					Not changed
↑	H	L	L	PO1n		PO38n	PO39n	PO40
↑	H	H	H	PO1n		PO38n	PO39n	PO40
↑	L	L	PO2n	PO3n		PO40n	L	PO1
↑	L	H	PO2n	PO3n		PO40n	H	PO1

X: Don't Care
PO1n to PO40n: PO1 to PO40 data just before CLOCK rises.

Latch

Input	Shift Register Parallel Out	Latch Output
LS	POm	Om
L	X	Not changed
H	L	L
H	H	H

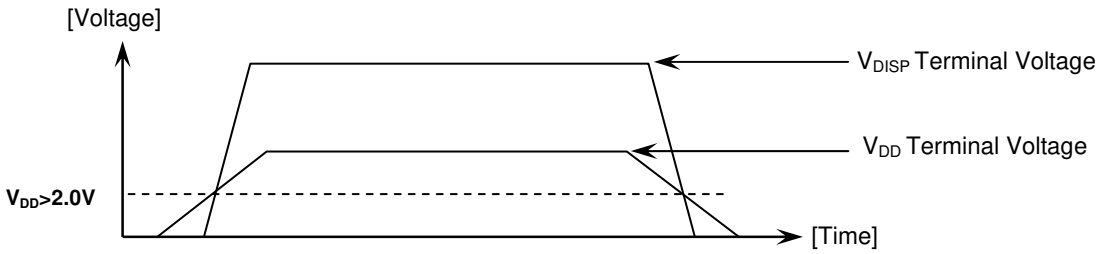
X: Don't Care, m: 1 to 40

Driver output

Input		Latch Output	Driver Output
$\overline{CL}$	CHG	Om	HVOm
L	X	X	L
H	H	X	H
H	L	L	L
H	L	H	H

X: Don't Care, m: 1 to 40

POWER-ON/OFF TIMING



To prevent IC from malfunctioning, V_{DISP} should be applied after V_{DD} is applied.
When turning off the power, V_{DD} should be applied after V_{DISP} is applied.

NOTES ON USE

1. Connect D-GND to L-GND externally to be an equal potential voltage.

2. The contents of the shift register are undefined when the power is applied.

   Therefore, unnecessary driver outputs may be driven high just after power-on, and the VFD tube may flicker.

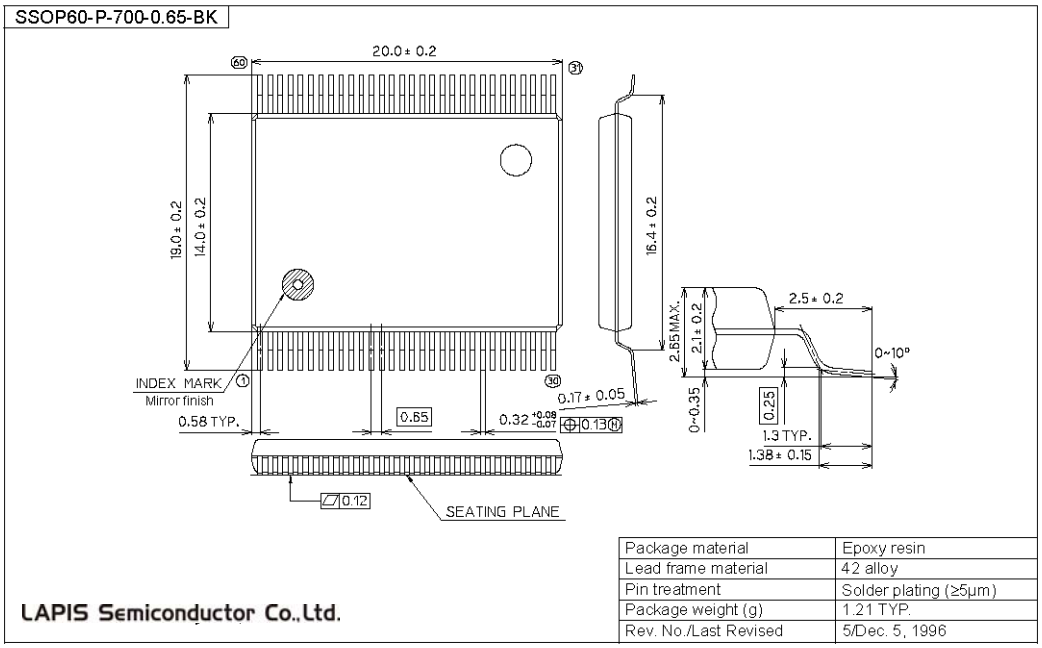
   To avoid this, follow the procedures:

   1) Apply the driver power supply after applying the logic power supply, with the $\overline{CL}$ pin remained low.

   2) Start displaying by setting the $\overline{CL}$ pin high after putting display data from the shift register through the DIN pin.

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.21 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9272-01	Dec. 21, 2005	–	–	Preliminary edition 1
PEDL9272-02	Mar. 17, 2006	1	1	I_{OHVH2} (All the driver outputs:"H") : -7mA → –2mA
		7	7	I_{IH1} MAX 80μA → 120μA V_{OH1-1} MIN V_{DISP}-4.0V → V_{DISP}-5.0V V_{OH1-2} Condition I_{OH1-2} = –7.0mA → –2.0mA
		8	8	CHG Pulse Width , CL Pulse Width Min 2μs → 6μs
FEDL9272-01	April. 27, 2006	–	–	Final edition 1
FEDL9272-02	Mar. 3, 2014	2	2	DIN→D-GND, CLK→L-GND

NOTES

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