

CMOS 4-Bit D-Type Registers

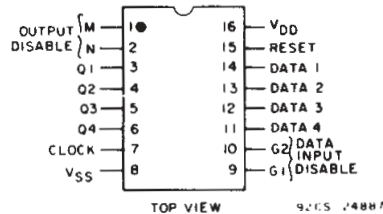
High-Voltage Types (20-Volt Rating)

■ CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

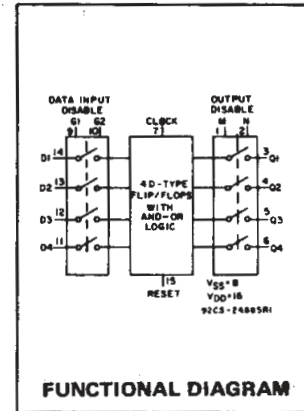
The CD4076B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | UNITS |
|---|--------------|--------|------|---------|
| | | Min. | Max. | |
| Supply Voltage Range (For T_A = Full Package Temperature Range) | | 3 | 18 | V |
| Data Setup Time, t_S | 5 | 200 | — | ns |
| | 10 | 80 | — | |
| | 15 | 60 | — | |
| Clock Pulse Width, t_{PW} | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 80 | — | |
| Clock Input Frequency, f_{CL} | 5 | dc | 3 | MHz |
| | 10 | — | 6 | |
| | 15 | — | 8 | |
| Clock Input Rise or Fall Time, t_{rCL}, t_{fCL} | 5 | — | 15 | μ s |
| | 10 | — | 5 | |
| | 15 | — | 5 | |
| Reset Pulse Width, t_{RW} | 5 | 120 | — | ns |
| | 10 | 50 | — | |
| | 15 | 40 | — | |
| Data Input Disable Setup Time, t_S | 5 | 180 | — | ns |
| | 10 | 100 | — | |
| | 15 | 70 | — | |

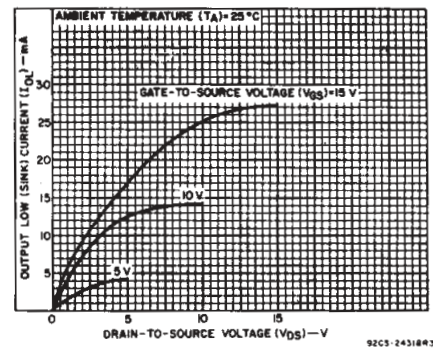


Fig. 1 — Typical output low (sink) current characteristics.

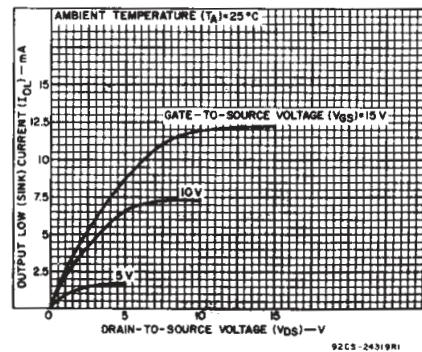


Fig. 2 — Minimum output low (sink) current characteristics.

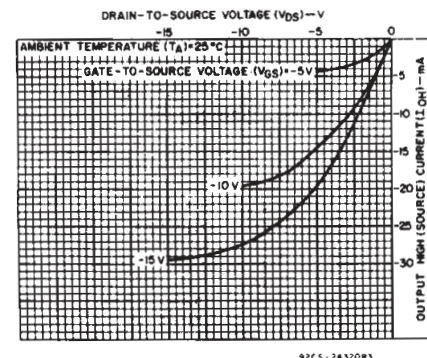


Fig. 3 — Typical output high (source) current characteristics.

CD4076B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

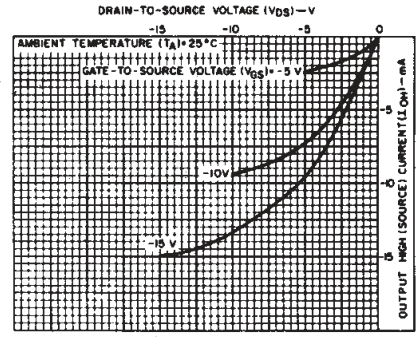
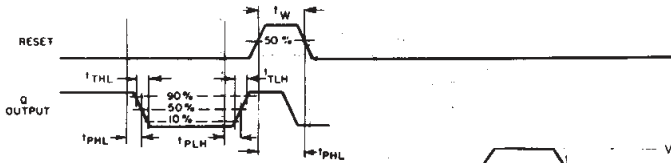
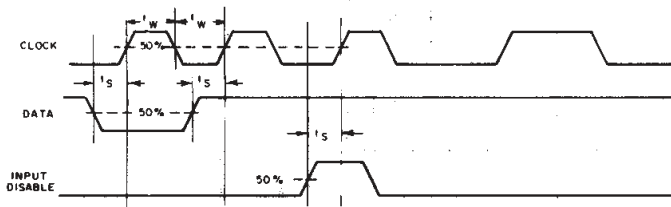
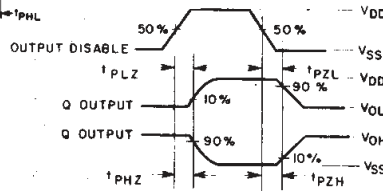


Fig.4 - Minimum output high (source) current characteristics.



92CM-24886R2

(a)

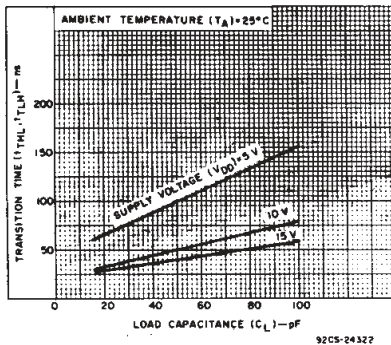


| CHAR. | TEST VOLT. |
|------------------|---------------------------------|
| t _{PHZ} | V _{DD} V _{SS} |
| t _{PLZ} | V _{SS} V _{DD} |
| t _{PZL} | V _{SS} V _{DD} |
| t _{PZH} | V _{DD} V _{SS} |

92CS-29299

(b)

Fig.5 - Functional waveforms for CD4076B.



92CS-24322

Fig.7 - Typical transition time vs. load capacitance.

Truth Table

| Reset | Clock | Data Input Disable G1 | Data Input Disable G2 | Data D | Next State Output Q |
|-------|-------|-----------------------|-----------------------|--------|---------------------|
| 1 | X | X | X | X | 0 |
| 0 | 0 | X | X | X | Q |
| 0 | 1 | 1 | X | X | Q |
| 0 | 1 | X | 1 | X | Q |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | X | X | X | Q |
| 0 | 1 | X | X | X | Q |

When either Output Disable M or N is high, the outputs are disabled (high impedance state), however sequential operation of the flip flops is not affected.

1 = High Level
0 = Low Level
X = Don't Care
NC = No Change

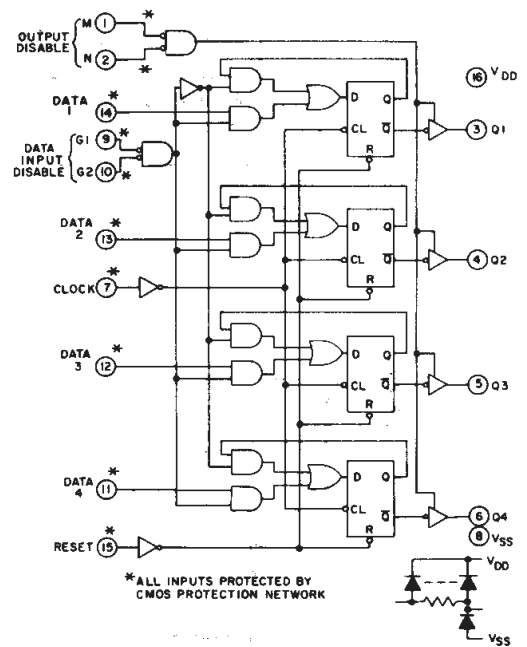


Fig.8 - CD4076B logic diagram.

COMMERCIAL CMOS HIGH VOLTAGE ICs

CD4076B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$ (Unless otherwise noted)

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|---|--------------------------|---------------|------|------|-------|---------------|
| | | V_{DD} V | Min. | Typ. | | Max. |
| Propagation Delay Time: Clock to Q Output, t_{PHL} , t_{PLH} | | 5 | | 300 | 600 | |
| | | 10 | | 125 | 250 | |
| | | 15 | | 90 | 180 | |
| Reset, t_{PHL} | | 5 | | 230 | 460 | ns |
| | | 10 | | 100 | 200 | |
| | | 15 | | 75 | 150 | |
| 3-State Output 1 or 0 to High Impedance, t_{PHZ} , t_{PLZ} | $R_L = 1\text{ k}\Omega$ | 5 | | 150 | 300 | |
| | | 10 | | 75 | 150 | |
| | | 15 | | 60 | 120 | |
| 3-State High Impedance to 1 or 0 Output, t_{PZH} , t_{PZL} | $R_L = 1\text{ k}\Omega$ | 5 | | 150 | 300 | |
| | | 10 | | 75 | 150 | |
| | | 15 | | 60 | 120 | |
| Transition Time, t_{THL} , t_{TLH} | | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| Maximum Clock Input Frequency, f_{CL} | | 5 | 3 | 6 | | MHz |
| | | 10 | 6 | 12 | | |
| | | 15 | 8 | 16 | | |
| Minimum Clock Pulse Width, t_W | | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 40 | 80 | |
| Maximum Clock Input Rise or Fall Time, t_{rcl} , t_{fcl} | | 5 | 15 | - | - | μs |
| | | 10 | 5 | - | - | |
| | | 15 | 5 | - | - | |
| Minimum Reset Pulse Width, t_W | | 5 | - | 60 | 120 | ns |
| | | 10 | - | 25 | 50 | |
| | | 15 | - | 20 | 40 | |
| Minimum Data Setup Time, t_S | | 5 | - | 100 | 200 | ns |
| | | 10 | - | 40 | 80 | |
| | | 15 | - | 30 | 60 | |
| Minimum Data Input Disable Setup Time, t_S | | 5 | - | 90 | 180 | ns |
| | | 10 | - | 50 | 100 | |
| | | 15 | - | 35 | 70 | |
| Input Capacitance, C_{IN} | Any Input | - | - | 5 | 7.5 | pF |

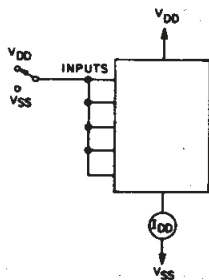


Fig. 11 – Quiescent device current test circuit.

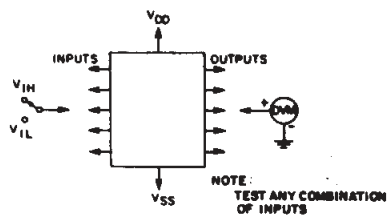


Fig. 12 – Input voltage test circuit.

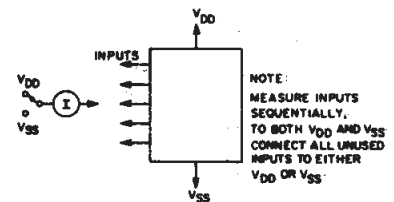


Fig. 13 – Input current test circuit.

CD4076B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0.04 | 5 | μA |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0.04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0.08 | 100 | |
| Output Low (Sink) Current I _{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0,5 | 5 | 0.05 | | | | — | 0 | 0.05 | V |
| | — | 0,10 | 10 | 0.05 | | | | — | 0 | 0.05 | |
| | — | 0,15 | 15 | 0.05 | | | | — | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | — | V |
| | — | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | — | |
| | — | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | — | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | — | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1.9 | — | 10 | 3 | | | | — | — | 3 | |
| | 1.5, 13.5 | — | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | — | 5 | 3.5 | | | | 3.5 | — | — | V |
| | 1.9 | — | 10 | 7 | | | | 7 | — | — | |
| | 1.5, 13.5 | — | 15 | 11 | | | | 11 | — | — | |
| Input Current I _{IN} Max. | — | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0.1 | μA |
| 3-State Output Leakage Current I _{OUT} Max. | 0,18 | 0,18 | 18 | ±0.4 | ±0.4 | ±12 | ±12 | — | ±10 ⁻⁴ | ±0.4 | μA |

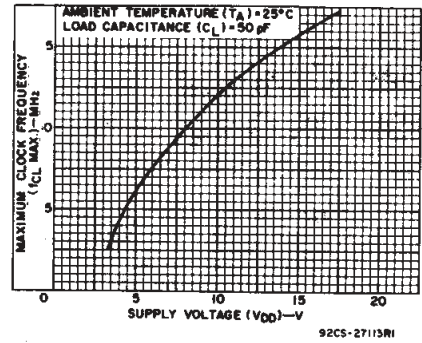


Fig.9 — Typical maximum clock input frequency vs. supply voltage.

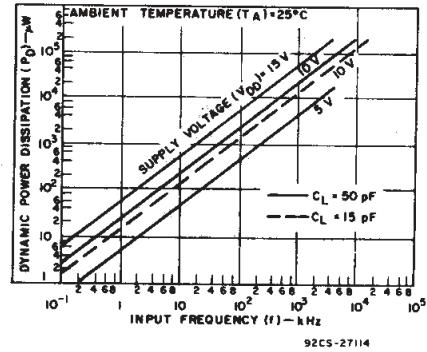
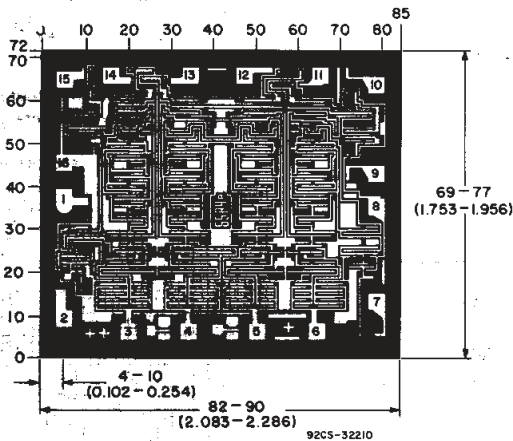


Fig.10 — Typical dynamic power dissipation vs. frequency.



Dimensions and pad layout for CD4076BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|---|
| CD4076BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Contact TI Distributor or Sales Office |
| CD4076BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Contact TI Distributor or Sales Office |
| CD4076BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| CD4076BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| CD4076BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BM96 | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | Purchase Samples |
| CD4076BM96E4 | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | Purchase Samples |
| CD4076BM96G4 | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | Purchase Samples |
| CD4076BME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BMTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BMTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD4076BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD4076B, CD4076B-MIL :

- Catalog: [CD4076B](#)
- Military: [CD4076B-MIL](#)

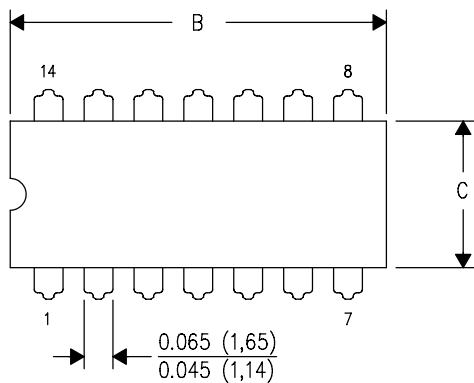
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

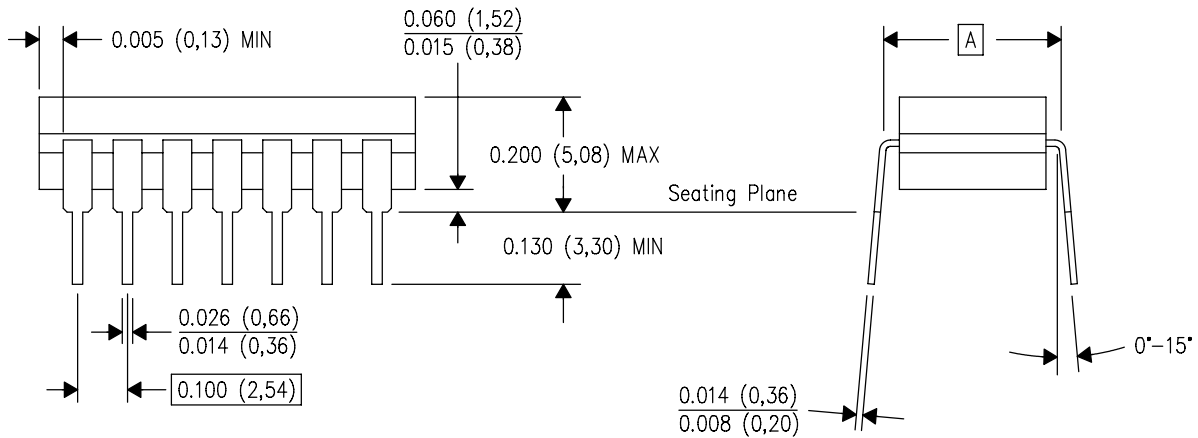
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

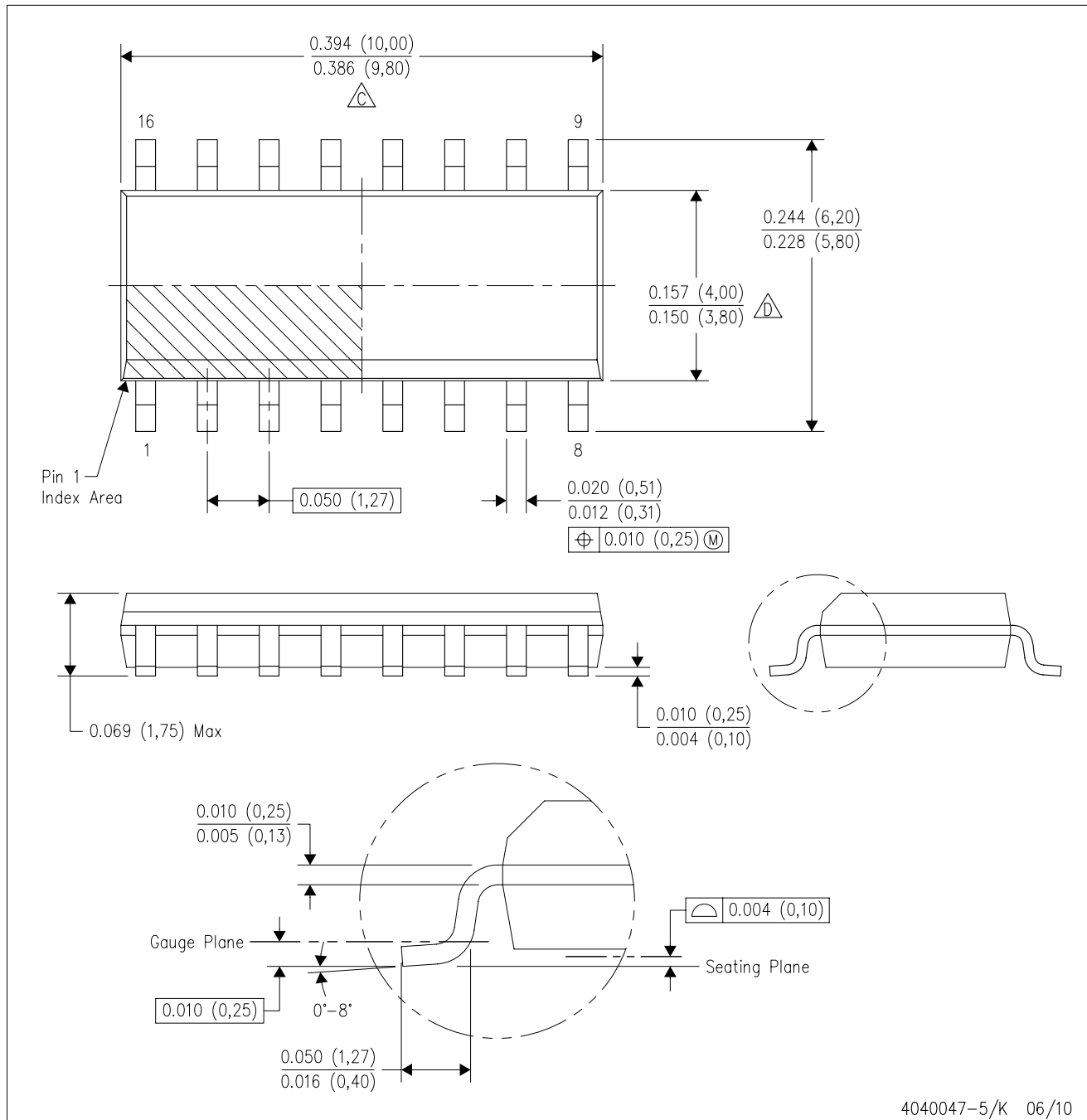
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

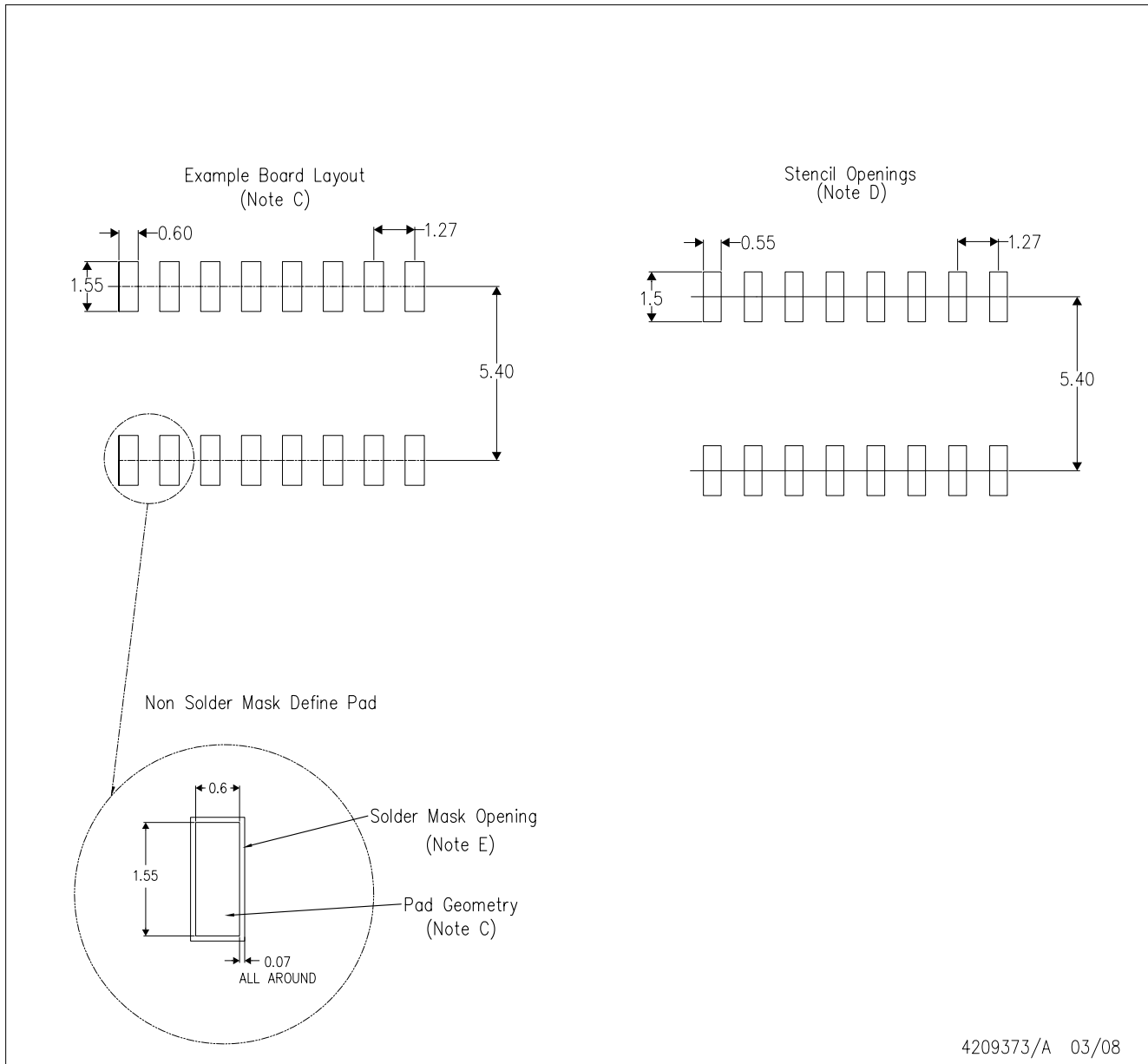
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



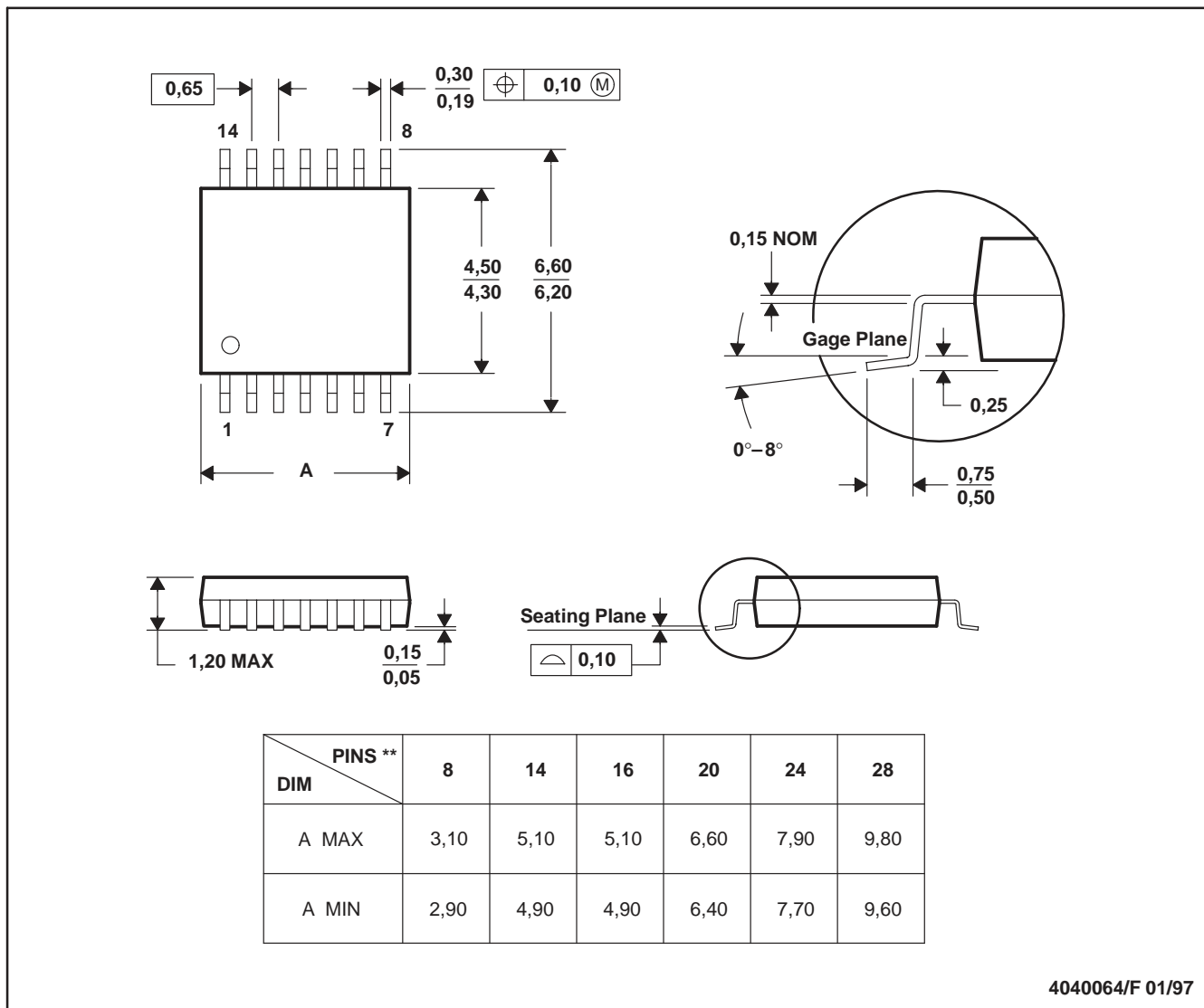
4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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