SHARP

Reference

SPEC No.	EL186032A

ISSUE : Dec. 04 2007

To;

S P E C I F I C A T I O N S

Product Type Current Driver IC for LED

Model No. IR2E49U6

※This specifications contains 30 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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IR2E49PC Reference

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● Please direct all queries regarding the products covered herein to a sales representative of the company.

Content

1. Overview

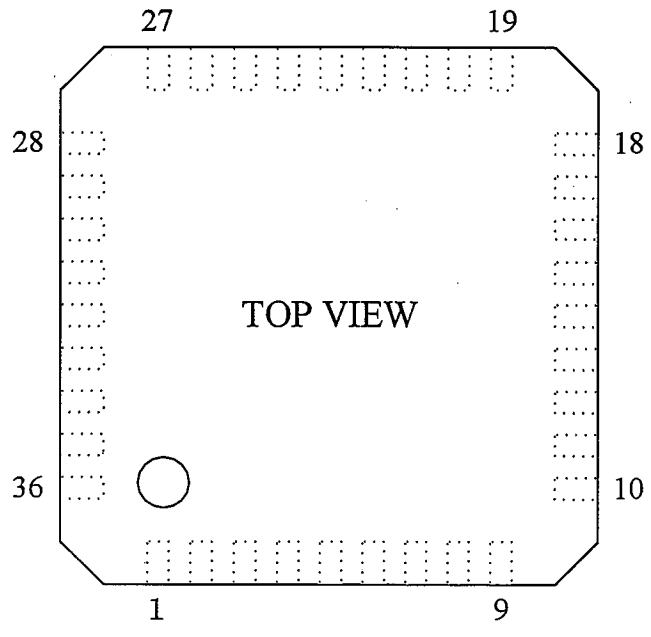
This IC is a current driver supply IC for driving LEDs, consisting of a current driver (5 outputs) and a step-up DC/DC controller.
LEDs with a total of up to 29V VF can be connected in serial, and a large number of LEDs can be driven from a single chip.
The LED driving current values are set with external resistance, and where necessary, can be adjusted through the input of analog voltage. Additionally, it also supports PWM dimming control.

2. Features

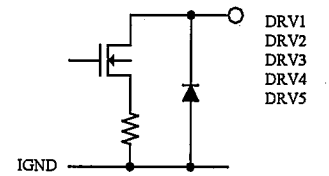
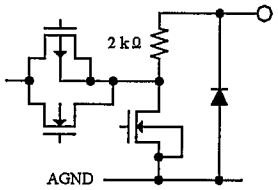
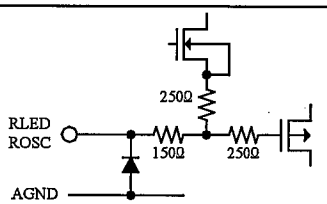
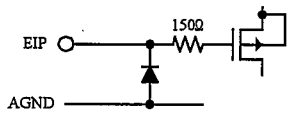
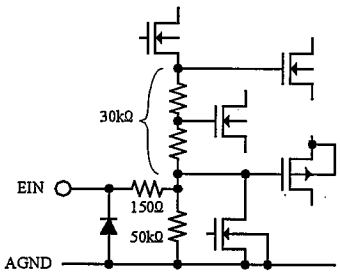
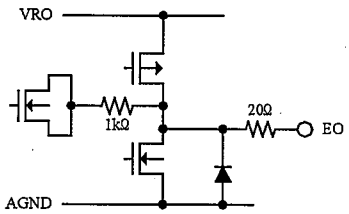
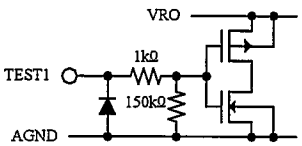
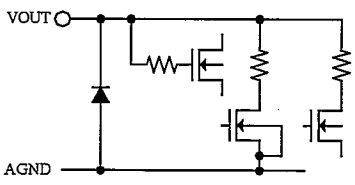
(1) Input voltage range:	6V to 28V
(2) Mounted in the step-up DC/DC controller:	PWM Oscillating frequency setting range 100kHz to 1MHz Output voltage range Vcc to 32V (MIN)
(3) Current driver for LED:	Outputs 5 Current setting range 30mA to 150mA Adjustment of current possible through input of analog voltage Adjustable current range to preset -50% to +50% Voltage input range 0.6V to 1.9V
(4) Support for PWM dimming control:	PWM pulse duty cycle OFF - 100% (During pulse driving: min pulse width 10μs at ROSC=12kΩ)
(5) Mounted safeguards:	Startup inrush current limit function Step-up DC/DC output short protection function Thermal shutdown function
(6) Abnormal status detection functions:	Current driver output open detection (each output can be detected separately) Step-up DC/DC output short protection detection

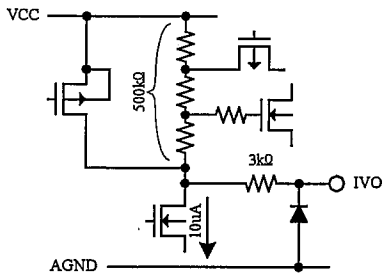
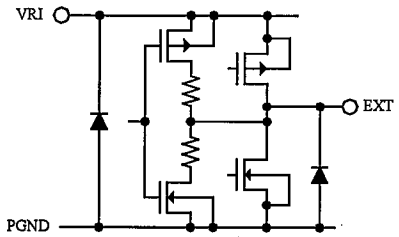
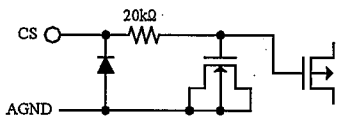
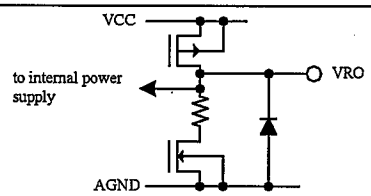
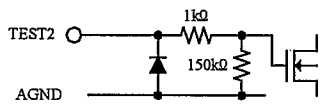
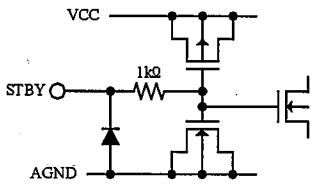
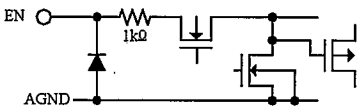
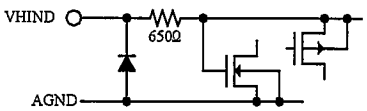
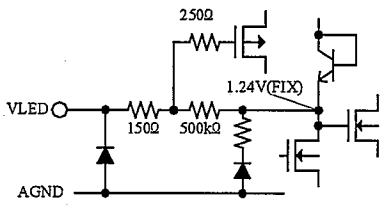
(7) P type silicon substrate monolithic IC (CMOS process)
(8) 6.2 mm × 6.2mm 36pin VQFN package (plastic)
(9) No radiation proofing design
(10) Lead surface finishing (lead-free)

3. Pin configuration



4. Pin description

Pin #	Pin name	I/O	Equivalent circuit	Description
1 3 5 7 9	DRV1 DRV2 DRV3 DRV4 DRV5	O		Current driver 1 - 5 output
10 11 12 13 14	OPN1 OPN2 OPN3 OPN4 OPN5	O		DRV1-5 open detection output pins. High: normal condition, Low: current driver output open Use this pin with 100kΩ pull-up resistance (when VHIND=OPEN), or with inputting voltage into VHIND (in this case, pull-up resistance is not needed). Do the same with the IND pin.
15	IND			VOUT short detection output pin. High: normal condition, Low: VOUT short
17	RLED	-		Resistor connection pin for setting current driver output current (default settings). Connect a resistor between this pin and GND.
18	ROSC			Resistor connection pin for step-up DC/DC oscillating frequency settings. Insert a resistor between this pin and GND.
19	EIP	I		Error amp positive input pin.
20	EIN	I		Error amp negative input pin.
21	EO	O		Error amp output pin.
22	TEST1	I		Test pin. Always use this pin in an open condition.
23	VOUT	I		Step-up DC/DC output voltage monitor pin.

Pin #	Pin name	I/O	Equivalent circuit	Description
24	IVO	O		Switch (Pch. MOSFET) driver output pin to limit startup inrush. Connect to external Pch. MOSFET gate.
25	EXT	O		Output pin for step-up DC/DC Nch. MOSFET driver Connect to external Nch. MOSFET gate.
28	VRI	I		Power supply pin for step-up DC/DC Nch. MOSFET driver Connect to VRO pin.
26	CS	I		Coil current monitor input pin. Insert a resistor between the external Nch.MOSFET source and PGND, and connect the source to this pin. If the voltage difference between CS and PGND exceeds 120mV, (TYP), the external Nch.MOSFET turns OFF.
29	VRO	O		Internal 5V regulator output pin. Connect a 1μF capacitor between this pin and PGND.
30	TEST2	I		Test pin. Always use this pin in an open condition.
32	STBY	I		Standby control input pin. High: Cancel standby Low: Standby (Vth = 1.0V)
33	EN	I		Current driver control input pin. High: ON, Low: OFF (Vth = 1.0V) Min. pulse width 10μs (for details, refer to Figure 5 on Page 10)
34	VHIND	I		IND and OPN 1- 5 output High level voltage input pin. (refer to 「*1 Important points on VHIND」 on Page 5)
35	VLED	I		Voltage input pin for adjustment of current driver output current. (Default settings ±50%). Input voltage range: 0.6V - 1.9V, when open, set at 1.24V.

Pin #	Pin name	I/O	Equivalent circuit	Description
36 2 4 6 8	IGND	-		GND pin for the current drivers 1 – 5.
16	AGND	-		GND pin for analog circuits.
27	PGND			GND pin for step-up DC/DC Nch. MOSFET driver.
31	Vcc	-		Power voltage (input voltage) input pin. Input voltage range: 6V - 28V Connect a 1μF or higher capacitor between this pin and GND.

*1 Important points on VHIND

1) For open drain output (VHIND = OPEN or 0V)

・When VHIND=OPEN

Impress a high-side voltage to the pull up resistor after a time span between the cancellation of standby (STBY=Low→High) and when VRO voltage exceeds operations start-up voltage (Vros) (MIN 1ms). Impressing a high-side voltage to the pull up resistor before VRO voltage exceeds operations start-up voltage (Vros) may result in OPN*, IND voltage not outputting correct voltage.

・When VHIND = 0V

While the VRO voltage during standby (STBY = Low) and after cancellation of standby (STBY=Low→High) does not exceed operations start-up voltage, even if a high-side voltage is impressed to the pull up resistor connected to the OPN*, IND pins, the internal parasitic diode will apply a voltage clamp, and the OPN*, IND pin voltage will only rise to approx. 0.7V.

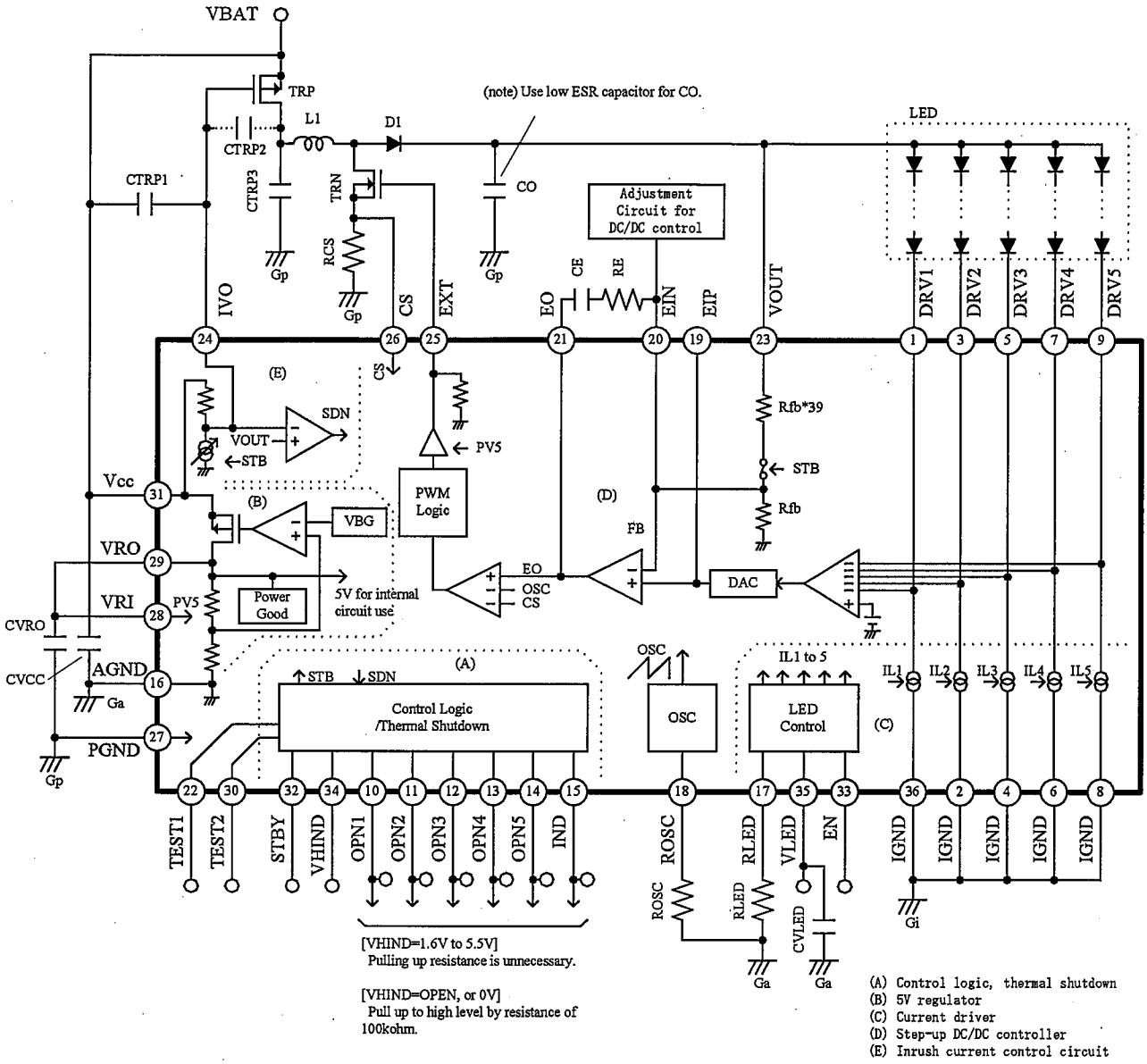
There is a possibility that this voltage may dip below the input Low level threshold for chips connected to the OPN*, IND pins, therefore in order to avoid misidentification as Low output through abnormal status (LED open, VOUT short) detection, a system configuration that ignores OPN* IND pins voltage as long as VRO voltage during standby and after cancellation of standby for the IC does not exceed operations start-up voltage (Vros) is recommended.

2) For CMOS output (VHIND=1.6V - 5.5V)

Use under VHIND voltage >VRO voltage +0.3V conditions may result in inflow current into the VHIND pin, when LED Open or VOUT shorts are detected.

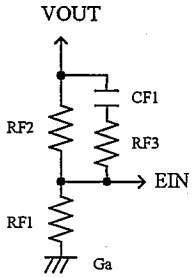
In these cases, ensure that the current supply function for VHIND power supply voltage is MIN 2mA or above.

5. Block diagram and basic connections diagram



[Adjustment Circuit for DC/DC control]

Adjustment of response speeds (or stability) for DC/DC control through use of the following parts may be necessary depending on usage conditions (input voltage range, output current range, temperature range, board pattern, etc.). Therefore, it is recommended that a pattern in which these parts can be connected is used in the investigative stage for boards with this IC.



[Board Layout Consideration]

1) Locate the decoupling capacitors (CVCC, CVRO) between Vcc and AGND, and between VRO and PGND as close as possible to the IC.

2) Ground patterns

Short all GND pins (AGND, PGND, IGND) as close as possible to the IC, and ensure no voltage differences when power supply is on and off.

Ensure that GND connection points of external devices are as indicated on block diagram and basic connections diagram on P.6.

Ga: AGND (analog GND)
Gp: PGND (switching regulator GND)
Gi: IGND (current driver GND)

Ensure that impedance for GND patterns is as low as possible.
Large pulse current flowing on PGND (Gp) and IGND (Gi) causes fluctuation on AGND (Ga), which may lead to instability in circuit operation.

Additionally, in order to reduce mutual interference, it is recommended that each wiring for each GND (Ga, Gp, Gi) be wired independently from a point on the GND side of the capacitor CVRO.

3) Please ensure a peripheral pattern that avoids noise on the following pins.
RLED (17 pin), ROSC (18 pin), EIP (19 pin), EIN (20 pin), EO (21 pin), VLED (35 pin)

Furthermore, please note that the following are examples of large amplitude signal lines on this IC.
DRV 1 - 5 (1, 3, 5, 7, 9 pin) , EXT (25 pin) , EN (33 pin)

4) Do not set the following pins at a floating status (no input status). During standby, set these at GND.
STBY (32 pin), EN (33 pin)

5) Ensure that wiring width does not exceed permissible values for the driving current.
Please note that LEDs may have current flow of maximum 150mA, and L1, TRN, TRP, RCS, D1, and CO may have current of several amps (depending on application, over 10A).

6. Descriptions of the Operations

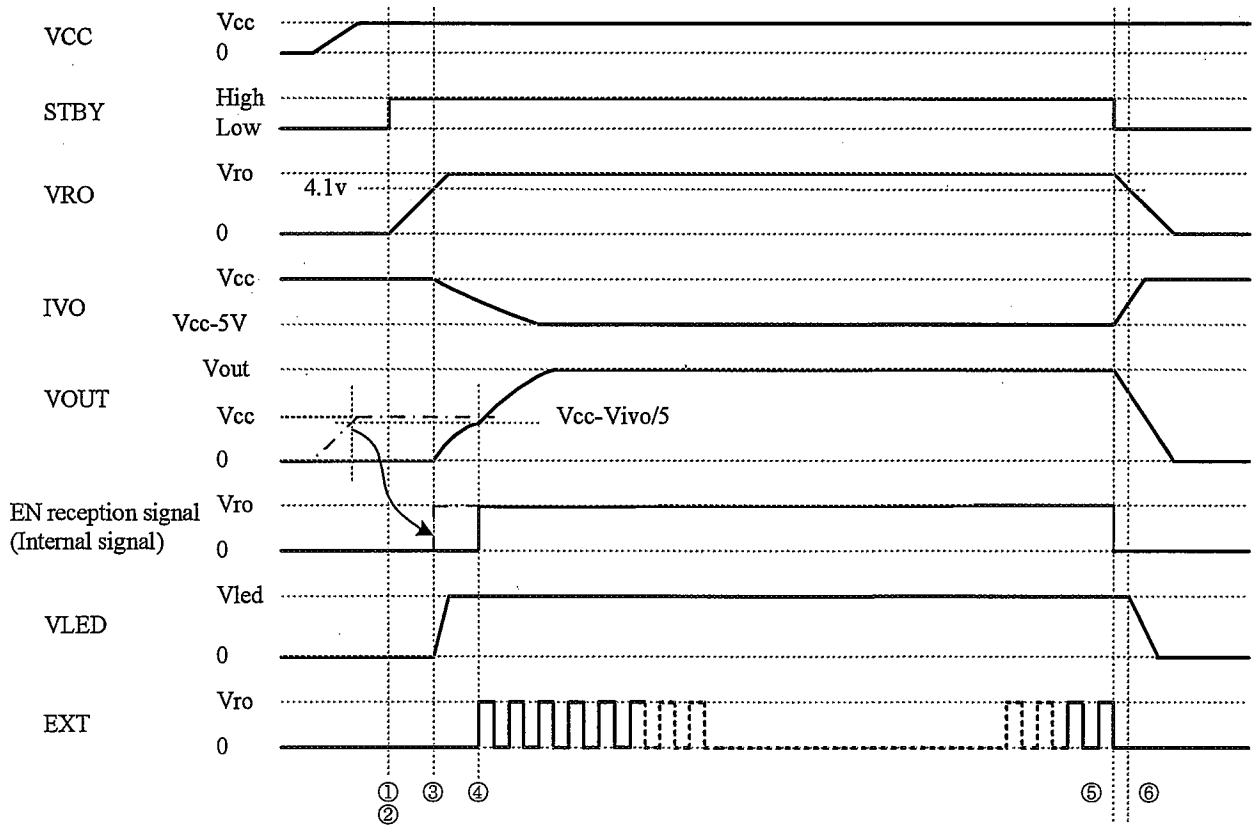
The IR2E49U/U6 comprises control logic, a thermal shutdown circuit, [A], 5V regulator [B], current driver [C], step-up DC/DC controller [D], and inrush current control circuit (E).
(Letters within [ ] are figures in block diagram and basic connections diagram on P.6.)
Below are explanations of their operation.

(l) Control logic, thermal shutdown circuits
This IC is started and shutdown in the following sequence.

[Startup]
① STBY = Low → High
② Start 5V regulator
③ (a) Start charging of output smoothing capacitor (block diagram: CO)
When using startup inrush current limit functionality, this limits the startup current while charging CO to Vcc.
When this is not being used, CO is charged to Vcc at the time that voltage is input to Vcc.
(b) Start thermal shutdown circuit
After startup of the 5V regulator, (VRO>4.1V), temperature detection starts.
An overheated status will not be detected if the 5V regulator output VRO is shorted to GND, etc.
Therefore, please ensure that the VRO pin is not shorted to anything else.

④ (a) Allow reception of current driver EN pin signal (PWM pulse).
(b) Start to control VOUT voltage by step-up DC/DC controller.

[Shut down]
⑤ STBY=High→Low
⑥ Shutdown all circuits simultaneously.



— · — indicates EN reception (internal) signal for VOUT if startup inrush current control function is not used.

Figure 1. Startup and shutdown sequence.

[VLED voltage application timing]

When using with voltage input to the VLED pin, input timing of EN pin is as in figure 2.
Inputting EN signal before VLED voltage has started may result in the current driver output being detected as OPEN.

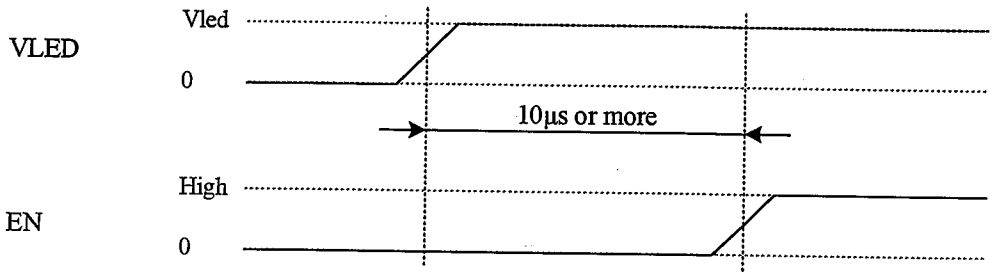


Figure 2. VLED and EN signal timing

- Thermal shutdown function

If the temperature of the IC internal chip exceeds 150°C (MIN), it enters standby status.
When the temperature decreases below this, the standby status is automatically cancelled.

- Abnormal status detection

Detection of either of the following 2 conditions results in output to IND pin and OPN 1 - 5 pins.
Each output status is preserved after detection. Therefore, in order to cancel these, set STBY=Low once.

(1) Step-up DC/DC output (VOUT) short detection
Please refer to Page 12 for short detection conditions.
If a short is detected, the following signals are output to the IND pin.
IND pin voltage = High: normal status, Low: VOUT short

(2) Current driver output open detection
When the EN pin=High, for the period that any of DRV 1 - 5 pins exceeds 2.1V (MIN), if the current that flows to current driver output DRV 1 - 5 drops below 5mA, then this will be determined to be open.

The following signals are output to pins OPN 1 - 5 for current driver output detected as OPEN.
OPN 1 - 5 pin voltage = High: normal status, Low: current driver output OPEN

Additionally, this output circuit switches as below when the VHIND pin voltage is open, or has input of 1.6V - 5.5V (refer to P. 5).

VHIND = OPEN: Nch open drain output (pull-up at 100kΩ.)
VHIND = 1.6V - 5.5V: CMOS output (pull-up resistance not necessary)

(ll) 5V regulator (VRO voltage)

5V (TYP) is generated from the Vcc pin input voltage using the internal regulator. Output from this regulator is used as a power source for internal circuits.
Internal circuits start up with VRO voltage of 4.1V (TYP) or more, and shut down with 3.0V (TYP) or less.

(lll) Current driver

(1) Output current settings and adjustment

Current 5,000 times higher than that which flows through the resistor (RLED) inserted between the RLED pin and GND pin is output to DRV 1 - 5.

RLED pin voltage is controlled to be equivalent to VLED pin voltage, and output current can be hanged within a ±50% range by changing VLED pin voltage without changing RLED values.

The relationship between the current driver output current IDRV (mA), the VLED pin voltage and RLED resistor is as follows. (The graph is shown in Figure 3)

$$IDRV(mA) = VLED(V)/RLED(k\Omega)\times 5000$$

Additionally, ensure current control with the VLED pin voltage is within the following range.

- VLED pin voltage input range:
  0.6V - 1.9V (1.24V with no input)
- Output current range:
  30mA - 150mA

Furthermore, VLED input impedance is TYP 500kΩ (MIN200kΩ). Therefore, when inputting voltage to the VLED pin, ensure that a power supply voltage that takes into consideration inflow and outflow current is used. (Refer to Page 4 for Equivalent circuits)

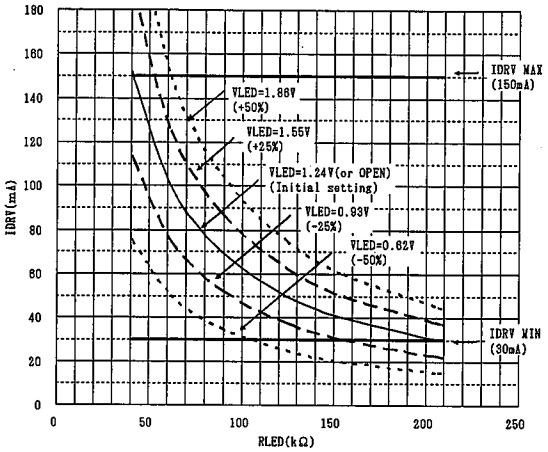


Figure 3. RLED vs. IDRV

(2) PWM dimming

Current driver ON/OFF can be controlled by voltage to the EN pin (EN=High: ON, EN=Low: OFF).

Input a PWM pulse into the EN pin, and by changing the H/L duty ratio (0 - 100%), the current driver ON/OFF duty ratio can be changed, and dimming can be controlled.

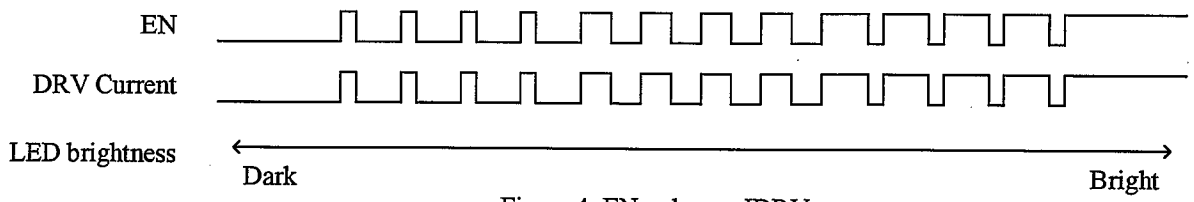


Figure 4. EN pulse vs. IDRV

Furthermore, minimum values for the EN pulse width are above those as indicated in Figure 5.

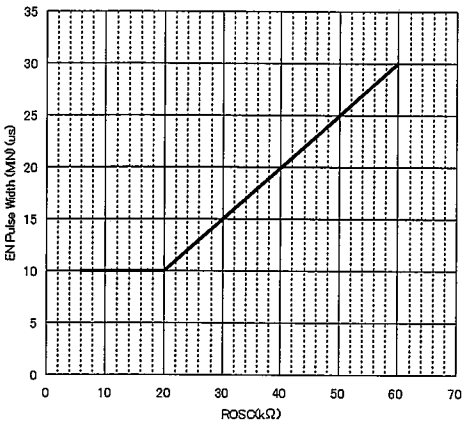


Figure 5. Pulse width (MIN) vs. ROSC

(IV) Step-up DC/DC controller

Voltages at both LED terminals change depending on the LED current and ambient temperature. Therefore, the IR2E49U/U6 has a method to change step-up voltage in accordance with required voltages at both LED terminals in order to reduce wasteful power consumption.

During the EN pin is HIGH, the VOUT voltage from the step-up DC/DC controller is controlled in order that the lowest voltage in DRV 1 - 5 current driver output pins is about 1V.

Here, ensure that the voltage Vf 1 - 5 on both terminals of serially connected LEDs is within the following range.

1) LED Vf 1 - 5 maximum value ≦29V

Maximum value for VOUT voltage during normal operation is 32V (MIN). If Vf exceeds 29V, then the current to the DRV pin to which the LEDs are connected will drop below set values, and the brightness of the LEDs may drop.

2) LED Vf1 - 5 tolerance (between each output)

(Vf 1 - 5 at IDRV=5mA) maximum value - (Vf 1 - 5 at IDRV=set values) minimum value ≦2.1V

If the LED Vf tolerance between each of the outputs exceeds the range above, then the DRV pin to which the LEDs are connected that has a large Vf may be determined to be OPEN. The current for the DRV pin that is determined to be OPEN may drop below set values, and the brightness of the LEDs may drop.

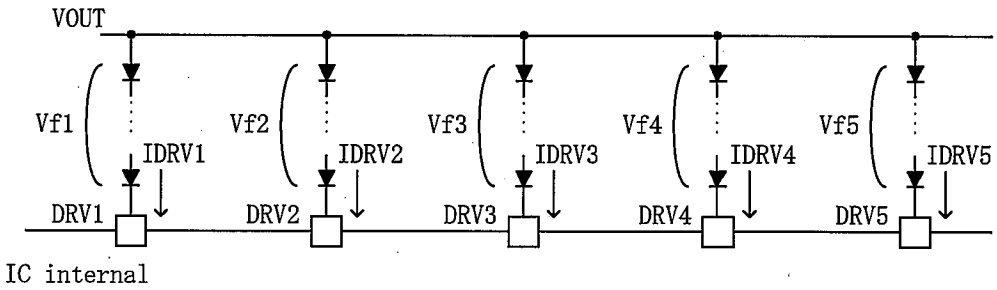


Figure 6. Vf 1 – 5

Step-up DC/DC PWM oscillating frequency fosc

Ensure that oscillating frequency settings are as below. The settings range is 100kHz to 1MHz.

$$fosc\ (kHz) = 500\ (kHz) \times 12\ (k\Omega)/ROSC\ (k\Omega)$$

(V) Startup inrush current control circuit

In the basic configuration diagram (refer to Figure 7) for the step-up DC/DC circuit that is configured externally on this IC, power supply VBAT and output capacitor CO are shorted with low impedance using coil L1 and diode D1. In these cases, at power up, startup inrush current (IrshA) flows into the output capacitor CO. Higher power supply voltages or precipitous rises may result in the inrush current damaging coil L1, diode D1, and condenser CO. In this IC, Pch. MOSFET (TRP) is inserted between power supply VBAT and coil L1 as is shown in Figure 8; the voltage can be gradually raised between these gate sources (the ON resistance gradually drops) and the startup inrush current can be controlled.

IVO pin are connected to GND with a constant current I (10μA TYP) and to the Vcc side with a 500kΩ resistor through a connection that uses an input resistor of 3kΩ. Set the voltage between gate sources at maximum 5V (TYP), and set a time period during which the voltage is lowered, at the value of the capacitor CTRP1: between Vcc, CTRP2: between TRP drain terminals) connected to the IVO pin.

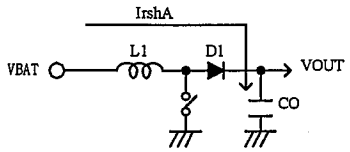


Figure 7. Step-up DC/DC basic configuration diagram

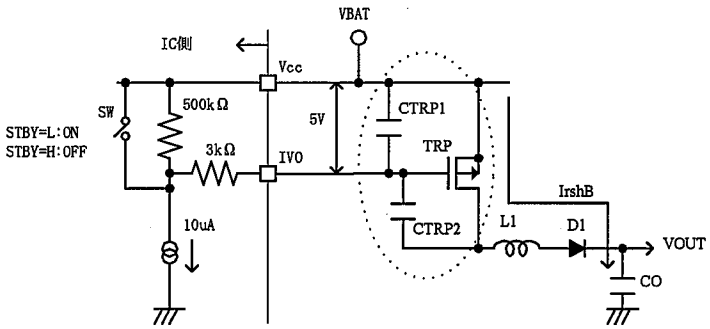


Figure 8. Step-up DC/DC basic configuration diagram of this IC

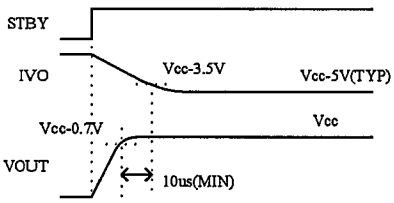


Figure 9. STBY→VOUT timing diagram

[CTRP1, 2 settings values]

After cancellation of standby (STBY=Low→High), until the IVO pin voltage drops 3.5V from Vcc, complete charging of VOUT is required (VOUT>Vcc-0.5V).

Set values after due consideration of the characteristics of Pch. MOSFET used in TRP.

[VOUT short detection]

In the following 2 cases, where it is determined that VOUT has shorted to GND, etc., it will enter shutdown status (in these instances, IND=Low will be output) To restore from shutdown status, set STBY=Low once.

- If, after cancellation of standby, (STBY=Low→High), when the IVO pin voltage drops 3.5V from Vcc, VOUT voltage is VOUT<Vcc-0.5V.
- If, after VOUT voltage has completed charging, VOUT voltage is VOUT<0.5V.

Furthermore, even if not inserting Pch. MOSFET, VOUT short detection is carried out in a similar way. Accordingly, a capacitor CTRP1 is required between the IVO pin and Vcc.

Please refer to [CTRP1, 2 settings values] above for CTRP1 capacitance values.

7. Absolute Maximum Ratings

Ensure that the following values are never exceeded at any time, whether the power is on or off.

Item	Symbol	Condition	Ratings	Unit
Power supply voltage	VCC	Vcc	35	V
Input voltage 1	VIN1	STBY, VOUT, EN, IVO, TEST1,2	-0.3 ~ 35.0	V
Input voltage 2	VIN2	VHIND, VLED, VRI, CS, EIP, EIN	-0.3 ~ 6.0	V
Output voltage 1	VOUT1	DRV1 to 5	-0.3 ~ 35.0	V
Output voltage 2	VOUT2	VRO, EXT, IND, OPN1 to 5, EO	-0.3 ~ 6.0	V
ESD (electrostatic discharge)*2	HBM	Human Body Model	2000	V
	MM	Machine Model	200	V
	CDM	Charged Device Model	1000	V
Power dissipation *3	PD	Ta≦25℃	1923	mW
Power dissipation reduction raito *3	ΔP_D	Ta>25℃	15.38	mW/℃
Operating temperature range	TOPR		-40 ~ 90	℃
Storage temperature range	TSTG		-55 ~ 150	℃

*2 HBM(EIAJ ED-4701 304, MIL-STD-883 3015 compliant : C=100pF, R=1.5kΩ), MM (C=100pF, R=0Ω), CDM (EIAJ ED-4701 305 compliant)

*3 Free Air, On-Board (SEMI42-996compliant)

See Figure 10 for a graph of power dissipation. Ensure that power consumption at each temperature stays within the range as indicated with the line on the graph.

Total power consumption:

P = main unit power consumption (with no external load) + external Nch driver power + current driver loss
= (Vcc × Icc)+(Cnch × VRO ×VRO × fosc) + (VDRVn × IDRVn)n=1-5

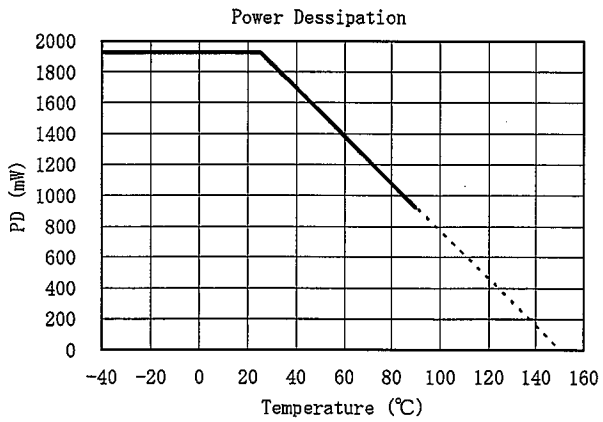


Figure 10. Power Dissipation

VCC : Power supply voltage
Icc : current consumption during operation
Cnch : gate capacitance of externally connected Nch. MOSFET
VRO : 5V (5V regulator output voltage)
Fosc : step-up DC/DC oscillating frequency.
VDRVn : n channel driver voltage (n = 1 - 5)
IDRVn : n channel driver current (n = 1 - 5)

8. Electrical characteristics

Unless otherwise specified:
Ta=25°C Vcc=VOUT=STBY=EN=12V, IVO=10V
DRV 1 - 5=0.8V, CS=0V, RLED=62kΩ, ROSC=12kΩ, VHIND=5V, EXT=no load

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage range:	Vcc	Vcc	6	-	28	V
Quiescent Current (during operation)	ICC	Vcc inflow current pin	-	3	6	mA
Quiescent Current (during standby)	ICCS	Vcc inflow current STBY=Low	-	-	3	μA
5V regulator						
5V regulator output voltage	Vro	VRO voltage	4.6	5.0	5.4	V
Operations start-up voltage	Vros	Raise the VRO voltage from 0V, and measure voltage when IVO reaches 3V.	-	4.1	4.6	V
Hysteresis	VHSro	The VRO voltage difference between startup voltage, and the VRO voltage when operation halts after dropping VRO	0.9	1.1	1.3	V
Current driver						
Output current range	Idrvr	Current values are set by RLED	30	-	150	mA
Output current	IDRV	DRV current. RLED=62kΩ*4	95	100	105	mA
Relative accuracy between outputs	⊿drv	Output current 100mA, (MAX-MIN)/AVERAGE of 5 outputs	-	1	5	%
MIN voltage at DRV pin	Vdrvm	DRV 1 to 5, EN=High	-	-	1	V
EN pulse width	tEN	When EN=High. ROSC=12kΩ*5	10	-	-	μs
VLED voltage input range	Vled	VLED pin.	0.6	-	1.9	V
Current control range (MIN)	SledL	VLED=0.62V ratio to 1.24V(100%)	45	50	55	%
Current control range (MAX)	SledH	VLED=1.86V ratio to 1.24V(100%)	140	150	160	%
VLED input impedance	Zvled	VLED pin	200	500	1000	kΩ
Current driver off leak	LKdrv	DRV pin =28V	-	1	10	μA
Step-up DC/DC controller						
Oscillating frequency range	foscr	ROSC=6kΩ ~ 60kΩ	100	-	1000	kHz
Oscillating freq accuracy	fosc	Measured at EXT pin	-20	0	20	%
Maximum duty ratio	DT	Measured at EXT pin ROSC=12kΩ DT=High period / cycle	77	87	97	%
Maximum output voltage	Vout	The VOUT voltage raised while EIP is maintained regardless of DRV pin voltage. (Exclude the ripple voltage)	32	33	34	V
FET over current detection voltage	Vcs	The voltage at which EXT oscillations stop when CS voltage is raised from 0V	90	120	150	mV
Startup inrush current control circuit						
IVO current	Iivo	IVO inflow current when IVO=12V	5	10	20	μA
VOUT_OK voltage	Vook	The Vcc-VOUT voltage at the time DRV 1 - 5 current starts to flow when VOUT voltage is raised from 0V with IVO=8V	0.5	0.7	0.9	V
IVO_OK voltage	Vivok	The Vcc-IVO voltage at the time IND=High→Low when IVO is dropped, and with VOUT=10V	3.5	4.0	4.5	V
IVO voltage	Vivo	The Vcc-IVO voltage at the point IVO voltage stops dropping with IVO=OPEN	4.0	5.0	5.5	V
VOUT short detection voltage	Vos	The VOUT voltage at the time IND=High→Low when VOUT is dropped from 12V with IVO=OPEN.	0.5	1.0	1.5	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Control input/output						
VHIND pin input voltage range	VHIND	VHIND pin	1.6	-	5.5	V
STBY pin input Low level	VstbL	STBY pin	-	-	0.2	V
STBY pin input High level	VstbH	STBY pin	2	-	-	V
EN pin input Low level	VenL	EN pin	-	-	0.2	V
EN pin input High level	VenH	EN pin	1.4	-	-	V
TEST pin input Low level	VtlL	TEST1, 2 pins	-	-	VRO*0.2	V
TEST pin input High level	VtlH	TEST1, 2 pins	VRO*0.7	-	-	V
TEST pin input impedance	Ztest	TEST 1, 2 pins Calculated with TEST 1, 2=3.0V inflow current	70	150	400	kΩ
IND pin output H level (VHIND=1.6V~5.5V)	VindH	During normal operation. VHIND-IND pin voltage when VHIND=1.6V~5.5V and the IND pin has 20μA outflow current.	-	-	0.3	V
IND pin output L level	VindL	When a VOUT short is detected (IVO=OPEN, VOUT=10V). IND pin voltage when VHIND=OPEN and the IND pin has 50μA inflow current.	-	-	0.3	V
IND pin off leak (VHIND=OPEN)	LKind	During normal operation (IVO=10V, VOUT=12V), An inflow current when IND=5.5V.			1	μA
OPN pin output H level (VHIND=1.6V~5.5V)	VopnH	During normal operation. VHIND-OPN 1 - 5 pin voltage when VHIND=1.6V~5.5V and the OPN 1 - 5 pin has 20μA outflow current.	-	-	0.3	V
OPN pin output L level	VopnL	When DRV detected as being open. OPN 1 - 5 pin voltage when the OPN1 -5 pins have 50μA inflow current.	-	-	0.3	V
OPN pin off leak (VHIND=OPEN)	LKopn	When VHIND=OPEN, and in normal operation, An inflow current when OPN 1 - 5=5.5V.			1	μA
Current driver output open detection						
DRV pin voltage at output open detection	Vdrvopn	The DRV(a) pin=open. DRV(b) pin voltage when DRV(b) pin voltage is raised, and OPN(a) pin voltage becomes Low level.*6	2.1	2.5	3.0	μA

*4 The accuracy of output current (IDRV) change depending on a current set value. Please refer to Figure 11.

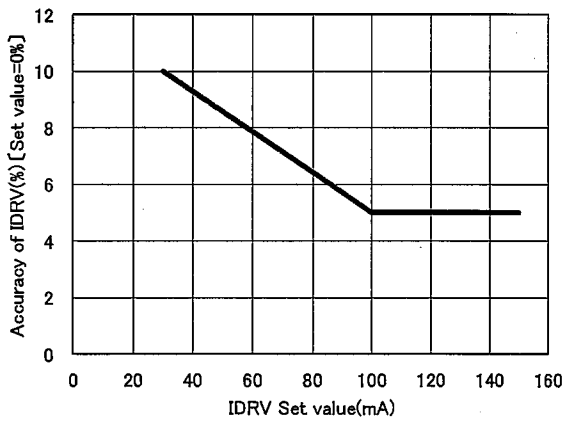
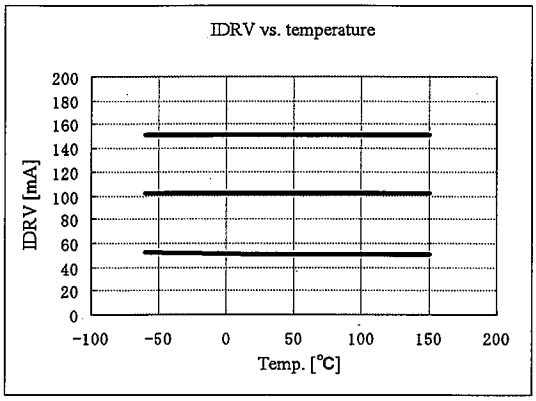


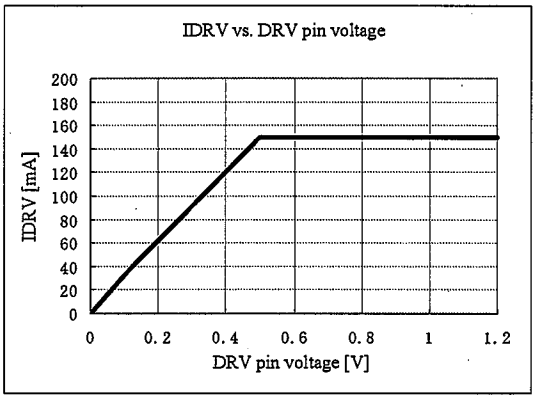
Figure 11. Accuracy of IDRV vs Settings of IDRV

*5 Permissible MIN values for EN pulse width vary depending on ROSC values. Please refer to Figure 5 on Page 10.
*6 DRV(a) and DRV(b) pin are another pins of DRV1-5 pins. In addition , (a) such as OPN(a) and DRV(a) pin is the same number (a).

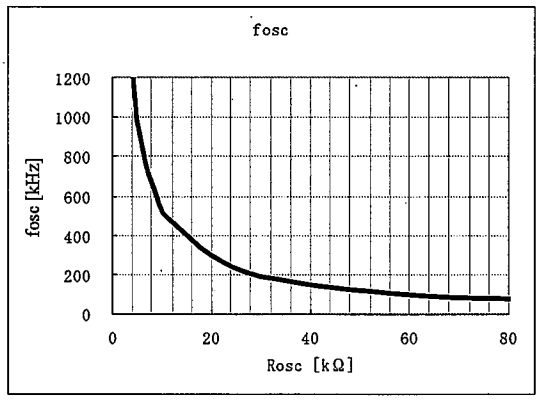
9. Representative characteristics



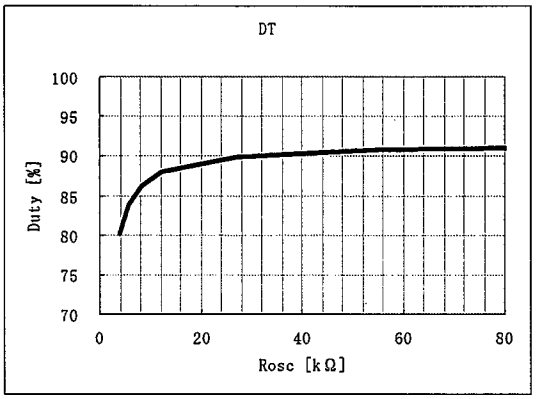
IDRV temperature dependency
When at 150mA, 100mA, or 50mA



Current driver DRV pin voltage dependency
Ta=25°C, DRV pin voltage 0 - 1.2V
DRV pin voltage [V]



Step-up DC/DC PWM oscillating frequency ROSC dependency
Ta=25°C



Step-up DC/DC PWM pulse maximum duty ROSC dependency
Ta=25°C

10 Package and packing specification

[Applicability]

This specification applies to an IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80% (Relative humidity) max.
- Storage period : One year max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

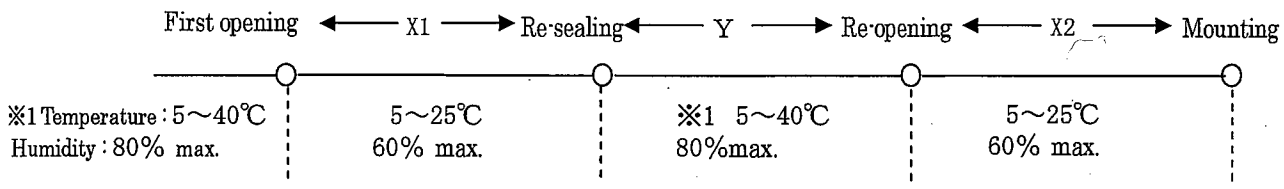
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1＋X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
  (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period : 120+10/-0℃ for 2~3 hours.
- The above baking conditions do not apply since the embossed carrier tape are not heat-resistant . Replace the devices on heat-resistant carrier .

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

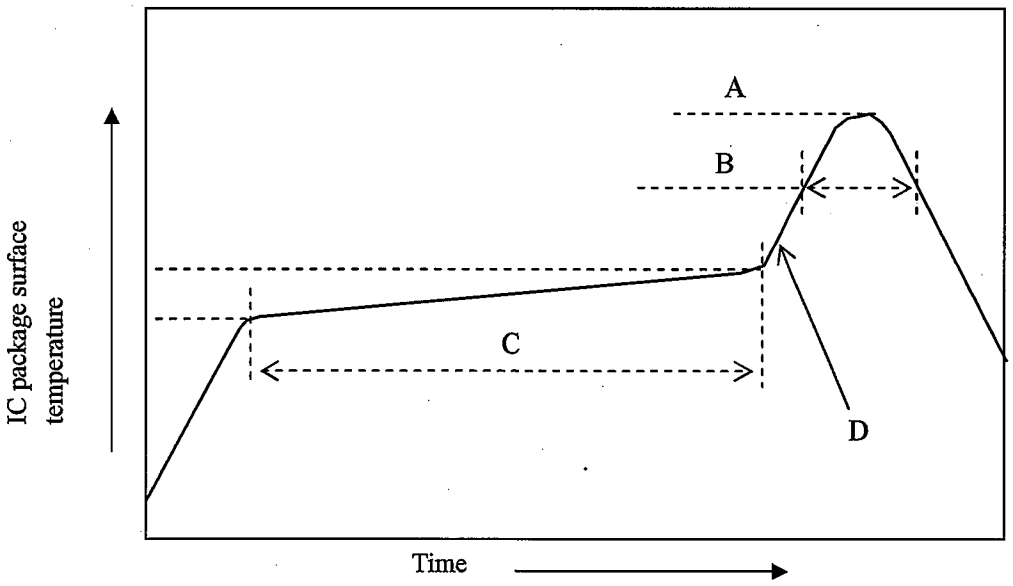
3. Surface mount conditions.

The following soldering conditions are recommended to ensure device quality.

3-1.Soldering.

(1) Convection reflow or IR/Convection reflow. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  - A) Peak temperature. 250℃ max.
  - B) Heating temperature. 40 to 60 seconds as 220℃
  - C) Preheat temperature. It is 150 to 200℃, and is 120±30 seconds
  - D) Temperature increase rate. It is 1 to 3℃/seconds
- Measuring point : IC package surface.
- Temperature profile :



4. Condition for removal of residual flux.
   (1) Ultrasonic washing power : 25 watts / liter max.
   (2) Washing time : Total 1 minute max.
   (3) Solvent temperature : 15～40℃

5. Package outline specification.
   Refer to the attached drawing.
   (Plastic body dimensions do include burr of resin.)
   The contents of LEAD-FREE TYPE application of the specifications. (*2)

6. Markings.
   6-1.Marking details. (The information on the package should be given as follows.)
   (1) Product name : 2E49
   (2) Company name : S
   (3) Date code : (Example) YMXXX
   Y → Denotes the production year. (The which shows years)
   M → Denotes the production month. (1・2・～・8・9・0・N・D)
   XXX → Denotes the production ref. code (3 digit).

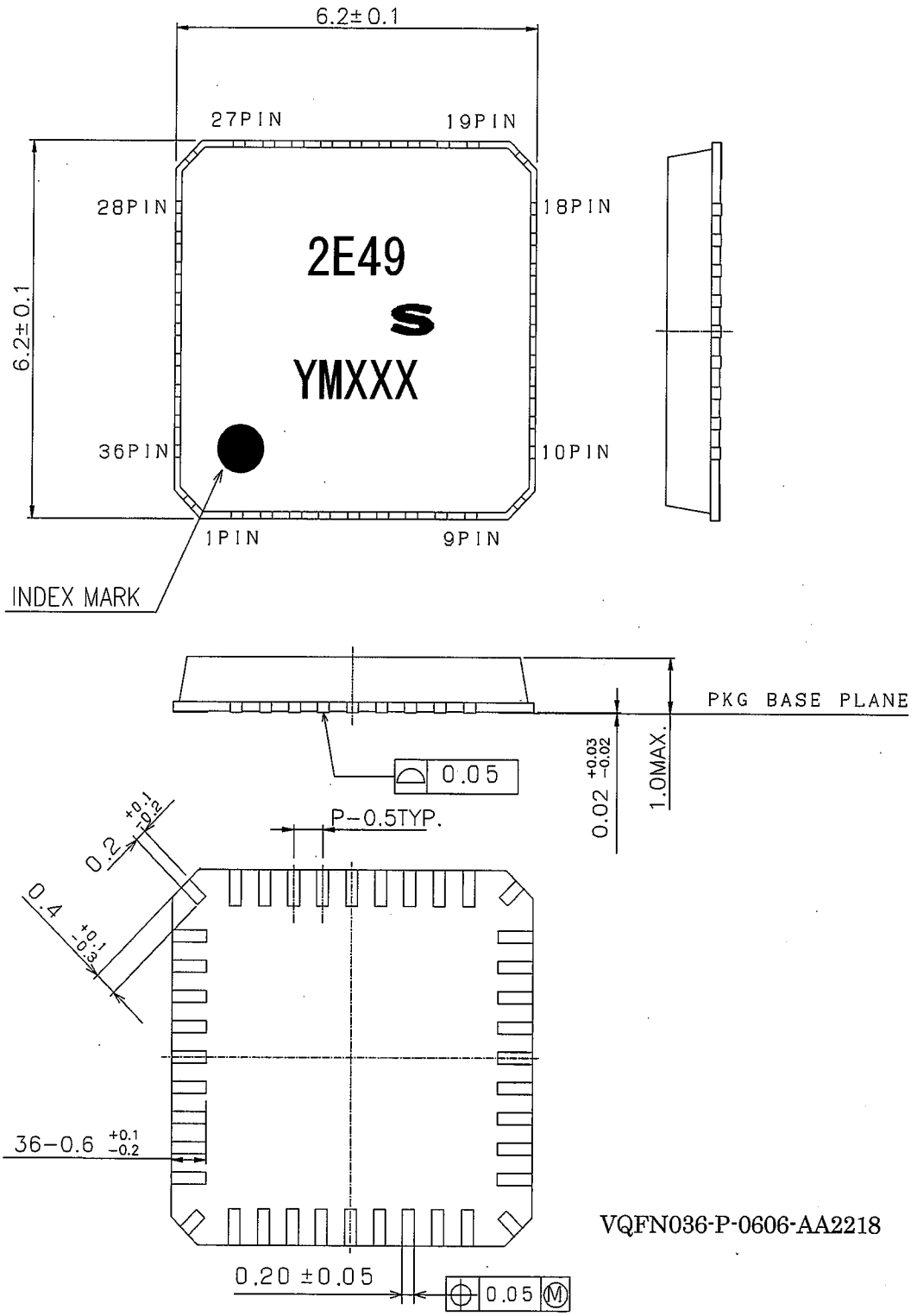
   6-2.Marking layout.
   The layout is shown in the attached drawing.
   (However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-2%Bi) 10μm TYP.(Min. 5μm)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

Reference

(Note) It is those with an underline printing in a date code because of a LEAD FREE type.



VQFN036-P-0606-AA2218

LEAD TYPE	LEAD FINISH	LEAD MATERIAL
	Sn-2%Bi PLATING 10μm TYP.(Min. 5μm)	Cu

NAME	VQFN036-P-0606			NOTE : Plastic body dimensions do include burr of resin.
DRAWING NO.	AA2218	UNIT	mm	

*S20070206

7.Packing specifications (Embossed carrier tape specifications)

This standard applies to the embossed carrier tape specifications for ICs supplied by SHARP CORPORATION. SHARP's embossed carrier tape specifications are generally based on those described in JIS C 0806 (Japanese Industrial Standard) and EIA481A.

7-1.Tape structure

The embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and a top covering tape is used to enclose them.

7-2.Taping reel and embossed carrier tape size

For the taping reel and embossed carrier tape sizes, refer to the attached drawing.

7-3.IC package enclosure direction in embossed carrier tape

The IC package enclosure direction in the embossed portion relative to the direction in which the tape is pulled is indicated by an index mark on the package (indicating the No. 1 pin) shown in the attached drawing.

7-4.Missing IC packages in embossed carrier tape

The number of missing IC packages in the embossed carrier tape per reel should not exceed either 1 or 0.1 % of the total contained on the tape per reel, whichever is larger. There should never be more than two consecutive missing IC packages.

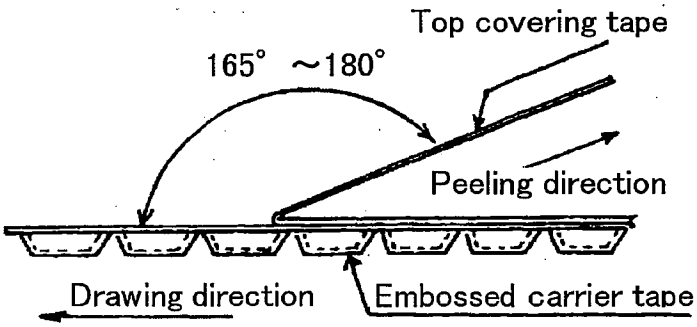
7-5.Tape joints

There is no joint in an embossed carrier tape.

7-6.Peeling strength of the top covering tape

Peeling strength must meet the following conditions.

(1) Peeling angle at 165～180°.
(2) Peeling speed at 300mm／min .
(3) Peeling strength at 0.2～0.7N (20～70gf) .



7-7. Packing

(1) The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, should both be held in place with paper adhesive tape at least 30 mm in length.

(2) The leading and trailing edges of the embossed carrier tape should be left empty (with embossed portions not filled with IC packages) in the attached drawing.

(3) The number of IC packages enclosed in the embossed carrier tape per reel should generally comply with the list given below.

Number of IC Packages/ Reel	Number of IC Packages/ Inner carton	Number of IC Packages/ Outer carton
2000 devices / Reel	2000 devices / Inner carton	10000 devices / Outer carton

7-8.Indications

The following should be indicated on the taping reel and the packing carton.

・Part Number (Product Name) ・Storage Quantity ・Packed Date

・Manufacture's Name (SHARP)

Note : The IC taping direction is indicated by " EL " suffixed to the part number .

EL : Equivalent to " L " of the JIS C 0806 standard..

7-9.Protection during transportation

The IC packages should have no deformation and deterioration of their electrical characteristics resulting from transportation.

8.Precautions for use.

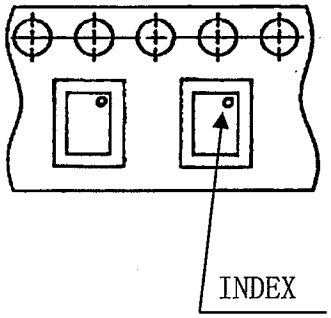
(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The devices should be mounted within one year of the date of delivery.

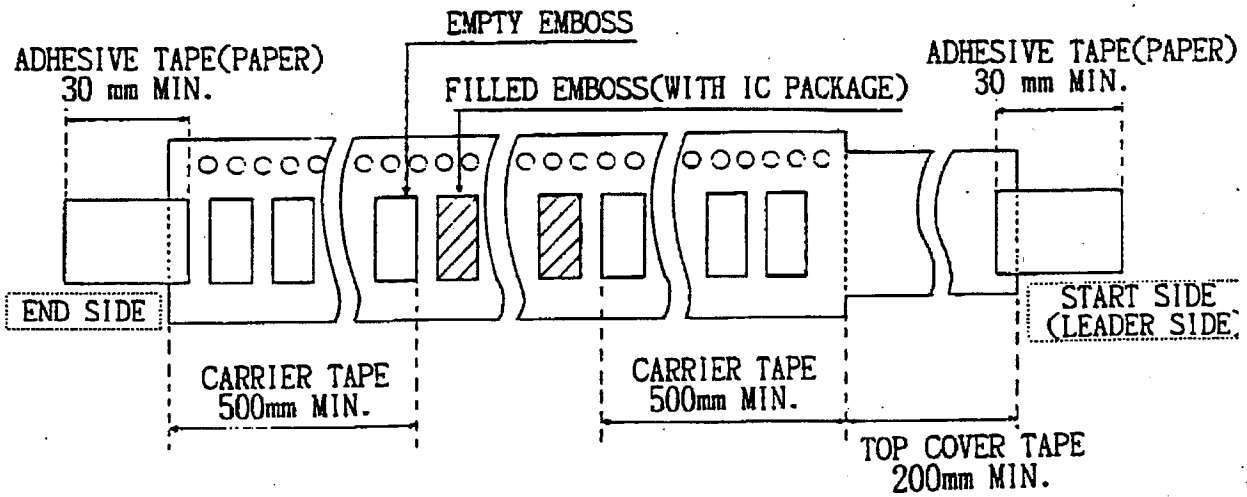
EMBOSS TAPING TYPE (EL)

IC TAPING DIRECTION

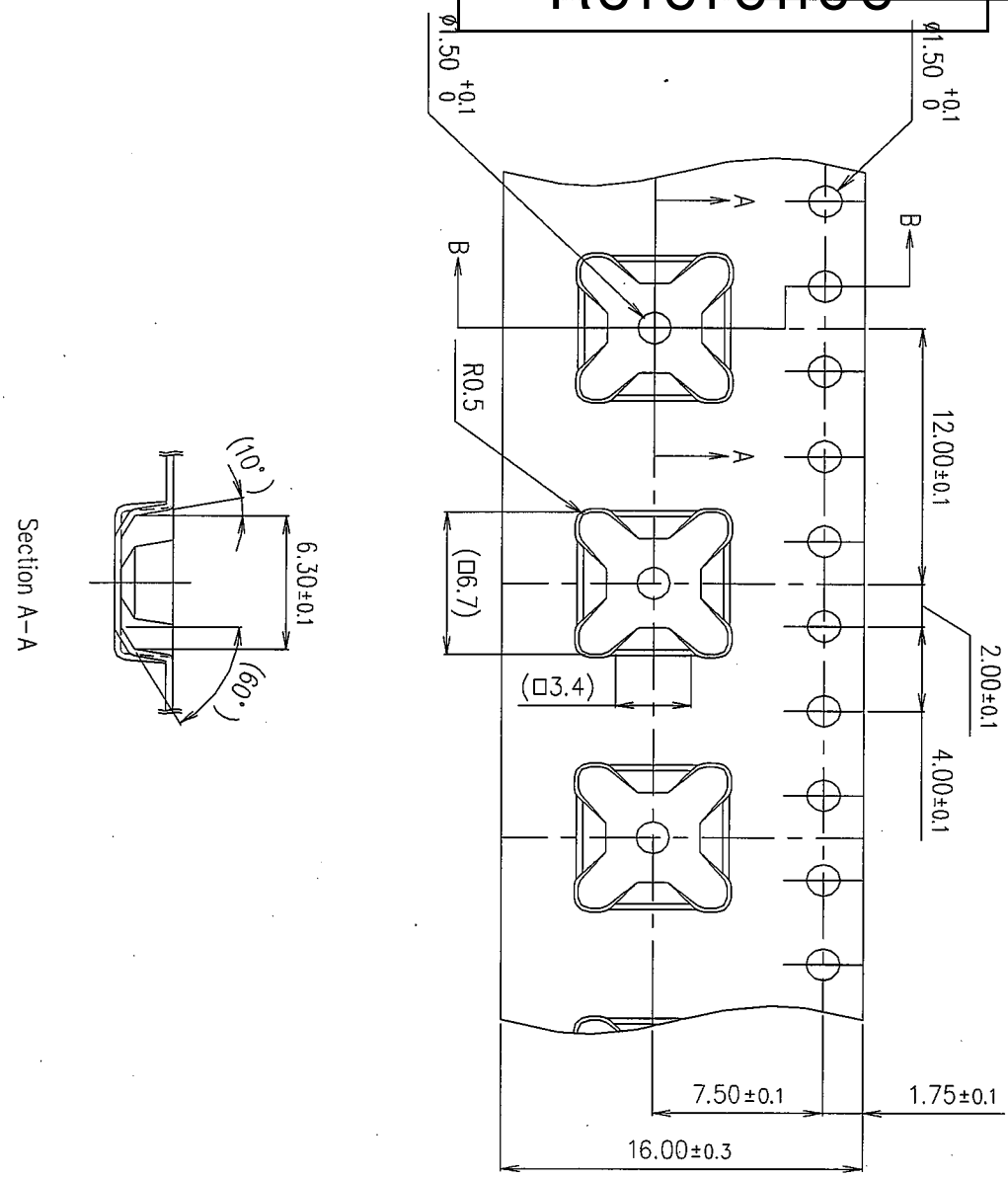
THE DRAWING DIRECTION OF TAPE →



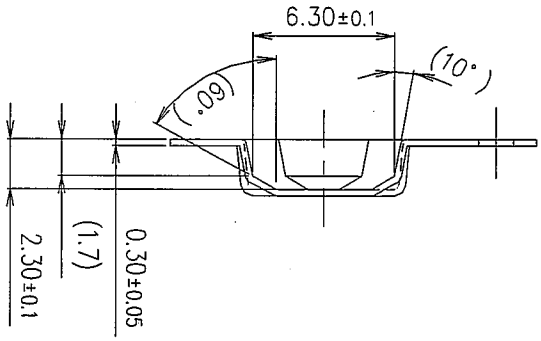
LEADER SIDE AND END SIDE OF TAPE



名称 NAME	Emboss taping type(EL)			備考 NOTE
DRAWING NO.	CV522	単位 UNIT	mm	



Section A–A



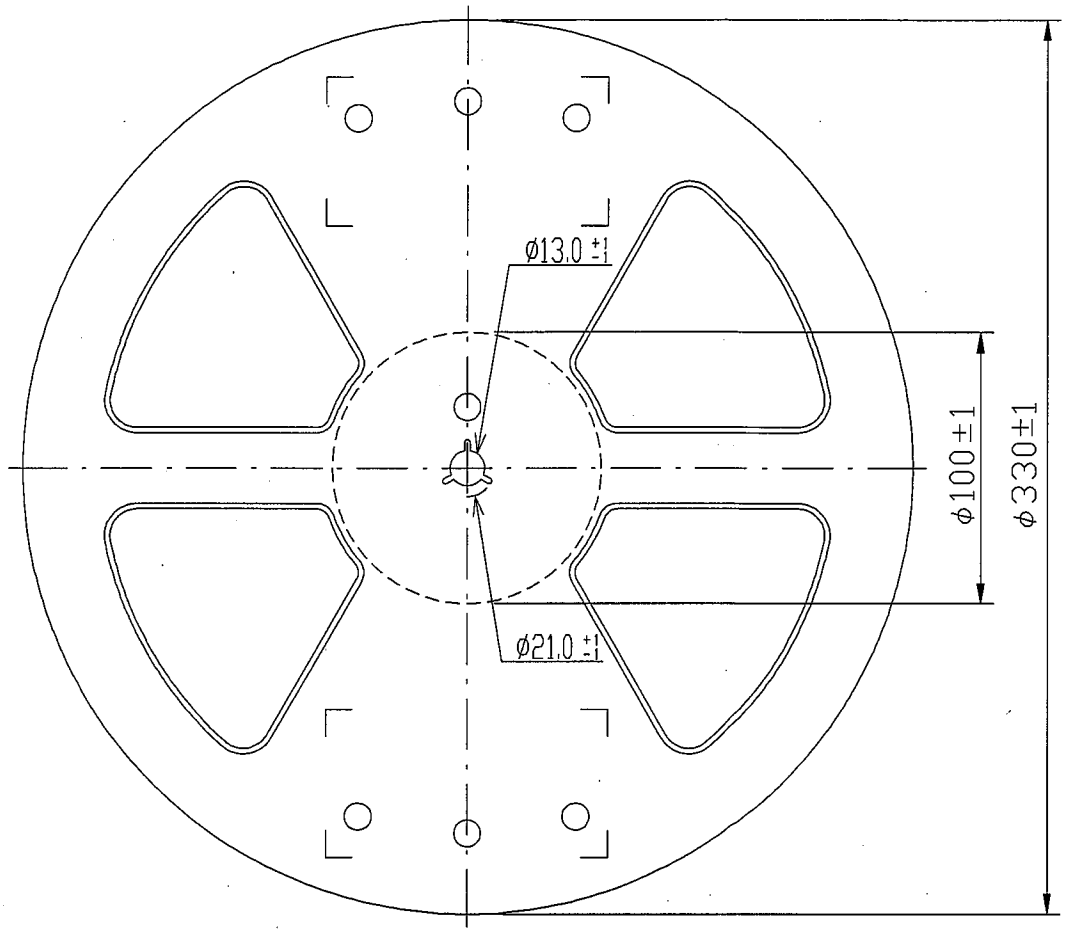
Section B–B

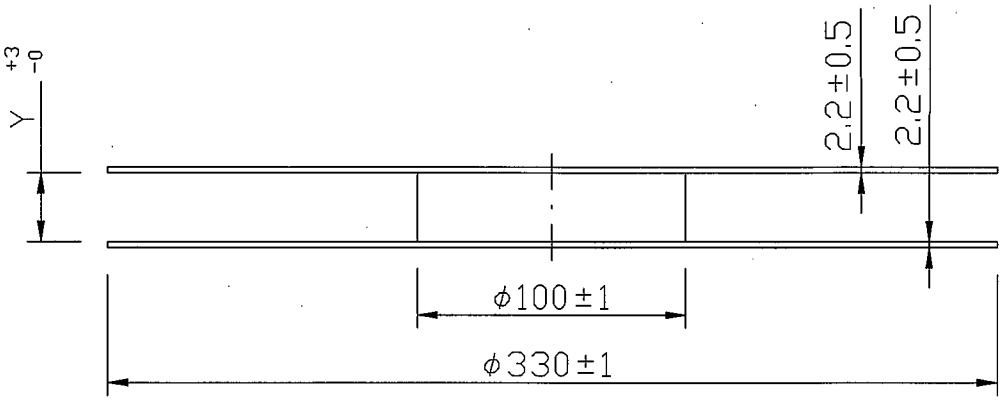
Note
1) The radius (R) is 0.3mm max
2) Cumulative tolerance of 10 pitches of the sprocket hole is ±0.2mm

名称 NAME	EC36-0606VQNSS	備考 NOTE
DRAWING NO. CV888	単位 UNIT mm	

*S20070206

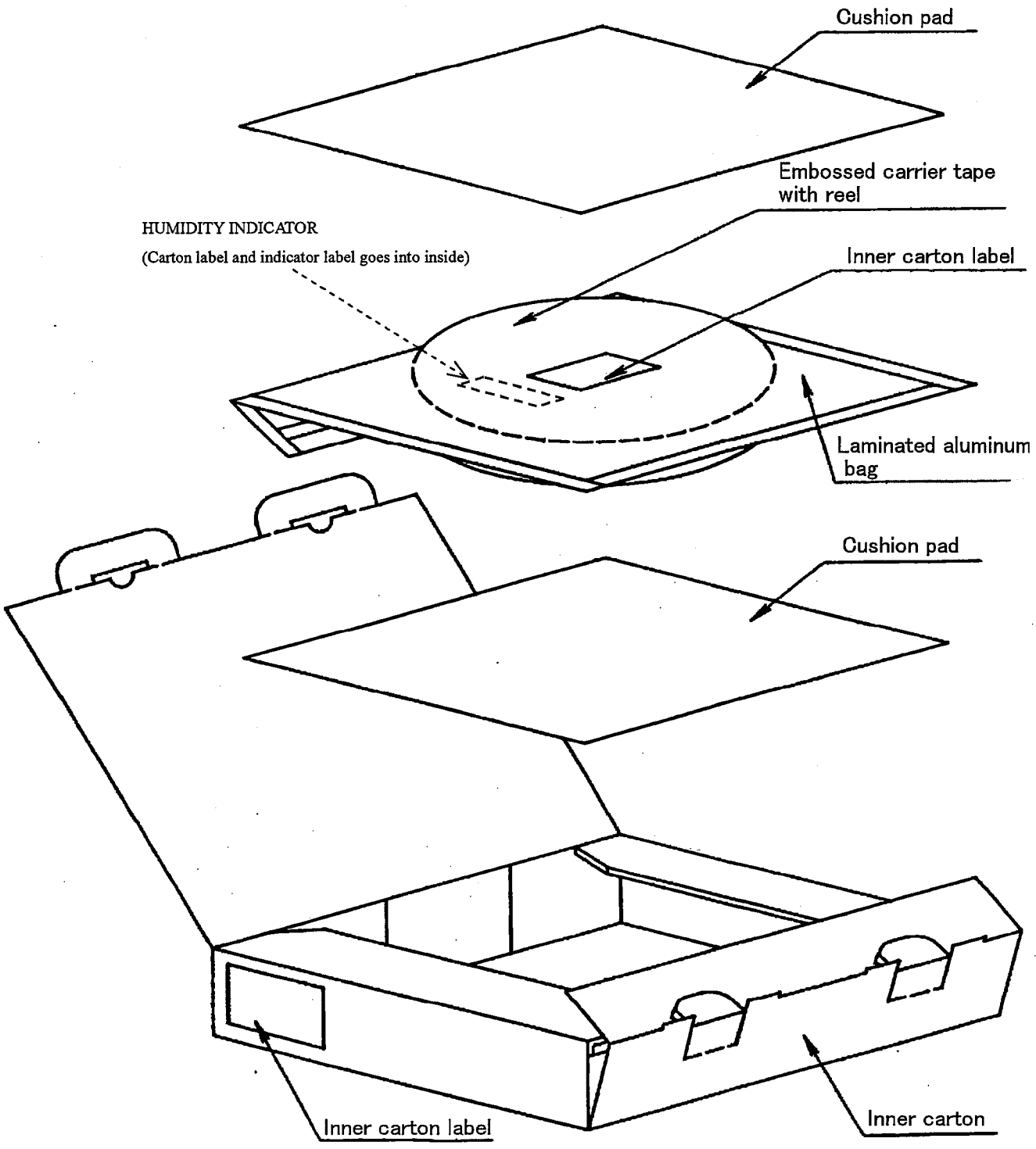
Reference





SIZE	Y	SIZE	Y
8mm	9.5	32mm	33.5
12mm	13.5	44mm	45.5
16mm	17.5	56mm	57.5
24mm	25.5		

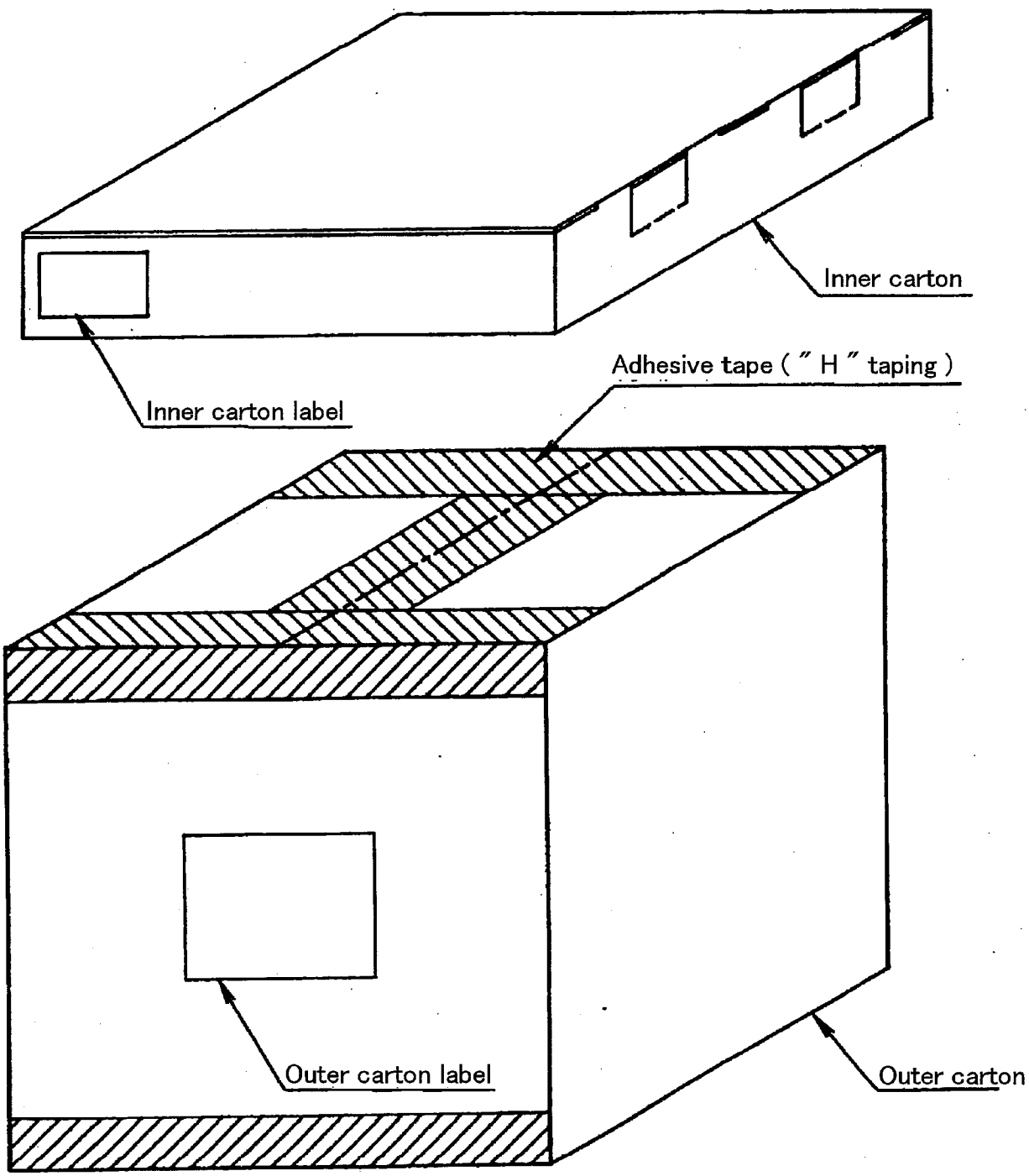
名称 NAME	Reel for embossed carrier tape		備考 NOTE
DRAWING NO.	CV755	単位 UNIT	mm



Inner carton - Outer dimensions :	L		W		H
:	345	×	345	×	55

名称 NAME	Packing specifications《1》	備考 NOTE
DRAWING NO. CV428	単位 UNIT mm	

Reference



	L		W		H
Inner carton - Outer dimensions :	345	×	345	×	55
Outer carton - Outer dimensions :	365	×	315	×	385

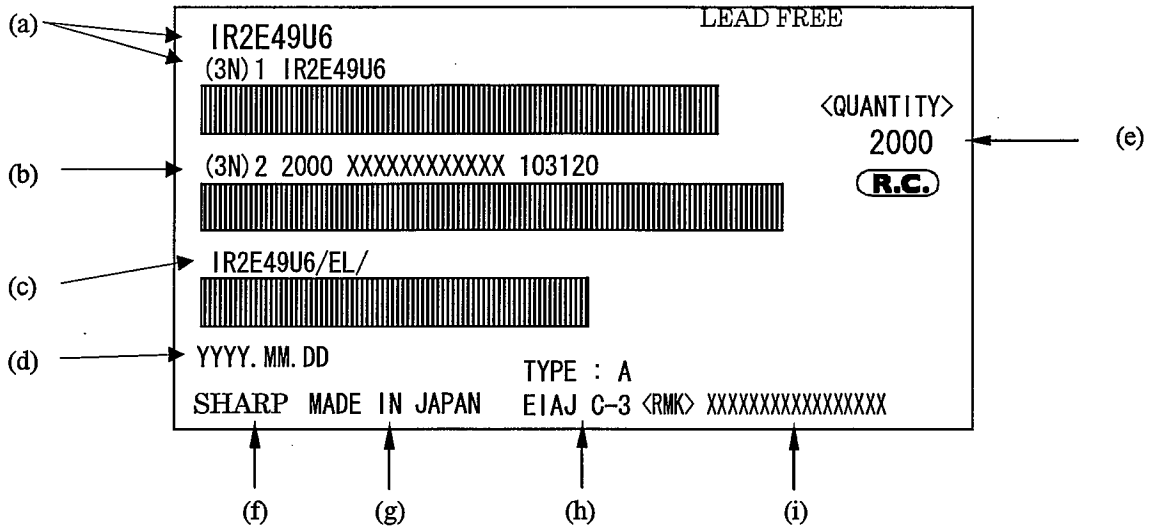
名称 NAME	Packing specifications《2》		
DRAWING NO.	BJ426	単位 UNIT	mm

備考　出荷数量が端数の場合、本仕様と異なることがあります。
NOTE There is a possibility different from this specification when the number of shipments is fractions.

*S20070206

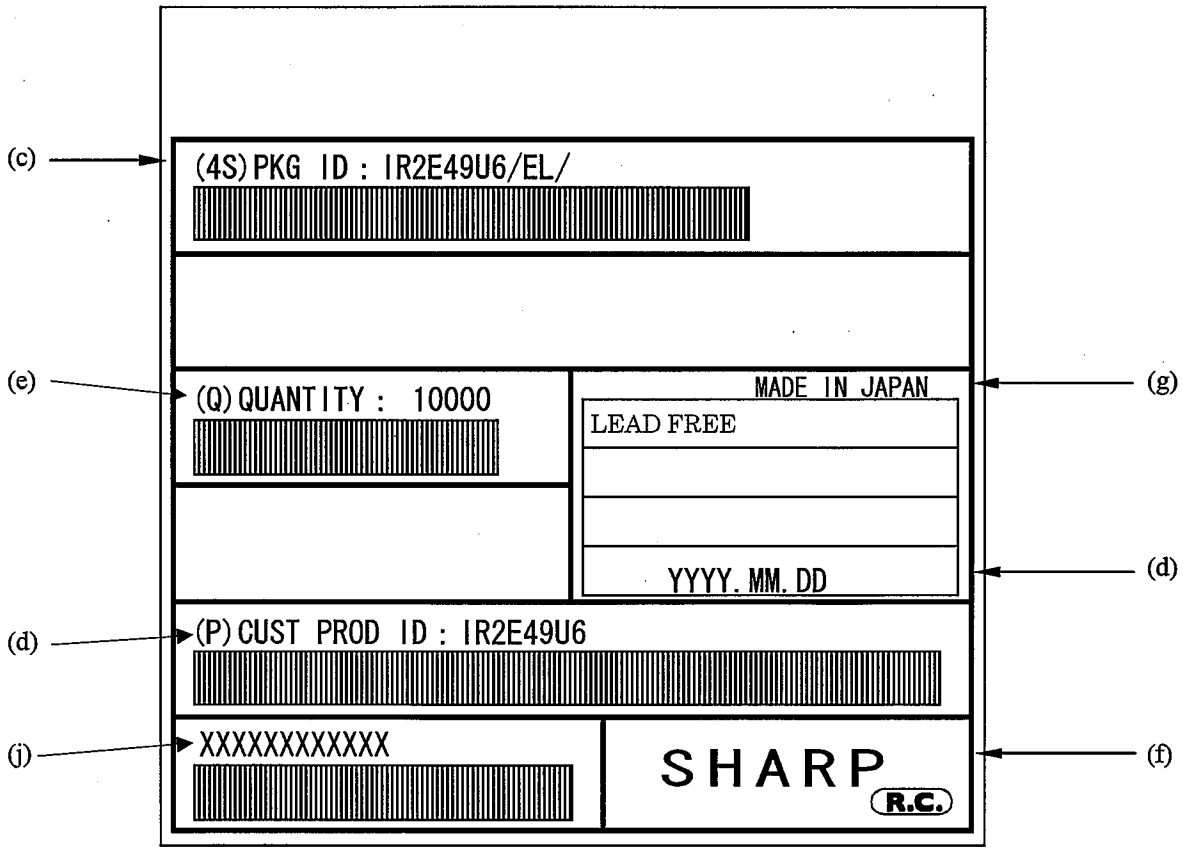
(Note) The << LEAD-FREE >> display shows a lead-free article.
"R.C." means "RoHS Compliant".

Inner carton label



Outer carton label

(Former) EIAJ B Standard conforming



(a) Product name
(b) Quantity PD lot Company code
(c) Part No. (SHARP)
(d) Packed date
(e) Quantity
(f) "SHARP" Logo
(g) The country of origin(It displays, when the country of origin is Japan.)
(h) Type name (Conformity standard)
(i) Assembly management No.
(j) Shipment lot