Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

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Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

TMC2249A

Digital Mixer

12 x 12 Bit, 60 MHz

Features

- 60 MHz input and computation rate
- Two 12-bit multipliers
- Separate data and coefficient inputs
- Independent, user-selectable pipeline delays of 1 to 16 clocks on all input ports
- Separate 16-bit input port allows cascading or addition of a constant
- User-selectable rounded output
- Internal 1/2 LSB rounding of products
- Fully registered, pipelined architecture
- Available in 120-Pin CPGA, PPGA, MPGA or MQFP

Applications

- Video switching
- Image mixing
- Digital signal modulation
- Complex frequency synthesis
- Digital filtering
- Complex arithmetic functions

Description

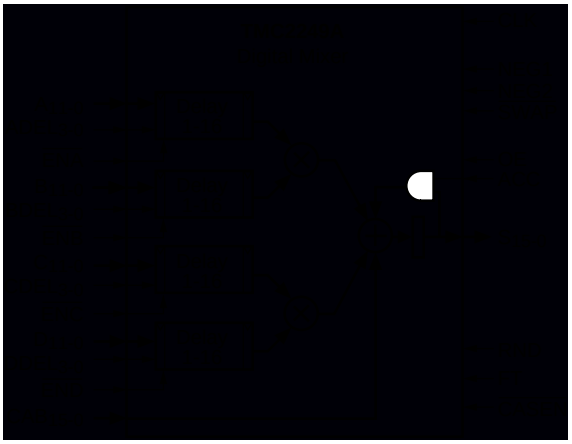
The TMC2249A is a high-speed digital arithmetic circuit consisting of two 12-bit multipliers, an adder and a cascadeable accumulator. All four multiplier inputs are simultaneously accessible to the user, and each includes a user-programmable pipeline delay of up to 16 clocks in length. The 24-bit adder/subtractor is followed by an accumulator and 16-bit input port which allows the user to cascade multiple TMC2249As. A new 16-bit accumulated output is available every clock, up to the maximum rate of 60 MHz. All inputs and outputs are registered except the three-state output enable, and all are TTL compatible.

The TMC2249A utilizes a pipelined, bus-oriented structure offering significant flexibility. Input register clock enables and programmable input data pipeline delays on each port offer an adaptable input structure for high-speed digital systems. Following the multipliers, the user may perform addition or subtraction of either product, arithmetic rounding to 16 bits, and accumulation and summation of products with a cascading input. The output port allows access to all 24 bits of the internal accumulator by switching between overlapping least and most-significant 16-bit words, and a three-state output enable simplifies connection to an external system bus.

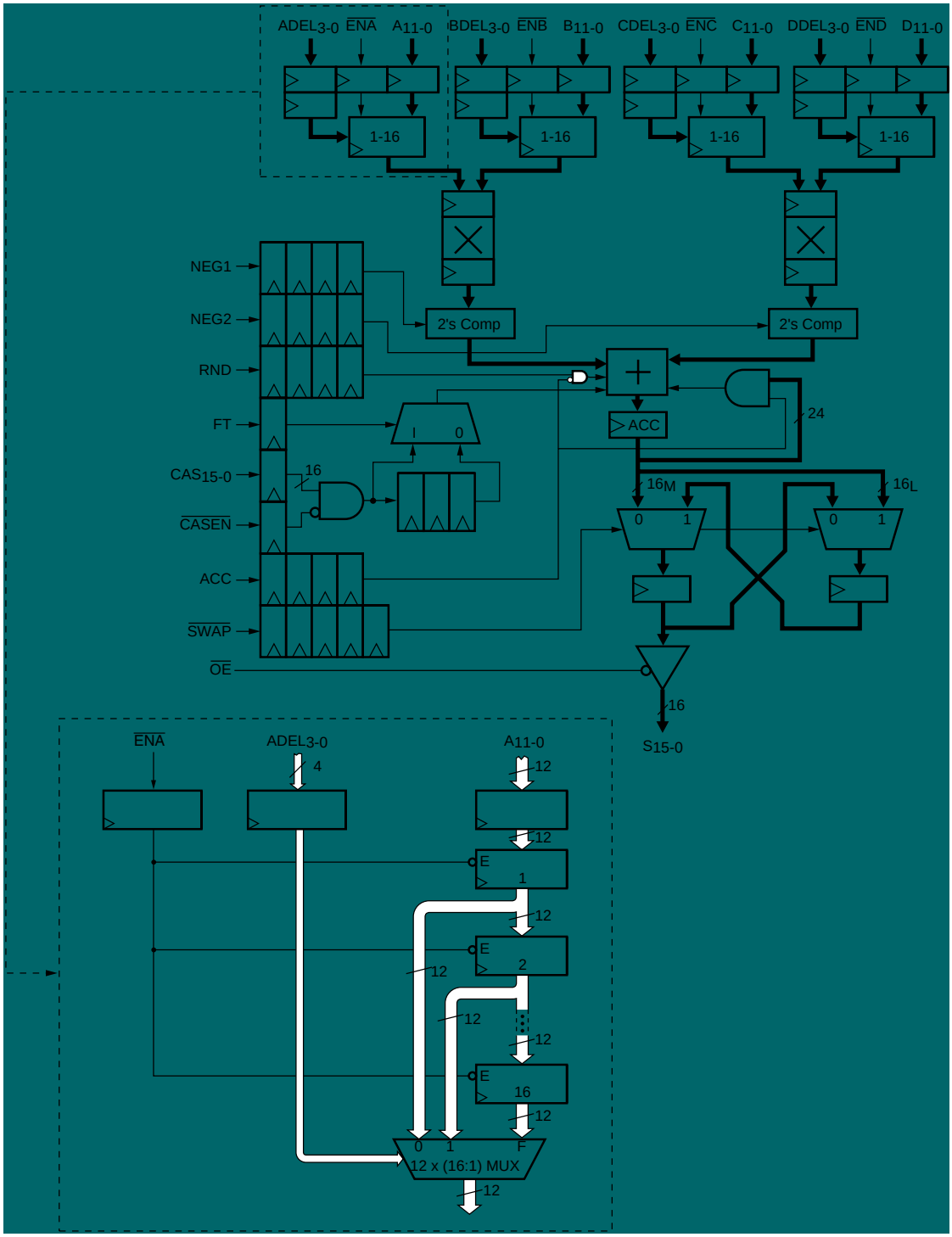
The TMC2249A has numerous applications in digital processing algorithms, from executing simple image mixing and switching, to performing complex arithmetic functions and complex waveform synthesis. FIR filters, digital quadrature mixers and modulators, and vector arithmetic functions may also be implemented with this device.

Fabricated in a submicron CMOS process, the TMC2249A operates at guaranteed clock rates of up to 60 MHz over the full temperature and supply voltage ranges. It is pin- and function-compatible with Fairchild's TMC2249, while providing higher speed operation and lower power dissipation. It is available in a 120 pin Ceramic Pin Grid Array (CPGA), 120 pin Plastic Pin Grid Array (PPGA), 120 lead MQFP to PPGA package (MPGA), and a 120 lead Metric Quad Flat-Pack (MQFP).

Logic Symbol



Block Diagram



Functional Description

The TMC2249A performs the summation of products described by the formula:

$$S(N+5) = A(N\text{-}ADEL) \times B(N\text{-}BDEL) \times (-1^{NEG1(N)}) + C(N\text{-}CDEL) \times D(N\text{-}DDEL) \times (-1^{NEG2(N)}) + CAS(N+3 \times FT)$$

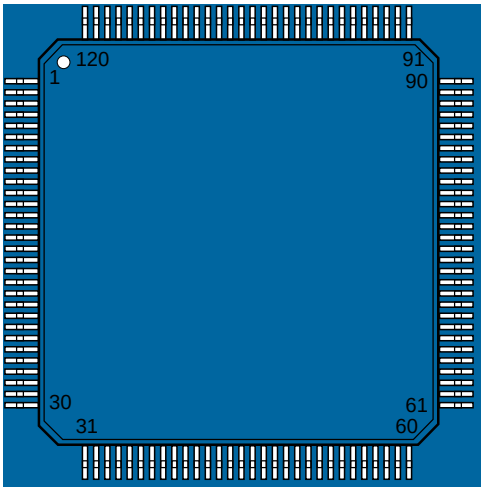
where ADEL through DDEL range from 1 to 16 pipe delays.

All inputs and controls utilize pipeline delay registers to maintain synchronicity with the data input during that clock, except when the Cascade data input is routed directly to the accumulator by use of the Feedthrough control. One-half LSB rounding to 16 bits may be performed on the sum of products while summing with the cascade input data.

The user may access either the upper or lower 16 bits of the 24-bit accumulator by swapping overlapping registers. The output bus has an asynchronous high-impedance enable, to simplify interfacing to complex systems.

Pin Assignments

120 Pin Metric Quad Flat Pack, KE Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CLK	31	$BDEL_2$	61	$ADEL_3$	91	C_1
2	ACC	32	$BDEL_3$	62	$ADEL_2$	92	C_2
3	NEG1	33	$\overline{ENB}$	63	$ADEL_1$	93	C_3
4	NEG2	34	B_0	64	$ADEL_0$	94	C_4
5	RND	35	B_1	65	NC	95	C_5
6	S_{15}	36	B_2	66	CAS_{15}	96	C_6
7	S_{14}	37	B_3	67	CAS_{14}	97	C_7
8	GND	38	B_4	68	CAS_{13}	98	C_8
9	S_{13}	39	B_5	69	CAS_{12}	99	C_9
10	S_{12}	40	B_6	70	CAS_{11}	100	C_{10}
11	S_{11}	41	B_7	71	CAS_{10}	101	C_{11}
12	V_{DD}	42	GND	72	GND	102	V_{DD}
13	S_{10}	43	B_8	73	CAS_9	103	D_{11}
14	S_9	44	B_9	74	CAS_8	104	D_{10}
15	S_8	45	B_{10}	75	CAS_7	105	D_9
16	GND	46	V_{DD}	76	CAS_6	106	GND
17	S_7	47	B_{11}	77	CAS_5	107	D_8
18	S_8	48	A_{11}	78	CAS_4	108	D_7
19	S_5	49	A_{10}	79	CAS_3	109	D_6
20	V_{DD}	50	A_9	80	CAS_2	110	D_5
21	S_4	51	A_8	81	CAS_1	111	D_4
22	S_3	52	A_7	82	CAS_0	112	D_3
23	S_2	53	A_6	83	$\overline{CASEN}$	113	D_2
24	GND	54	A_5	84	FT	114	D_1
25	S_1	55	A_4	85	$CDEL_0$	115	D_0
26	S_0	56	A_3	86	$CDEL_1$	116	$\overline{END}$
27	$\overline{OE}$	57	A_2	87	$CDEL_2$	117	$DDEL_3$
28	$\overline{SWAP}$	58	A_1	88	$CDEL_3$	118	$DDEL_2$
29	$BDEL_0$	59	A_0	89	$\overline{ENC}$	119	$DDEL_1$
30	$BDEL_1$	60	$\overline{ENA}$	90	C_0	120	$DDEL_0$

Pin Assignments

120 Pin Plastic Pin Grid Array, H5 Package, 120 Pin Ceramic Pin Grid Array, G1 Package, and 120 Pin Metric Quad FlatPack to 120 Pin Plastic Pin Array, H6 Package

Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	CPGA/PPGA/ MPGA	MQFP	
Power			
V_{DD}	F3, H3, L7, C8	12, 20, 46, 102	**Supply Voltage.** The TMC2249A operates from a single +5V supply. All power and ground pins must be connected.
GND	E3, G3, J3, L6, H11, C7	8, 16, 24, 42, 72, 106	**Ground.** The TMC2249A operates from a single +5V supply. All power and ground pins must be connected.
Clock			
CLK	C3	1	**System Clock.** The TMC2249A operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
Inputs			
A_{11-0}	N8, M8, L8, N9, M9, N10, L9, M10, N11, N12, L10, M11	48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59	**A-D Input.** A through D are the four 12-bit registered data input ports. A_0-D_0 are the LSBs (see Table 1). Data presented to the input ports is clocked in to the top of the 16-stage delay pipeline on the next clock when enabled, "pushing" data down the register stack.
B_{11-0}	N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, L4	47, 45, 44, 43, 41, 40, 39, 38, 37, 36, 35, 34	
C_{11-0}	A9, B9, A10, C9, B10, A11, B11, C10, A12, B12, C11, A13	101, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90	
D_{11-0}	B8, A8, B7, A7, A6, B6, C6, A5, B5, A4, C5, B4	103, 104, 105, 107, 108, 109, 110, 111, 112 113, 114, 115	
$ADEL_{3-0}$	L11, M12, M13, K11	61, 62, 63, 64	**A-D Delay.** ADEL through DDEL are the four-bit registered input data pipe delay select word inputs. Data to be presented to the multipliers is selected from one of sixteen stages in the input data delay pipe registers, as indicated by the delay select word presented to the respective input port during that clock. The minimum delay is one clock (select word=0000), and the maximum delay is 16 clocks (select word=1111). Following powerup these values are indeterminate and must be initialized by the user.
$BDEL_{3-0}$	M2, L3, N1, L2	32, 31, 30, 29	
$CDEL_{3-0}$	D11, B13, C13, D12	88, 87, 86, 85	
$DDEL_{3-0}$	A2, C4, B3, A1	117, 118, 119, 120	
CAS_{15-0}	L13, K12, J11, K13, J12, J13, H12, H13, G12, G11, G13, F13, F12, F11, E13, E12	66, 67, 68, 69, 70, 71, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82	**Cascade Input.** CAS is the 16-bit Cascade data input port. CAS_0 is the LSB. See Table 1.
Controls			
S_{15-0}	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	6, 7, 9, 10, 11, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 26	**Sum Output.** The current 16-bit result is available at the Sum output. The output may be the most or least significant 16 bits of the current accumulator output, as determined by $\overline{SWAP}$. S_0 is the LSB. See Table 1.

Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	CPGA/PPGA/ MPGA	MQFP	
Controls			
$\overline{ENA}$-$\overline{END}$	N13, N2, C12, A3	60, 33, 89, 116	**Input Enables.** Input data presented to port i11-0 (i=A,B,C, or D) are latched into delay pipeline i, and data already in pipeline i advance by one register position, on each rising edge of CLK for which $\overline{ENi}$ is LOW. When $\overline{ENi}$ is HIGH, the data in pipeline i do not move and the value at the input port i will be lost before it reaches the multiplier.
NEG1,2	B1, D3	3, 4	**Negate.** The products of the multipliers are negated causing a subtraction to be performed during the internal summation of products, when the NEGate controls are HIGH, NEG1 negates the product A x B, while NEG2 acts on the output of the multiplier which generates the product C x D. When the length controls ADEL–DDEL are set to zero, these controls indicate the operation to be performed on data input during the same clock. As nonzero values for ADEL–DDEL do not affect the pipelining of these controls, their effect is not synchronous with the data input in these cases.
RND	C2	5	**Round.** When the rounding control is HIGH, the 24-bit sum of products resulting from data input during that clock is rounded to 16 bits. When enabled rounding is automatically performed only during the first cycle of each accumulation sequence, to avoid the accumulation of roundoff errors.
FT	E11	84	**Feedthrough.** When the Feedthrough control is HIGH, the pipeline delay through the cascade data path is minimized to simplify the cascading of multiple devices. When FT is LOW and ADEL through DDEL are all set to 0, the data inputs are aligned, such that S(n+6) = CAS(n) + A(n)B(n) + C(n)D(n). See Table 2.
$\overline{CASEN}$	D13	83	**Cascade Enable.** Data presented at the cascade data input port are latched and accumulated internally when the input enable $\overline{CASEN}$ during that clock is LOW. When $\overline{CASEN}$ is HIGH, the cascade input port is ignored.
ACC	B2	2	**Accumulate.** When the registered ACCumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of the previous products and RND is disabled.
$\overline{SWAP}$	K3	28	**Swap Output Words.** The user may access both the most and least-significant 16 bits of the 24-bit accumulator by utilizing $\overline{SWAP}$. Normal operation of the device, with $\overline{SWAP}$ = HIGH, outputs the most significant word. Setting $\overline{SWAP}$ = LOW puts a double-register structure into "toggle" mode, allowing the user to examine the LSW on alternate clocks. New output data will not be clocked into the output registers until $\overline{SWAP}$ returns HIGH.
$\overline{OE}$	M1	27	**Output Enable.** Data currently in the output registers is available at the output bus $S_{15\text{-}0}$ when the asynchronous Output Enable is LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.
No Connect			
	L12	65	Do Not Connect
	D4		Index Pin (optional)

Table 1. Data Formats and Bit Weighting

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
				-2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	DATA (A_{11-0}-D_{11-0})
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	CASCADE INPUT (CAS_{15-0})
																SUM (S_{15-0})
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	LSW
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	MSW

Notes:

A minus sign indicates the two's complement sign bit.

RND adds 1 to the 2^{7} position if ACC is low.

Equivalent Circuits and Threshold Levels

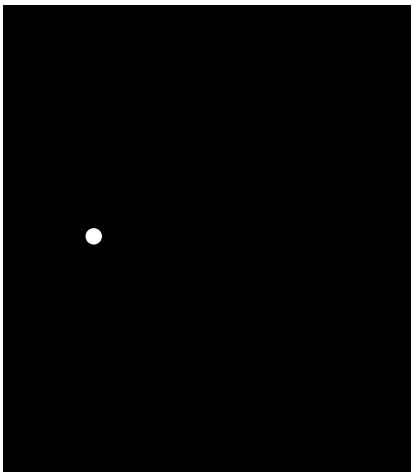


Figure 1. Equivalent Digital Input Circuit

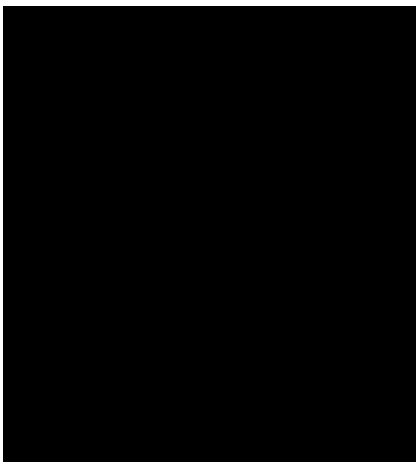


Figure 2. Equivalent Digital Output Circuit

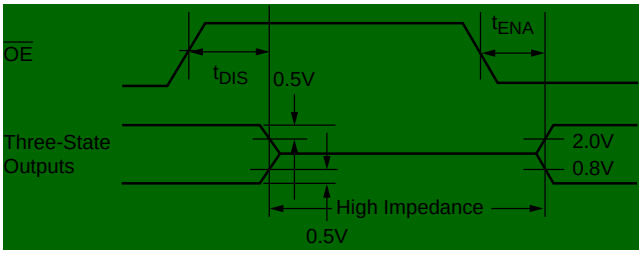


Figure 3. Threshold Levels for Three-State Measurement

Absolute Maximum Ratings (beyond which the device may be damaged)1

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD} + 0.5	V
Applied Voltage (Output) [2]	-0.5	V_{DD} + 0.5	V
Externally Forced Current (Output) [3,4]	-3.0	6.0	mA
Output Short Circuit Duration (single output in HIGH state to ground)		1	sec
Operating, Ambient Temperature	-20	110	°C
Operating, Junction Temperature		140	°C
Storage Temperature	-65	150	°C
Lead, Soldering (10 seconds)		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2249A			25	MHz
		TMC2249A-1			40	MHz
		TMC2249A-2			60	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		7			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1.5			ns
V_{IH}	Input Voltage, Logic HIGH	Data Inputs	2.0			V
		CLK Input	2.2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2249A			75	mA
		TMC2249A-1			105	mA
		TMC2249A-2			145	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK} = Max				
		TMC2249A			68	mA
		TMC2249A-1			92	mA
		TMC2249A-2			124	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0}, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions[1]	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			14	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	2.5			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			12	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			12	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.

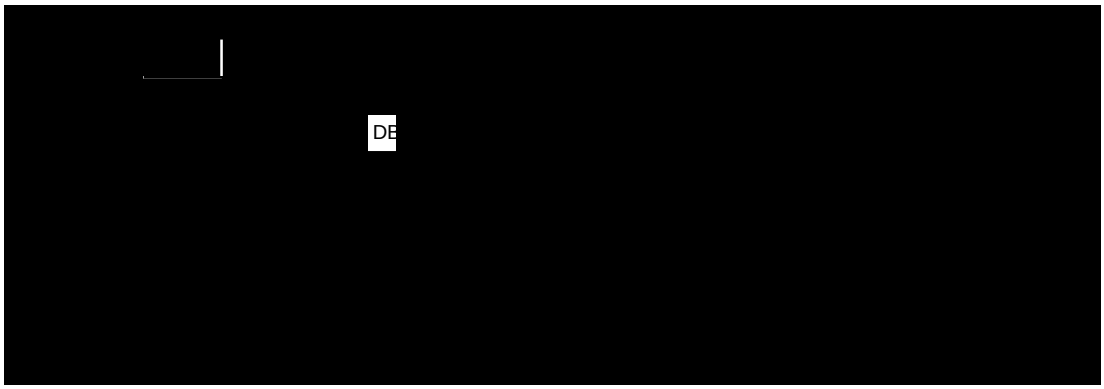


Figure 4. Timing Diagram

Application Notes

The TMC2249A is a flexible signal and image processing building block with numerous user-selectable functions which expand its usefulness. Table 2 clarifies the operation of the device, demonstrating the various feature available to the user and the timing delays incurred.

Table 2. TMC2249A Operation Sequence

CLK	ADEL	A_{11-0}	BDEL	B_{11-0}	CDEL	C_{11-0}	DDEL	D_{11-0}	NEG1	NEG2	CAS_{15-0}	FT	ACC	RND	SWAP	S_{15-0}
1	0	A(1)	0	B(1)	0	C(1)	0	D(1)	L	L	0	L	L	H	H	—
2	0	A(2)	0	B(2)	0	C(2)	0	D(2)	L	H	0	L	L	H	H	—
3	0	A(3)	0	B(3)	0	C(3)	0	D(3)	H	L	0	L	L	L	H	—
4	0	A(4)	0	B(4)	0	C(4)	0	D(4)	L	L	CAS(4)	L	L	L	H	—
5	0	A(5)	0	B(5)	0	C(5)	0	D(5)	L	L	0	L	L	L	H	—
6	0	A(6)	0	B(6)	0	C(6)	0	D(6)	L	L	0	L	L	H	H	$(A(1) \times B(1)+C(1) \times D(1)+2^7)_{ms}$
7	0	A(7)	0	B(7)	0	C(7)	0	D(7)	L	L	0	L	H	X	H	$(A(2) \times B(2)-C(2) \times D(2)+2^7)_{ms}$
8	0	A(8)	0	B(8)	0	C(8)	0	D(8)	L	L	CAS(8)	H	L	L	L	$(-A(3) \times B(3)+C(3) \times D(3))_{ms}$
9	0	A(9)	0	B(9)	0	C(9)	0	D(9)	L	L	0	L	L	H	H	$(A(4) \times B(4)+C(4) \times D(4)+CAS(4))_{ms}$
10																$(A(5) \times B(5)+C(5) \times D(5)+CAS(8))_{ms}$
11																$(A(6) \times B(6)+C(6) \times D(6)+2^7)_{ms}$
12																$(A(7) \times B(7)+C(7) \times D(7)+S(11))_{ms}$
13																$(S(12))_{ls}$
14																$(A(9) \times B(8)+C(7) \times D(6)+2^7)_{ms}$

$\overline{CASEN}$ = 0, H=HIGH, L=LOW, “ms” indicates most significant output word (bits 23-8), “ls” indicates least significant word (bits 15-0). The appropriate enables for the indicated data are assumed, otherwise ‘-’ indicates that port not enabled. Note that the output data summations including A(8)-D(8) is lost, since the output on cycle 13 is swapped to the LSW of S(12) on cycle 8. In general, RND may be left high unless the ls output is to be used, as on line 8 above.

Digital Filtering

The input structure of the TMC2249A demonstrates great versatility when all four multiplier inputs and the programmable delay registers are utilized.

Table 3 and Table 4 illlustrate how a direct-form symmetric FIR filter of up to 32 taps can be implemented. By utilizing the four input delay registers as pipelined storage banks, the user can store up to 32 coefficient-data word pairs, split into alternate "even" and "odd" halves. Two taps of the filter are calculated on each clock, and the user then increments/decrements the delay words (ADEL-DDEL). The sums of products are successively added to the global sum in the internal accumulator.

Table 3. FIR Filtering with the TMC2249A—Initial Data Loading

Register Position (Hex)	Even Data A	Odd Data C	Coefficient B	Storage D
0	x(31)	x(30)	h(0)	h(1)
1	x(29)	x(28)	h(2)	h(3)
2	x(27)	x(26)	h(4)	h(5)
3	x(25)	x(24)	h(6)	h(7)
4	x(23)	x(22)	h(8)	h(9)
5	x(21)	x(20)	h(10)	h(11)
6	x(19)	x(18)	h(12)	h(13)
7	x(17)	x(16)	h(14)	h(15)
8	x(15)	x(14)	h(15)	h(14)
9	x(13)	x(12)	h(13)	h(12)
A	x(11)	x(10)	h(11)	h(10)
B	x(9)	x(8)	h(9)	h(8)
C	x(7)	x(6)	h(7)	h(6)
D	x(5)	x(4)	h(5)	h(4)
E	x(3)	x(2)	h(3)	h(2)
F	x(1)	x(0)	h(1)	h(0)

Once all of the products of the desired taps have been summed, the result is available at the output. The user then "pushes" a new time-data sample on to the appropriate even or odd data register "stack" and reiterates the summation. Note that the coefficient bank "pointers", the BDEL and DDEL delay words, are alternately incremented and decremented on successive filter passes to maintain alignment between the incoming data samples and their respective coefficients.

The effective filter speed is calculated by dividing the clock rate by one-half the number of taps implemented.

Alternatively, non-symmetric FIR filters can be implemented using the TMC2249A in a similar fashion. Here, a shift register is used to delay the incoming data fed to the A input by an amount equal to one-half the length of the filter (the length of the A delay register).

As shown in Figure 5, the data is then sent to the C input, thus "stacking" the A and C delay registers to create a single N-tap FIR filter. The incremented delay words (ADEL-DDEL) for all four inputs are identical. Again, the filter throughput is equal to the clock speed divided by one-half the number of taps implemented.

Figure 5. Non-Symmetric 32-Tap FIR Filtering Using the TMC2249A

Table 4. FIR Filtering – Operation Sequence

Cycle	Push A	B	Push C	D	ADEL	CDEL	BDEL	DDEL	ACC	$\overline{ENA}$	$\overline{ENB}$	$\overline{ENC}$	$\overline{END}$	Convolutional Sum	Resultant Output
1	–	–	–	–	0	0	0	0	L	H	H	H	H	x(31)•h(0)+x(30)•h(1)	See Note 2
2	–	–	–	–	1	1	1	1	H	H	H	H	H	+x(29)•h(2)+x(28)•h(3)	
3	–	–	–	–	2	2	2	2	H	H	H	H	H	+x(27)•h(4)+x(26)•h(5)	
4	–	–	–	–	3	3	3	3	H	H	H	H	H	+x(25)•h(6)+x(24)•h(7)	
5	–	–	–	–	4	4	4	4	H	H	H	H	H	+x(23)•h(8)+x(22)•h(9)	
6	–	–	–	–	5	5	5	5	H	H	H	H	H	+x(21)•h(10)+x(20)•h(11)	
7	–	–	–	–	6	6	6	6	H	H	H	H	H	+x(19)•h(12)+x(18)•h(13)	
8	–	–	–	–	7	7	7	7	H	H	H	H	H	+x(17)•h(14)+x(16)•h(15)	
9	–	–	–	–	8	8	8	8	H	H	H	H	H	+x(15)•h(15)+x(14)•h(14)	
10	–	–	–	–	9	9	9	9	H	H	H	H	H	+x(13)•h(13)+x(12)•h(12)	
11	–	–	–	–	A	A	A	A	H	H	H	H	H	+x(11)•h(11)+x(10)•h(10)	
12	–	–	–	–	B	B	B	B	H	H	H	H	H	+x(9)•h(9)+x(8)•h(8)	
13	–	–	–	–	C	C	C	C	H	H	H	H	H	+x(7)•h(7)+x(6)•h(6)	
14	–	–	–	–	D	D	D	D	H	H	H	H	H	+x(5)•h(5)+x(4)•h(4)	
15	–	–	–	–	E	E	E	E	H	H	H	H	H	+x(3)•h(3)+x(2)•h(2)	
16	–	–	x(32)	–	F	F	F	F	H	H	H	L	H	+x(1)•h(1)+x(0)•h(0)	
17	–	–	–	–	0	0	F	F	H	H	H	H	H	+x(31)•h(1)+x(32)•h(0)	
18	–	–	–	–	1	1	E	E	H	H	H	H	H	+x(29)•h(3)+x(30)•h(2)	
19	–	–	–	–	2	2	D	D	H	H	H	H	H	+x(27)•h(5)+x(28)•h(4)	
20	–	–	–	–	3	3	C	C	H	H	H	H	H	+x(25)•h(7)+x(26)•h(6)	
21	–	–	–	–	4	4	B	B	H	H	H	H	H	+x(23)•h(9)+x(24)•h(8)	
•															
•															

Notes:

1. If only the 16 MSBs of the result are used, the user may leave RND HIGH and $\overline{SWAP}$ low. If the 16 LSBs or all 24 bits of the result are used, then RND should be set low.

2. $$s = \sum_{K=0}^{15} (x(k)h(k) + x(k+16)h(k))$$

Complex Arithmetic Functions

The TMC2249A can also be used to perform complex arithmetic functions. The basic function performed by the device, ignoring the delay controls,

$SUM = (\pm A \bullet B) + (\pm C \bullet D)$

can realize in two steps the familiar summation:

$(P+jR)(S+jT)=(PS-RT) + j(PT+SR)$

(1) (2)

by loading the TMC2249A as follows:

Step	TMC2249A Inputs						Resultant Output
	A	B	C	D	NEG1	NEG2	
1	P	S	R	T	L	H	(PS-RT)
2	P	T	R	S	L	L	(PT+SR)

where H and L indicate a logic HIGH and LOW.

Thus we can perform a complex multiplication in two clock cycles. Notice that the user must switch the two components of the second input vector between the B and D inputs to obtain the second complex summation.

Calculating a Butterfly

Taking advantage of the complex multiply which we implemented above using the TMC2249A, we can expand slightly to calculate a Radix-2 Butterfly, the core of the Fast Fourier Transform algorithm. To review, the Butterfly is calculated as shown in Figure 6.

Figure 6. Signal Flow of Radix-2 Butterfly

Where

$X=A+B(W_N^r)$

$Y=A–B(W_N^r)$,

and W_N^r is the complex phase coefficient, or "twiddle factor" for the N-point transform, which is:

$$W_N^r = e^{j(2\pi/N)} = \cos(2\pi/N) + j(\sin(2\pi/N)) = Re(W) + jIm(W)$$

with Re and Im indicating the real and imaginary parts of the vector.

Expanding the complex vectors A and B to calculate X and Y, we get:

X = (Re(A)+jlm(A))+(Re(B)Re(W)-lm(B)lm(W)+j(Re(B)lm(W)+lm(B)Re(W)))

= (Re(A)+Re(B)Re(W)-lm(B)lm(W))+j(lm(A)+Re(B)lm(W)+lm(B)Re(W))

= Re(X)+jlm(X)

and,

Y = (Re(A)+jlm(A))-(Re(B)Re(W)-lm(B)lm(W)+j(Re(B)lm(W)+lm(B)Re(W)))

= (Re(A)-Re(B)Re(W)+lm(B)lm(W))+j(lm(A)-Re(B)lm(W)-lm(B)Re(W))

= Re(Y)+jlm(Y)

The butterfly is then neatly implemented in four clocks, as follows:

Step	TMC2249A Inputs							Resultant Output
	A	B	C	D	CAS Input	NEG1	NEG2	
1	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	L	H	Re(X)
2	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	H	L	Re(Y)
3	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	L	L	Im(X)
4	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	H	H	Im(Y)

Notice again that the components of the second vector must be switched by the user on the second half of the computation, as well as the parts of the vector presented to the cascade input.

Quadrature Modulation

The TMC2249A can also be used to advantage as a digital-domain complex frequency synthesizer, as demonstrated in Figure 7.

Here, orthogonal sinusoidal waveforms are generated digitally in the TMC2330A Coordinate Transformer. These quadrature phase coefficients are then multiplied with two input signals, such as digitized analog data.

The TMC2249A then adds these products, which can be output directly to a high-speed digital-to-analog converter such as the Fairchild TDC1012 for direct waveform synthesis. This 12-bit, 20MHz DAC is ideally suited to waveform generation, featuring extremely low glitch energy for low spurious harmonics and distortion.

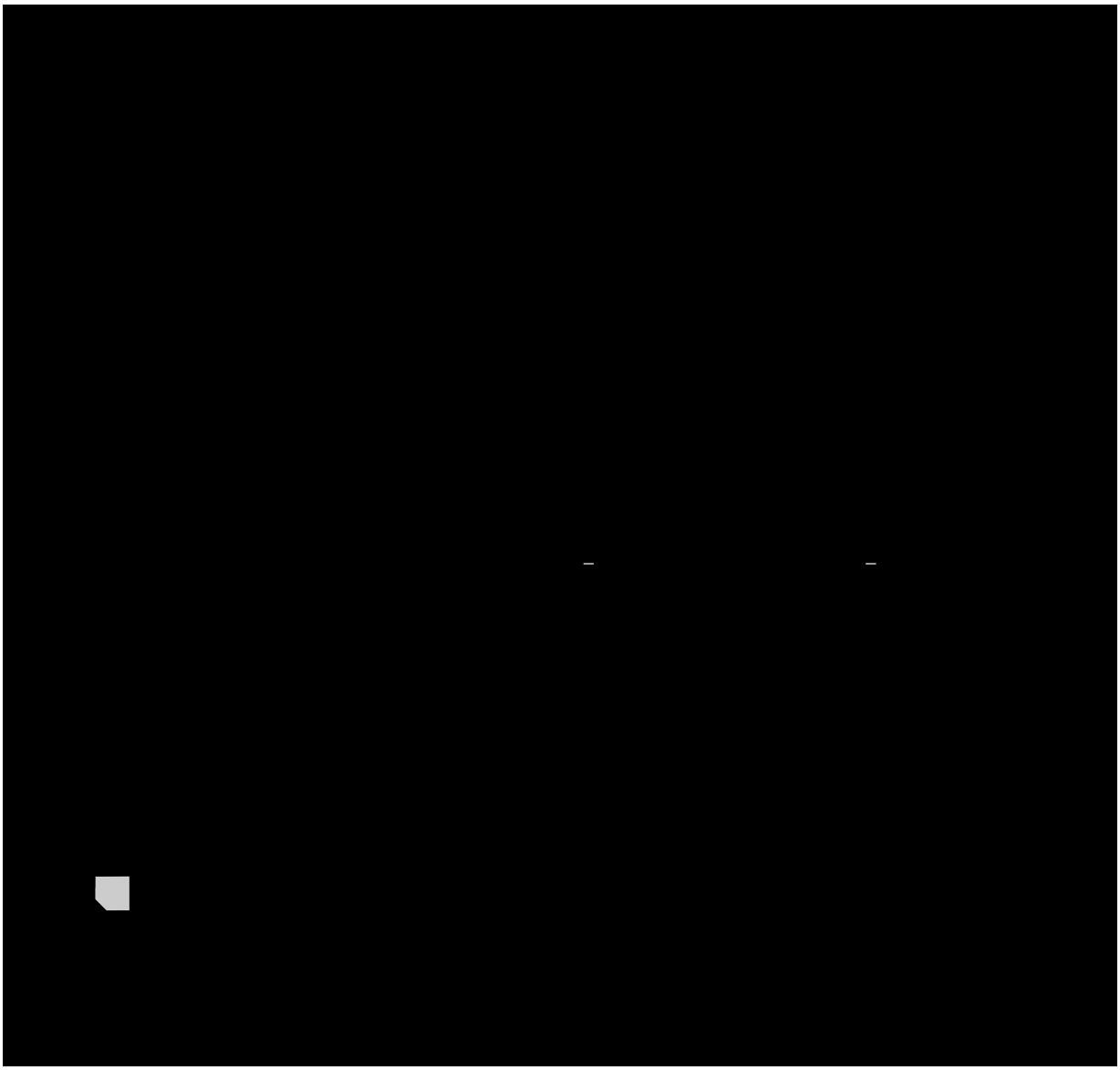
Figure 7. Direct Quadrature Waveform Synthesizer using the TMC2249A and TMC2330A

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302A Image Manipulation Sequencer
- TMC2246A Image Filter
- TMC2242B Half–Band Filter

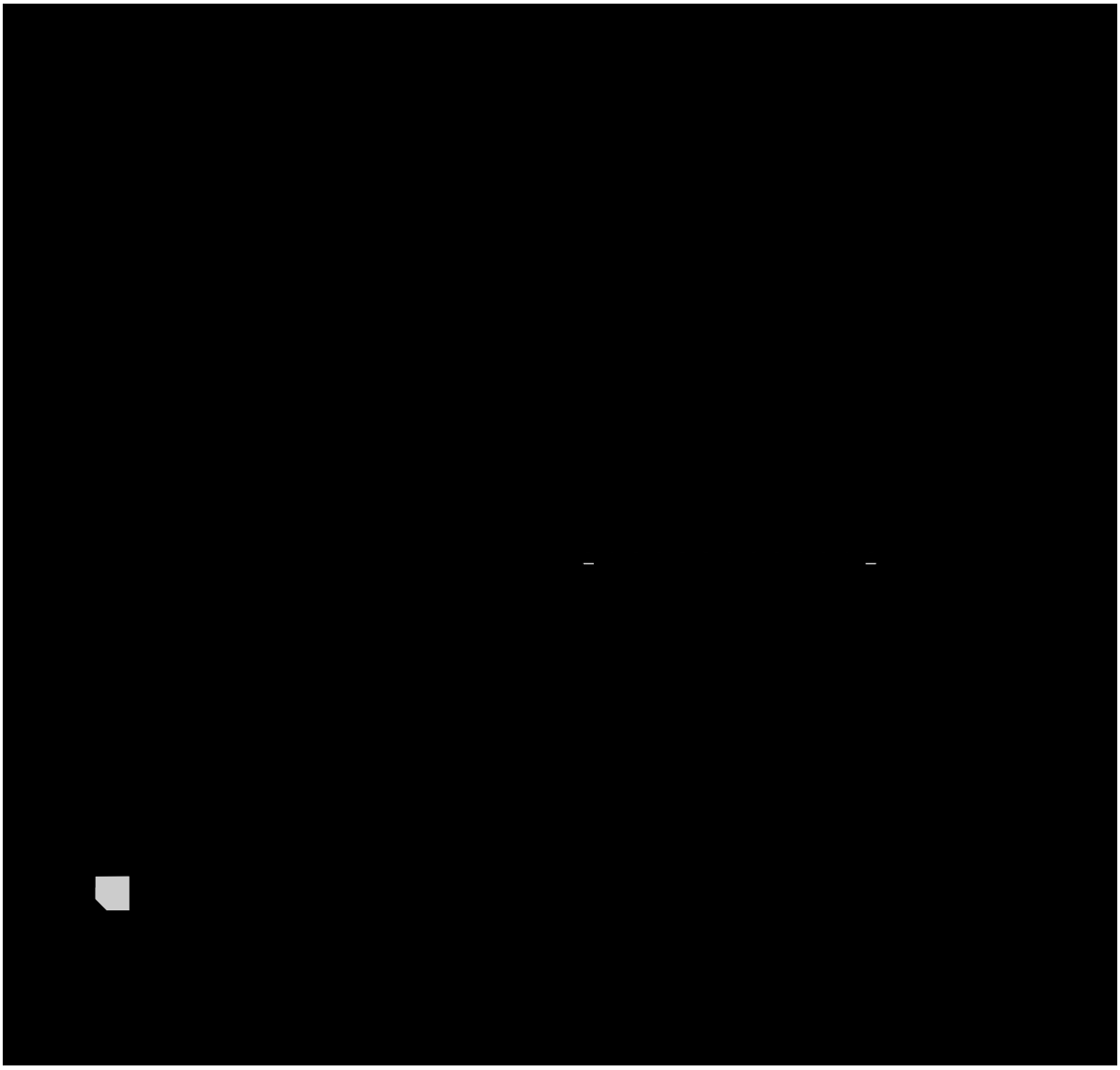
Mechanical Dimensions

120-Lead CPGA Package



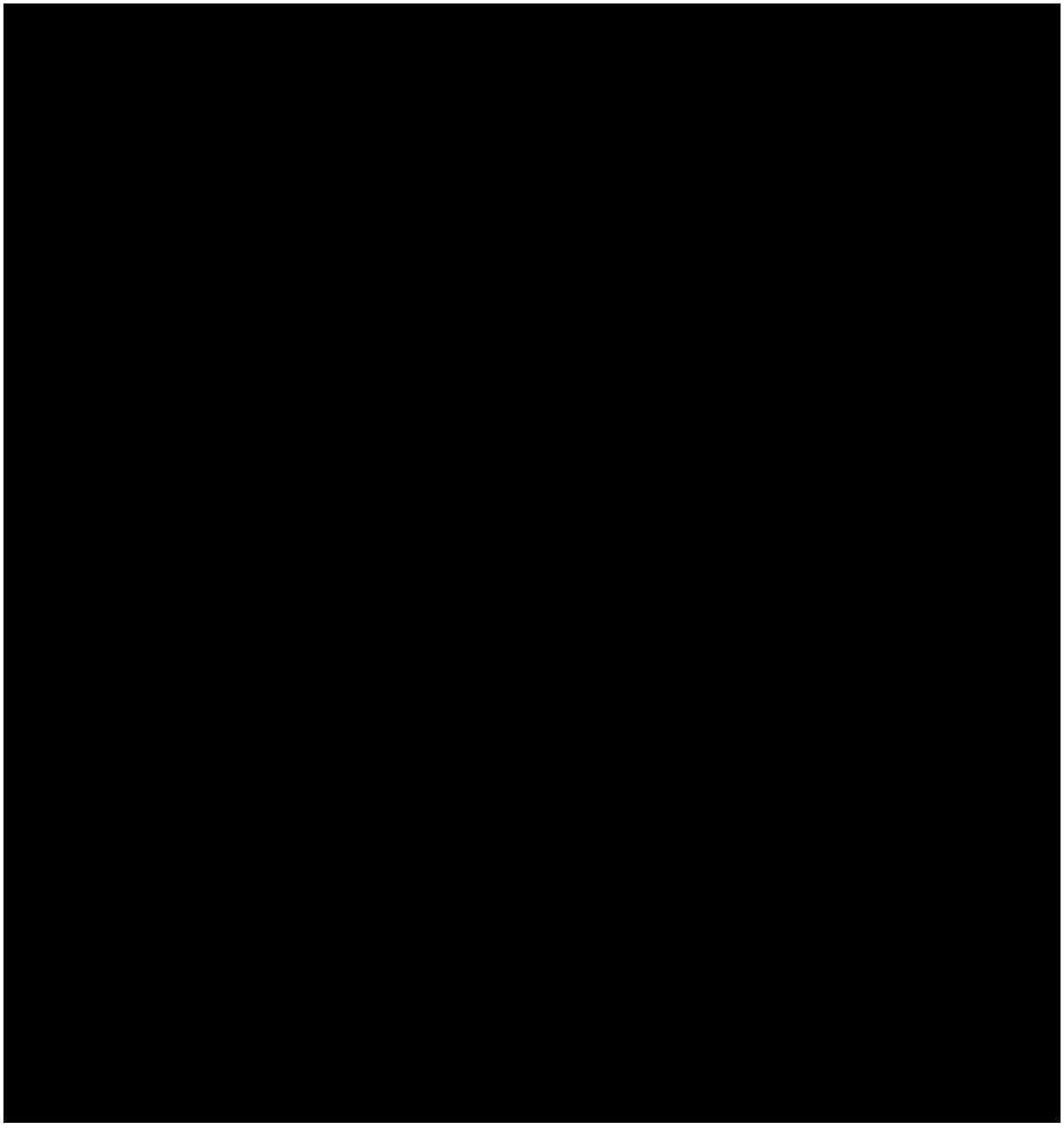
Mechanical Dimensions

120-Lead PPGA Package



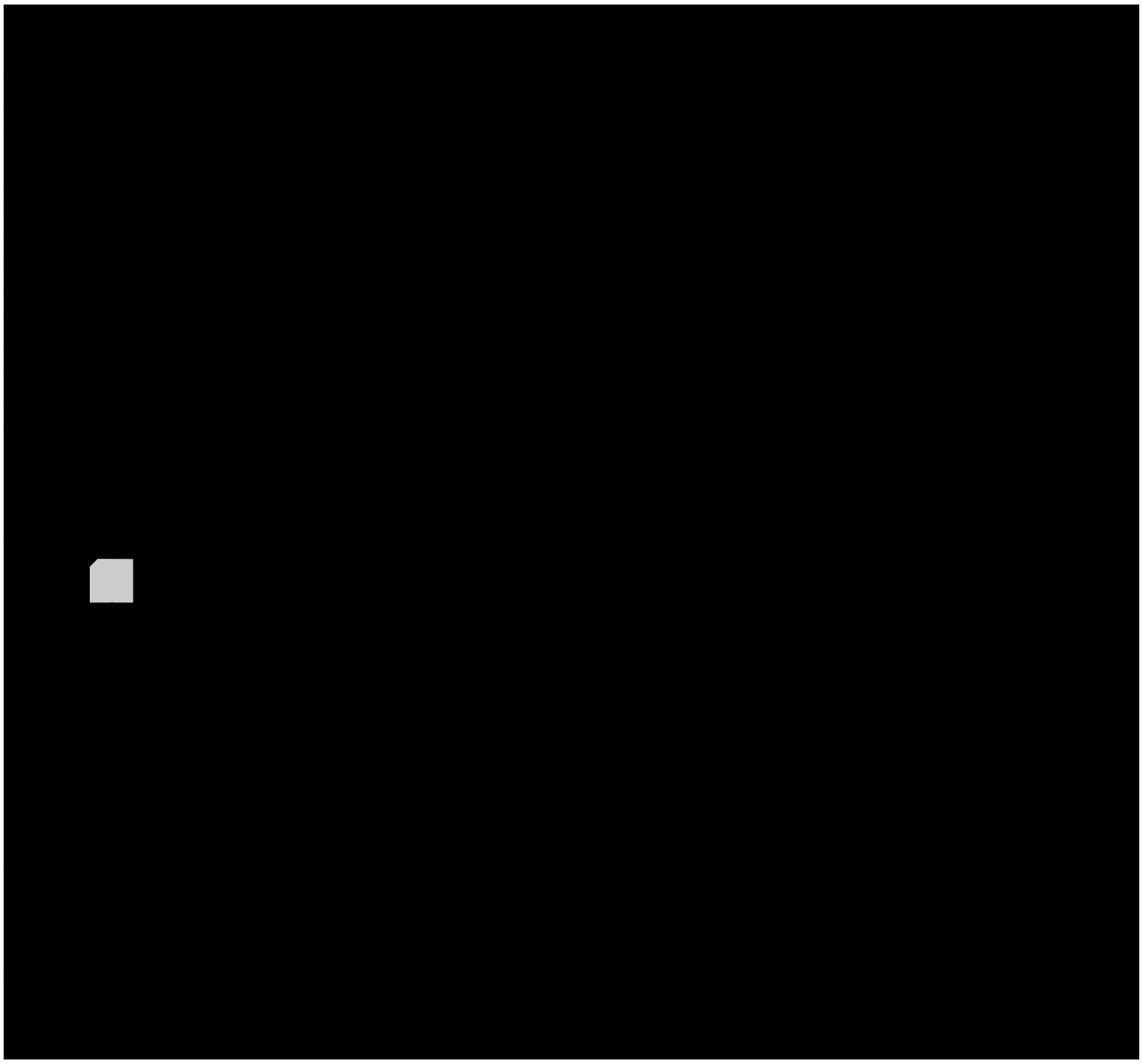
Mechanical Dimensions

120-Lead Metric Quad Flat Package to Pin Grid Array Package (MPGA)



Mechanical Dimensions

120-Lead MQFP Package



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2249AG1C	0°C to 70°C	25 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2249AG1C
TMC2249AG1C1	0°C to 70°C	40 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2249AG1C1
TMC2249AG1C2	0°C to 70°C	60 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2249AG1C2
TMC2249AH5C	0°C to 70°C	25 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C
TMC2249AH5C1	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C1
TMC2249AH5C2	0°C to 70°C	60 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C2
TMC2249AH6C	0°C to 70°C	25 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2249AH6C1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2249AH6C2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2249AKEC	0°C to 70°C	25 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC
TMC2249AKEC1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC1
TMC2249AKEC2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC2