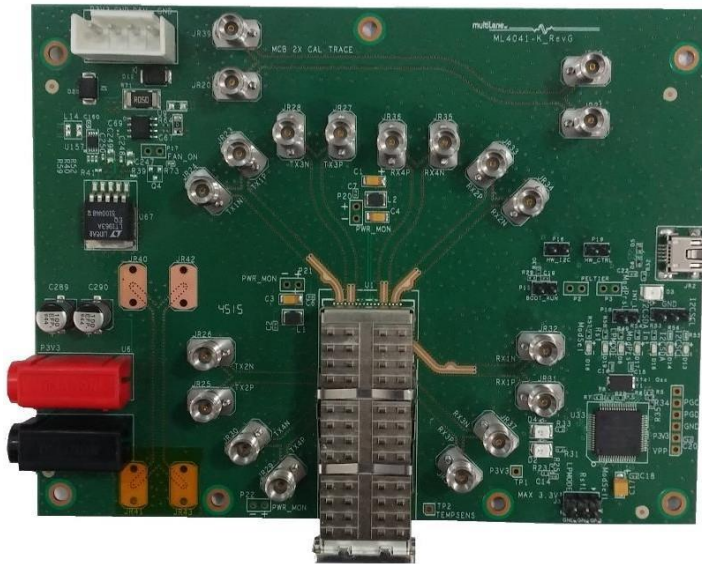
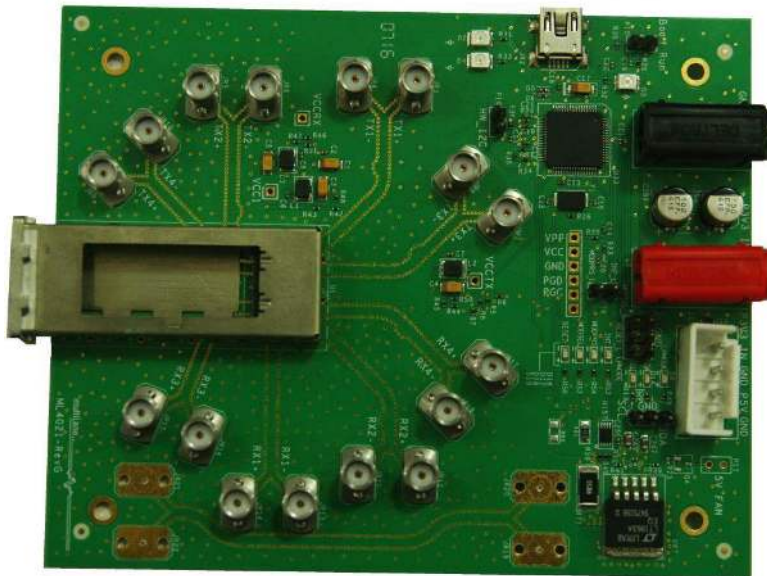


QSFP+/QSFP28 Fully MSA Compliant Master Host User Manual



ML4041K-QSFP28 Host



ML4021-QSFP+ Host

Table of contents

1.	Operating conditions	5
2.	LED indicators	5
2.1	Bootloader	5
3.	QSFP HW Signaling Pins	5
4.	Operating the QSFP28/QSFP+ host	8
4.1	Installing the GUI	8
4.2	Operating the QSFP28/QSFP+ host.....	8
5.	Communication Window	8
6.	Graphical User Interface sections.....	9
6.1	Monitor	10
6.2	Interrupt Masks	15
6.3	Controls	19
6.3.1	Rate Select	19
6.3.2	Output Disable	20
6.3.3	Squelch Disable	20
6.3.4	Power Control	20
6.3.5	Optional Channel Control	23
6.4	Identification	25
6.5	Options Available	28
6.6	Load/Save	28
		6.7 AOC 29
		6.8 DVT 30
7.	AOC VS normal mode	30
7.1	Operation in normal mode.....	30
7.2	Operation in AOC mode	32

List of Figures

Figure 1: Communication Window: Main Interface used for initial communication with host.....	8
Figure 2: Interrupt Flags, Channel Monitor page	10
Figure 3: Interrupt Masks page	15
Figure 4: Controls page	19
Figure 5: Identification page	25
Figure 6 : Options available page	28
Figure 7: Load/Save page.....	28
Figure 8: GUI_ AOC mode	29
Figure 9-DVT Tab	30
Figure 10: Normal Mode.....	31
Figure 11: AOC mode.....	32

Preface:

The following manual describes the ML4041K/ML4021 fully MSA compliant QSFP28/QSFP+ host. It addresses the following issues:

- Description of the functionalities, features and applications of the product.
- Description of the installation process.
- Detailed explanation and guidelines for using the Graphical User Interface.

1. Operating conditions

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
+3.3V power supply	Vcc	Main Supply voltage	3	3.3	3.6	V
I/O Load resistance	RI	AC-Coupled, Differential	90	100	110	Ω

2. LED indicators

The LED D3 indicates whether a USB cable is plugged or not.

The other two LEDs, D2 and D4, are used for diagnostic purposes.

- If the green LED, D2, is on: USB is locked and device is recognized by the USB driver.
- If the red LED, D4, is on: USB not connected or USB driver not found.
- If both LEDs are off: Board not powered correctly or firmware is corrupted.

2.1 Bootloader

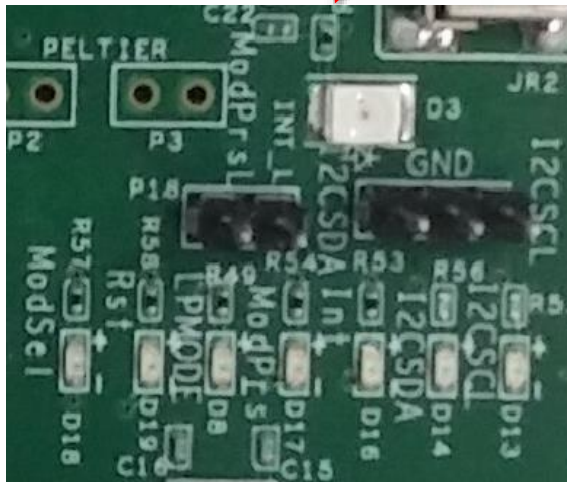
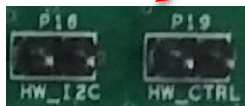
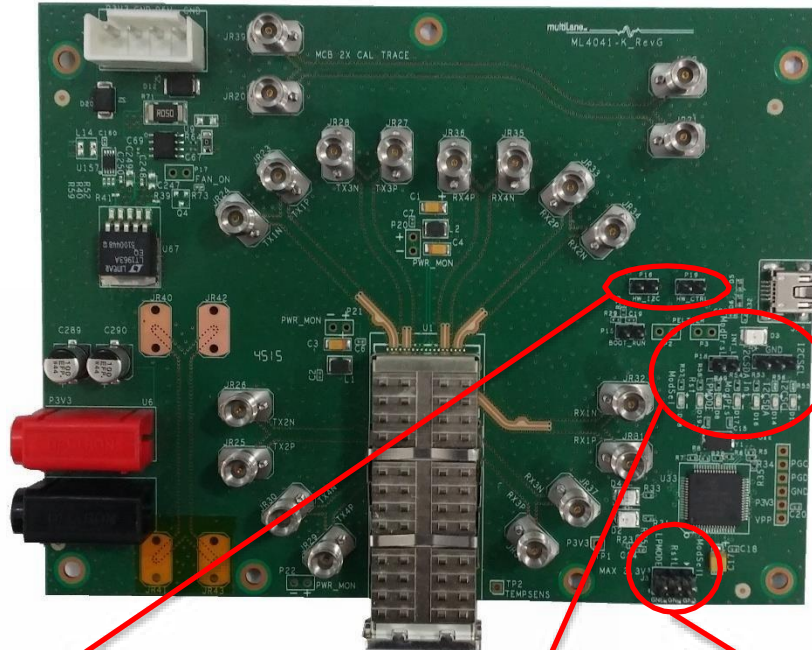
You can access the bootlaoder to reprogram the microcontroller, to do that, simply:

1. Connect a jumper on (P15) situated between the USB plug and the red power plug.
2. Connect a USB cable between the PC and Board.
3. Power up the board with a +3.3V supply.
4. LEDs (D2, D4) start blinking.
5. Remove jumper.
6. Open the software "Microchip USB HID Bootloader v2.3".
7. Click on "Open Hex File".
8. Choose the new FW to download.
9. Click on "Program/Verify".
10. Once the software finishes programming press on "Reset Device".
11. After reset the Firmware is successfully updated.

3. QSFP HW Signaling Pins

Hardware alarm pins, hardware control pins and I2C pins can be accessed from the software via USB or through on-board LEDs and pin headers. Dip switch U153 allows switching signaling pins control between software and hardware.

- A. All Hardware Alarm signals of ML4041K can be accessed through the pin headers or LEDs shown below:

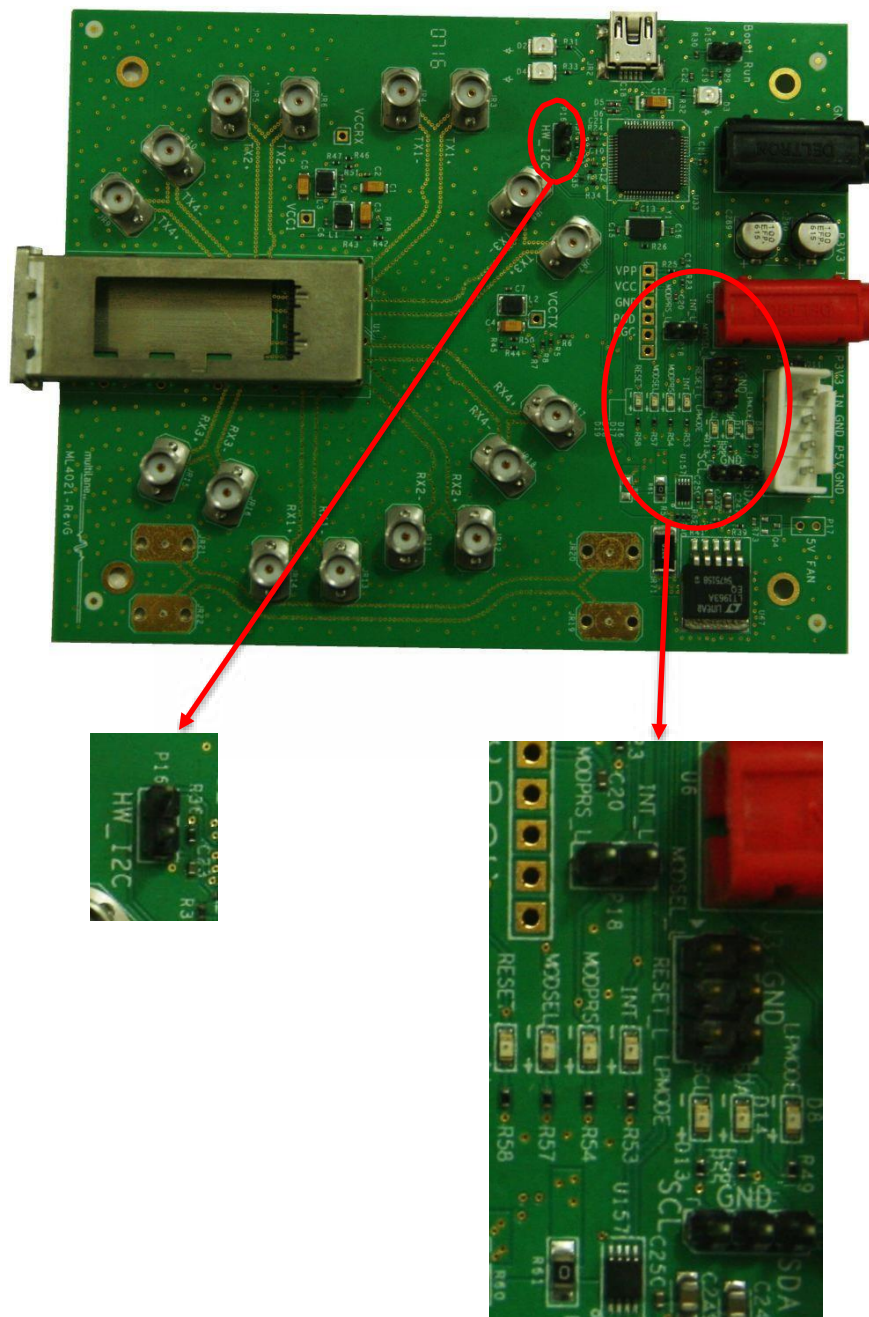


All hardware control signals can be driven through the jumpers. A jumper is placed on **P19 HW_CTRL** to be able to control hardware signals from the pins.

- ✚ ModSel, RstL, ModPrsL and IntL pins, when driven through jumpers, set their respective signals to 0, and their respective LEDs are on.
- ✚ LPMODE pin, when driven through a jumper set its signal to 0, and its LED is off.

To control I2C, a jumper is placed on **P16 HW_I2C**. Then the external I2C is driven through I2CSCL and I2CSDA pins.

B. All Hardware Alarm signals of ML4021 can be accessed through the pin headers or LEDs shown below:



All hardware control signals can be driven through the jumpers.

- ✚ RESET_L, MODSEL_L, MODPRS_L, INT_L pins, when driven through jumpers, set their respective signals to 0, and their respective LEDs are on.
- ✚ LPMODE pin, when driven through a jumper set its signal to 0, and its LED is off.

To control I2C, a jumper is placed on **P16 HW_I2C**. Then the external I2C is driven through SCL and SDA pins.

4. Operating the QSFP28/QSFP+ host

4.1 Installing the GUI

To install the GUI, simply double click on the installer provided with the board and follow the instructions.

4.2 Operating the QSFP28/QSFP+ host

To operate the QSFP28/QSFP+ host, follow the following steps:

- Place the host as to see the Multilane logo on top.
- Plug the host to a 3.3 V power supply.
- Plug the host to your computer using the USB plug.
- Hold the QSFP28/ QSFP+ module as to see the Multilane logo on top.
- Carefully slide the module into the host’s connector until the module and host are fully connected together.
- Run the GUI on your computer.

Note: Before unplugging the host from your computer, you should disconnect it from the GUI first.

5. Communication Window

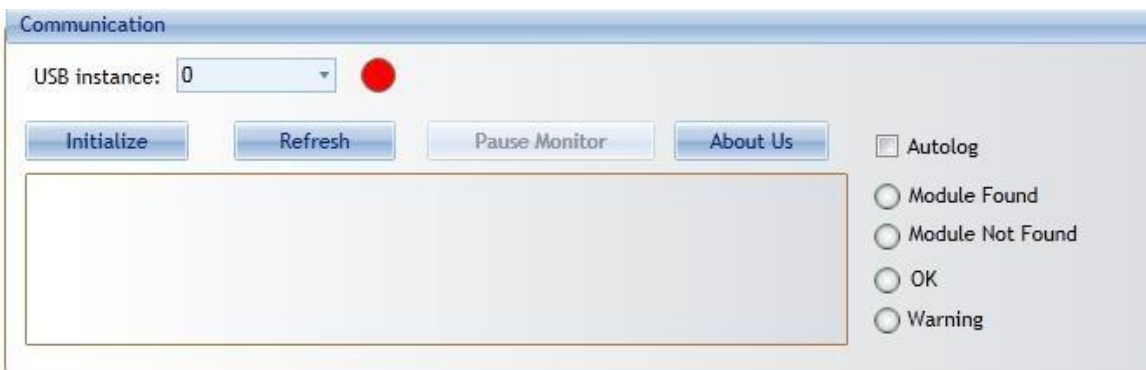


Figure 1: Communication Window: Main Interface used for initial communication with host.

The communication window is the first window to appear when you run the GUI.

The Initialize button is the application’s main entry point, used to establish a connection with the QSFP28 Host board and the Module. Once a USB connection is established, the Host checks if a QSFP28 Module is inserted, and accordingly illuminates the corresponding (Module Found or Module Not Found) LED. If a

QSFP28 Module is inserted, the initialization process proceeds with checking the related Hardware pins to ensure that the module is selected and ready to communicate with host.

You can check the “Autolog” check box for activating the silent logging mode. In this mode, a log file will be automatically generated, and all software steps will be logged during runtime. This is useful for debugging purposes when communicating with Multilane applications engineering support.

Note that multiple boards can be connected via USB. The desired board is selected using *USB Instance* field from the *Communication* window.

Refresh button: Checks for connection status, refresh Hardware Readings and updates GUI.

Pause Monitor button: Pause/Resume monitoring.

About Us button: Shows program information (name, version) and company information.

6. Graphical User Interface sections

The QSFP+ Host GUI contains the following sections:

- Monitor
- Interrupt Masks
- Controls
- Identification
- Options Available
- Load/Save
- AOC
- Read/Write Byte

We will be describing the functionality and MSA memory mapping for each of the below sections in the rest of this document.

6.1 Monitor

The Monitor tab in the QSFP Host GUI shows the digital diagnostic monitoring flags statuses.

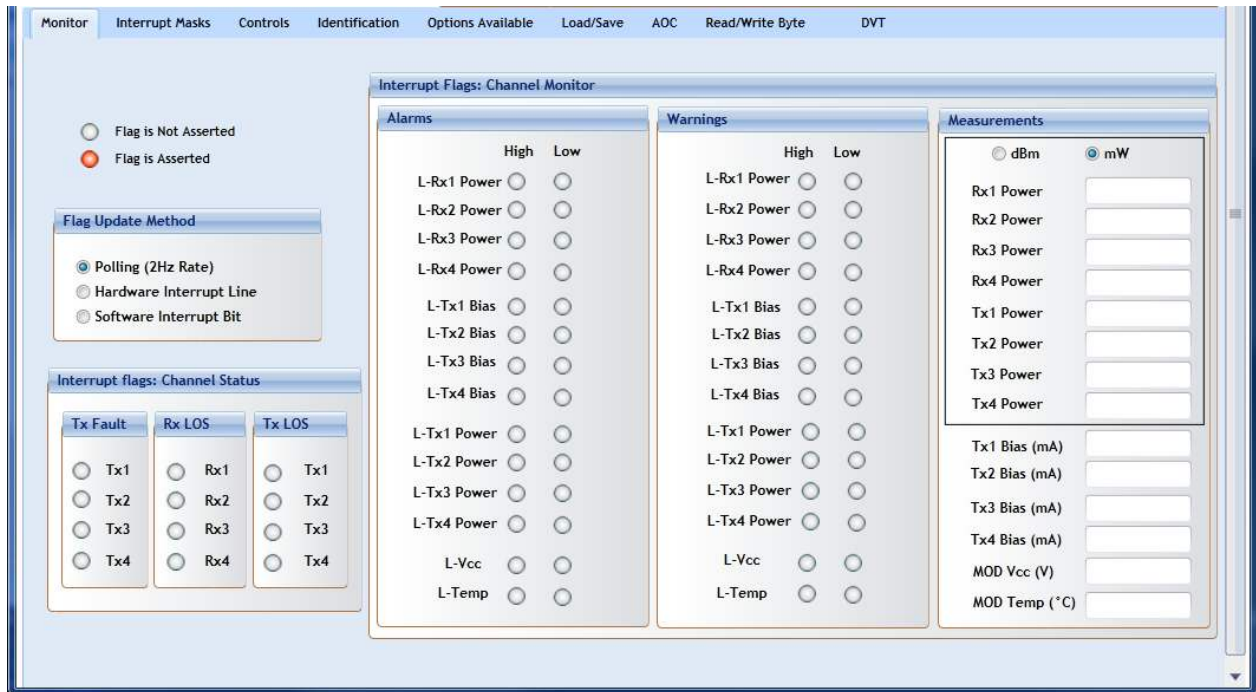


Figure 2: Interrupt Flags, Channel Monitor page

All alarms and warnings are expressed with LEDs as shown in Figure 3, when a flag is asserted the corresponding LED turns ON (becomes red), when not asserted the LED remains transparent.

The Measurements tab shows the A/D monitoring bytes values, two monitors are specified:

- 1- Module Monitors:
 - Internally measured transceiver temperature in degree Celsius.
 - Internally measured transceiver supply voltage in Volts.
- 2- Channel Monitors:
 - Measured TX bias current in mA.
 - Measured RX received optical power in mW.

The following table shows the MSA memory mapping for the monitoring tab objects.

Monitor Tab			
Interrupt Flags: Channel Status			
Channel Status Interrupt Flags (Lower Memory Map)			
Data Address	Name of Field	Default Value	Note and additional description
4 Bit 0	L-TX1 Fault	Status	Latched TX fault indicator, channel 1
4 Bit 1	L-TX2 Fault	Status	Latched TX fault indicator, channel 2
4 Bit 2	L-TX3 Fault	Status	Latched TX fault indicator, channel 3
4 Bit 3	L-TX4 Fault	Status	Latched TX fault indicator, channel 4
3 Bit 0	L-RX1 LOS	Status	Latched RX LOS indicator, channel 1
3 Bit 1	L-RX2 LOS	Status	Latched RX LOS indicator, channel 2
3 Bit 2	L-RX3 LOS	Status	Latched RX LOS indicator, channel 3
3 Bit 3	L-RX4 LOS	Status	Latched RX LOS indicator, channel 4
3 Bit 4	L-TX1 LOS	Status	Latched TX LOS indicator, channel 1 (Optional)
3 Bit 5	L-TX2 LOS	Status	Latched TX LOS indicator, channel 2 (Optional)
3 Bit 6	L-TX3 LOS	Status	Latched TX LOS indicator, channel 3 (Optional)
3 Bit 7	L-TX4 LOS	Status	Latched TX LOS indicator, channel 4 (Optional)
Interrupt Flags: Channel Monitor			
Alarms			
Channel Monitor Interrupt Flags (Lower Memory Map)			
Data Address	Name of Field	Note and additional description	
9 Bit 7	L-Rx1 Power High Alarm	Latched high RX power alarm, channel 1	
9 Bit 6	L-Rx1 Power Low Alarm	Latched low RX power alarm, channel 1	
9 Bit 3	L-Rx2 Power High Alarm	Latched high RX power alarm, channel 2	
9 Bit 2	L-Rx2 Power Low Alarm	Latched low RX power alarm, channel 2	
10 Bit 7	L-Rx3 Power High Alarm	Latched high RX power alarm, channel 3	
10 Bit 6	L-Rx3 Power Low Alarm	Latched low RX power alarm, channel 3	
10 Bit 3	L-Rx4 Power High Alarm	Latched high RX power alarm, channel 4	
10 Bit 2	L-Rx4 Power Low Alarm	Latched low RX power alarm, channel 4	
11 Bit 7	L-Tx1 Bias High Alarm	Latched high TX bias alarm, channel 1	

11 Bit 6	L-Tx1 Bias Low Alarm	Latched low TX bias alarm, channel 1
11 Bit 3	L-Tx2 Bias High Alarm	Latched high TX bias alarm, channel 2
11 Bit 2	L-Tx2 Bias Low Alarm	Latched low TX bias alarm, channel 2
12 Bit 7	L-Tx3 Bias High Alarm	Latched high TX bias alarm, channel 3
12 Bit 6	L-Tx3 Bias Low Alarm	Latched low TX bias alarm, channel 3
12 Bit 3	L-Tx4 Bias High Alarm	Latched high TX bias alarm, channel 4
12 Bit 2	L-Tx4 Bias Low Alarm	Latched low TX bias alarm, channel 4
13 Bit 7	L-Tx1 Power High Alarm	Latched high TX power alarm, channel 1
13 Bit 6	L-Tx1 Power High Alarm	Latched low TX power alarm, channel 1
13 Bit 3	L-Tx2 Power High Alarm	Latched high TX power alarm, channel 2
13 Bit 2	L-Tx2 Power High Alarm	Latched low TX power alarm, channel 2
14 Bit 7	L-Tx3 Power High Alarm	Latched high TX power alarm, channel 3
14 Bit 6	L-Tx3 Power High Alarm	Latched low TX power alarm, channel 3
14 Bit 3	L-Tx4 Power High Alarm	Latched high TX power alarm, channel 4
14 Bit 2	L-Tx4 Power High Alarm	Latched low TX power alarm, channel 4
Module Monitor Interrupt Flags (Lower Memory Map)		
7 Bit 7	L-Vcc High Alarm	Latched high supply voltage alarm
7 Bit 6	L-Temp Low Alarm	Latched low temperature alarm
6 Bit 7	L-Temp High Alarm	Latched high temperature alarm
6 Bit 6	L-Temp Low Alarm	Latched low temperature alarm

Warnings		
Channel Monitor Interrupt Flags (Lower Memory Map)		
9 Bit 5	L-Rx1 Power High Warning	Latched high RX power warning, channel 1
9 Bit 4	L-Rx1 Power Low Warning	Latched low RX power warning, channel 1
9 Bit 1	L-Rx2 Power High Warning	Latched high RX power warning, channel 2
9 Bit 0	L-Rx2 Power Low Warning	Latched low RX power warning, channel 2
10 Bit 5	L-Rx3 Power High Warning	Latched high RX power warning, channel 3
10 Bit 4	L-Rx3 Power Low Warning	Latched low RX power warning, channel 3
10 Bit 1	L-Rx4 Power High Warning	Latched high RX power warning, channel 4
10 Bit 0	L-Rx4 Power Low Warning	Latched low RX power warning, channel 4
11 Bit 5	L-Tx1 Bias High Warning	Latched high TX bias warning, channel 1
11 Bit 4	L-Tx1 Bias Low Warning	Latched low TX bias warning, channel 1
11 Bit 1	L-Tx2 Bias High Warning	Latched high TX bias warning, channel 2
11 Bit 0	L-Tx2 Bias Low Warning	Latched low TX bias warning, channel 2
12 Bit 5	L-Tx3 Bias High Warning	Latched high TX bias warning, channel 3
12 Bit 4	L-Tx3 Bias Low Warning	Latched low TX bias warning, channel 3
12 Bit 1	L-Tx4 Bias High Warning	Latched high TX bias warning, channel 4
12 Bit 0	L-Tx4 Bias Low Warning	Latched low TX bias warning, channel 4
13 Bit 5	L-Tx1 Power high Warning	Latched high TX Power warning, channel 1
13 Bit 4	L-Tx1 Power Low Warning	Latched low TX Power warning, channel 1
13 Bit 1	L-Tx2 Power High Warning	Latched High TX Power warning, channel 2
13 Bit 0	L-Tx2 Power Low Warning	Latched low TX Power warning, channel 2
14 Bit 5	L-Tx3 Power high Warning	Latched high TX Power warning, channel 3
14 Bit 4	L-Tx3 Power Low Warning	Latched low TX Power warning, channel 3
14 Bit 1	L-Tx4 Power High Warning	Latched High TX Power warning, channel 4
14 Bit 0	L-Tx4 Power Low Warning	Latched low TX Power warning, channel 4
Module Monitor Interrupt Flags (Lower Memory Map)		
7 Bit 5	L-Vcc High Warning	Latched high supply voltage warning
7 Bit 4	L-Vcc Low Warning	Latched low supply voltage warning

6 Bit 5	L-Temp High Warning	Latched high temperature warning
6 Bit 4	L-Temp Low Warning	Latched low temperature warning
Channel Monitor Values (Lower Memory Map)		
Data Address (All bits)	Name of Field	Note and additional description
34	Rx1 Power MSB	Measured
35	Rx1 Power LSB	Measured
36	Rx2 Power MSB	Measured
37	Rx2 Power LSB	Measured
38	Rx3 Power MSB	Measured
39	Rx3 Power LSB	Measured
40	Rx4 Power MSB	Measured
41	Rx4 Power LSB	Measured
42	Tx1 Bias MSB	Measured
43	Tx1 Bias LSB	Measured
44	Tx2 Bias MSB	Measured
45	Tx2 Bias LSB	Measured
46	Tx3 Bias MSB	Measured
47	Tx3 Bias LSB	Measured
48	Tx4 Bias MSB	Measured
49	Tx4 Bias LSB	Measured
50	Tx1 Power MSB	Measured
51	Tx1 Power LSB	Measured
52	Tx2 Power MSB	Measured
53	Tx2 Power LSB	Measured
54	Tx3 Power MSB	Measured
55	Tx3 Power LSB	Measured

56	Tx4 Power MSB	Measured	Internally measured TX Power, channel 4
57	Tx4 Power LSB	Measured	

6.2 Interrupt Masks

Masks shown in this tab are used to prevent a specified flag of generating an interrupt (IntL) when asserted and prevent continued interruption from on-going conditions.

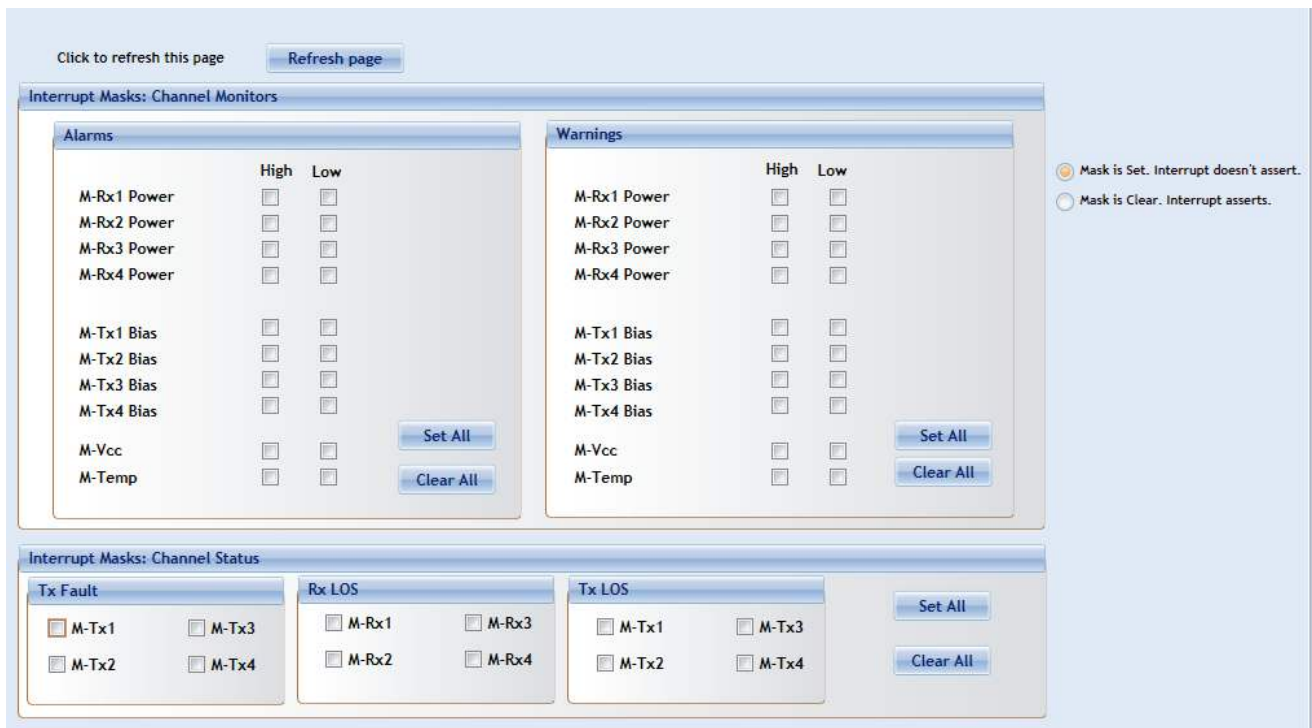


Figure 3: Interrupt Masks page

When a mask is set, an interrupt will not be asserted by the corresponding (Alarm/Warning) latched flag bit.

All Masking bits are volatile, and will be reset (set to 0) on module startup.

The table below shows the corresponding MSA mapping for the interrupt flags.

Interrupt Masks Tab		
Alarms		
Optional Channel Controls and Monitor Masks (Upper Memory, Page 03h)		
Channel Monitor Masks		
Data Address	Name of Field	Note and additional description
242	M-Rx1 Power High Alarm	Bit 7(High): Masking bit for high RX Power alarm, channel 1
	M-Rx1 Power Low Alarm	Bit 6(Low): Masking bit for low RX Power alarm, channel 1
242	M-Rx2 Power High Alarm	Bit 3(High): Masking bit for high RX Power alarm, channel 2
	M-Rx2 Power Low Alarm	Bit 2(Low): Masking bit for low RX Power alarm, channel 2
243	M-Rx3 Power High Alarm	Bit 7 (High): Masking bit for high RX Power alarm, channel 3
	M-Rx3 Power High Alarm	Bit 6(Low): Masking bit for low RX Power alarm, channel 3
243	M-Rx4 Power High Alarm	Bit 3 (High): Masking bit for high RX Power alarm, channel 4
	M-Rx4 Power Low Alarm	Bit 2(Low): Masking bit for low RX Power alarm, channel 4
244	M-Tx1 Bias High Alarm	Bit7 (High): Masking bit for high TX Bias alarm, channel 1
	M-Tx1 Bias Low Alarm	Bit 6(Low): Masking bit for low TX Bias alarm, channel 1
244	M-Tx2 Bias High Alarm	Bit3 (High): Masking bit for high TX Bias alarm, channel 2
	M-Tx2 Bias Low Alarm	Bit 2(Low): Masking bit for low TX Bias alarm, channel 2
245	M-Tx3 Bias High Alarm	Bit7 (High): Masking bit for high TX Bias alarm, channel 3
	M-Tx3 Bias Low Alarm	Bit 6(Low): Masking bit for low TX Bias alarm, channel 3
245	M-Tx4 Bias High Alarm	Bit 3(High): Masking bit for high TX Bias alarm, channel 4
	M-Tx4 Bias Low Alarm	Bit 2(Low): Masking bit for low TX Bias alarm, channel 4
IntL Masking Bits for Module and Channel Status Interrupts (Lower Memory Map)		

104	M-Vcc High Alarm	Bit 7(High): Masking bit for high Vcc alarm
	M-Vcc Low Alarm	Bit 6(Low): Masking bit for low Vcc alarm
103	M-Temp High Alarm	Bit 7(High): Masking bit for high Temperature alarm
	M-Temp Low Alarm	Bit 6(Low): Masking bit for low Temperature alarm
Warnings		
Optional Channel Controls and Monitor Masks (Upper Memory, Page 03h)		
Channel Monitor Masks		
242	M-Rx1 Power High Warning	Bit 5(High): Masking bit for high RX Power warning, channel 1
	M-Rx1 Power Low Warning	Bit 4(Low): Masking bit for low RX Power warning, channel 1
242	M-Rx2 Power High Warning	Bit 1(High): Masking bit for high RX Power warning, channel 2
	M-Rx2 Power Low Warning	Bit 0(Low): Masking bit for low RX Power warning, channel 2
243	M-Rx3 Power High Alarm	Bit 5 (High): Masking bit for high RX Power warning, channel 3
	M-Rx3 Power Low Alarm	Bit 4(Low): Masking bit for low RX Power warning, channel 3
243	M-Rx4 Power High Warning	Bit 1 (High): Masking bit for high RX Power warning, channel 4
	M-Rx4 Power Low Warning	Bit 0(Low): Masking bit for low RX Power warning, channel 4
244	M-Tx1 Bias High Warning	Bit 5 (High): Masking bit for high TX Bias warning, channel 1
	M-Tx1 Bias Low Warning	Bit 4(Low): Masking bit for low TX Bias warning, channel 1
244	M-Tx2 Bias High Warning	Bit 1 (High): Masking bit for high TX Bias warning, channel 2
	M-Tx2 Bias Low Warning	Bit 0(Low): Masking bit for low TX Bias warning, channel 2
245	M-Tx3 Bias High Warning	Bit 5 (High): Masking bit for high TX Bias warning, channel 3
	M-Tx3 Bias low Warning	Bit 4(Low): Masking bit for low TX Bias warning, channel 3
245	M-Tx4 Bias High Warning	Bit 1 (High): Masking bit for high TX Bias warning, channel 4
	M-Tx4 Bias Low Warning	Bit 0(Low): Masking bit for low TX Bias warning, channel 4
104	M-Vcc High Warning	Bit 5 (High): Masking bit for high Vcc warning
	M-Vcc Low Warning	Bit 4(Low): Masking bit for low Vcc warning
103	M-Temp High Warning	Bit 5 (High): Masking bit for high Temperature warning

	M-Temp Low Warning	Bit 4(Low): Masking bit for low Temperature
Interrupt Masks: Channel Status		
IntL Masking Bits for Module and Channel Status Interrupts (Lower Memory Map)		
101 Bit 0	M-Tx1 Fault	Masking bit for TX fault indicator, channel 1
101 Bit 1	M-Tx2 Fault	Masking bit for TX fault indicator, channel 2
101 Bit 2	M-Tx3 Fault	Masking bit for TX fault indicator, channel 3
101 Bit 3	M-Tx4 Fault	Masking bit for TX fault indicator, channel 4
100 Bit 0	M-Rx1 LOS	Masking bit for RX LOS indicator, channel 1
100 Bit 1	M-Rx2 LOS	Masking bit for RX LOS indicator, channel 2
100 Bit 2	M-Rx3 LOS	Masking bit for RX LOS indicator, channel 3
100 Bit 3	M-Rx4 LOS	Masking bit for RX LOS indicator, channel 4
100 Bit 4	M-Tx1 LOS	Masking bit for TX LOS indicator, channel 1
100 Bit 5	M-Tx2 LOS	Masking bit for TX LOS indicator, channel 2
100 Bit 6	M-Tx3 LOS	Masking bit for TX LOS indicator, channel 3
100 Bit 7	M-Tx4 LOS	Masking bit for TX LOS indicator, channel 4

6.3 Controls

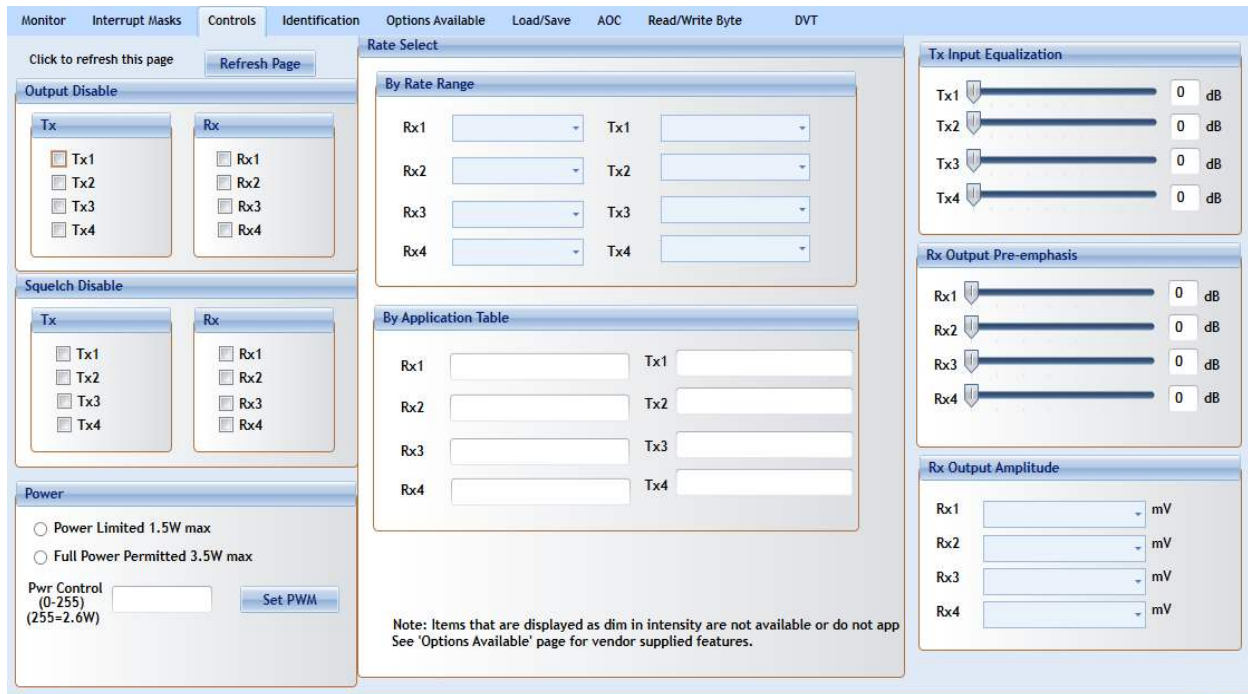


Figure 4: Controls page

6.3.1 Rate Select

Rate select is an optional control used to limit the receiver bandwidth for compatibility with multiple data rates. Rate selection also allows the transmitter to be fine-tuned for specific data rates transmissions.

The transceiver may provide:

- ✓ **No support for rate selection.**
- ✓ **Extended Rate Selection.**
- ✓ **Rate Selection Using Application Select Tables.**

xN_Rate_Select msb Value	xN_Rate_Select lsb Value	Description
0	0	Optimized for data rates less than 2.2Gb/s
0	1	Optimized for data rates from 2.2 up to 6.6Gb/s
1	0	Optimized for 6.6 Gb/s data rates and above
1	1	Reserved

The host reads the entire application select table on page 01h to determine the capabilities of the transceiver.

The host controls each channel separately by writing a Control Mode and Table Select (TS) byte to bytes 89-92 and bytes 94-97. The bits of the Rx_Application Select and the Tx_Application Select registers are defined in the below table.

7	6	5	4	3	2	1	0
Control Mode		Table Select, TS					

Control Mode defines the application control mode. Table Select selects module behavior from the Application Select Table (AST) among 63 possibilities (000000 to 111110). Note that (111111) is invalid. Default values for control mode is 0, 0 and is volatile memory.

Detailed description of Control Mode: (AST)

Bit 7	Bit 6	Function	Address 87, 88 Control	Table Select Control
0	0	Extended rate selection	lsb and msb are used according to declaration bits.	Ignored
1	Don't care	Application Select	Ignored	Field points to application

6.3.2 Output Disable

Output control functionality is optional. Output disable is controlled for each channel using byte 241 of page 03h. When the corresponding checkbox is checked, the output of the associated channel is squelched. These registers are read all “0”s on power-up.

6.3.3 Squelch Disable

Squelch control functionality is optional. Squelch disable is controlled for each channel using byte 240 of page 03h. When the corresponding checkbox is checked, the Squelch of the associated channel is disabled. These registers are read all “0”s on power-up.

6.3.4 Power Control

User can choose between two predefined power modes, allowing the module to reach different maximum power levels.

A value between 0 and 255 can be filled in the Pwr Control textbox, to customize the module power consumption relatively.

The table below shows the corresponding MSA memory mapping for the previously explained modules.

Controls Tab		
Output Disable		
Control Bytes (Lower Memory Map)		
Data Address	Name of Field	Note and additional description
86 Bit 0	Tx1_Disable	Read/write bit that allows software disable of transmitters
86 Bit 1	Tx2_Disable	Read/write bit that allows software disable of transmitters
86 Bit 2	Tx3_Disable	Read/write bit that allows software disable of transmitters
86 Bit 3	Tx4_Disable	Read/write bit that allows software disable of transmitters
Optional Channel Controls and Monitor Masks (Upper Memory, Page 03h)		
241 Bit 4	Rx1_Output_Disable	Rx Output Disable, channel 1 (optional)
241 Bit 5	Rx2_Output_Disable	Rx Output Disable, channel 2 (optional)
241 Bit 6	Rx3_Output_Disable	Rx Output Disable, channel 3 (optional)
241 Bit 7	Rx4_Output_Disable	Rx Output Disable, channel 4 (optional)
Squelch Disable		
240 Bit 0	Tx1_SQ_Disable	Tx Squelch Disable, channel 1 (optional)
240 Bit 1	Tx2_SQ_Disable	Tx Squelch Disable, channel 2 (optional)
240 Bit 2	Tx3_SQ_Disable	Tx Squelch Disable, channel 3 (optional)
240 Bit 3	Tx4_SQ_Disable	Tx Squelch Disable, channel 4 (optional)
240 Bit 4	Rx1_SQ_Disable	Rx Squelch Disable, channel 1 (optional)
240 Bit 5	Rx2_SQ_Disable	Rx Squelch Disable, channel 2 (optional)
240 Bit 6	Rx3_SQ_Disable	Rx Squelch Disable, channel 3 (optional)
240 Bit 7	Rx4_SQ_Disable	Rx Squelch Disable, channel 4 (optional)
Power		
Upper Memory Map Page 00h		
129 bit 7-6	00	Power Class 1 Module (1.5 W max. power consumption)
	01	Power Class 2 Module (2.0 W max. power consumption)
	10	Power Class 3 Module (2.5 W max. power consumption)

	11	Power Class 4 Module (3.5 W max. power consumption)
Power Control: Set PWM (GUI Function)	In the QSFP Host GUI the user have the ability to set the power consumption manually. By setting the PWM value. (Range 0 to 255).	
Rate Select		
By Rate Range		
87 Bit 1,0	Rx1_Rate_Select	Software Rate Select, Rx channel 1 msb , 1 lsb (Optional)
87 Bit 3,2	Rx2_Rate_Select	Software Rate Select, Rx channel 2 msb , 2 lsb (Optional)
87 Bit 5,4	Rx3_Rate_Select	Software Rate Select, Rx channel 3 msb , 3 lsb (Optional)
87 Bit 7,6	Rx4_Rate_Select	Software Rate Select, Rx channel 4 msb , 4 lsb (Optional)
88 Bit 1,0	Tx1_Rate_Select	Software Rate Select, Tx channel 1 msb , 1 lsb (Optional)
88 Bit 3,2	Tx2_Rate_Select	Software Rate Select, Tx channel 2 msb , 2 lsb (Optional)
88 Bit 5,4	Tx3_Rate_Select	Software Rate Select, Tx channel 3 msb , 3 lsb (Optional)
88 Bit 7,6	Tx4_Rate_Select	Software Rate Select, Tx channel 4 msb , 4 lsb (Optional)

xN_Rate_Select msb Value	xN_Rate_Select lsb Value	Description
0	0	Optimized for data rates less than 2.2Gb/s
0	1	Optimized for data rates from 2.2 up to 6.6Gb/s
1	0	Optimized for 6.6 Gb/s data rates and above
1	1	Reserved

The definition for each TX or RX bits combinations is the following: Functionality of xN_Rate_Select with Extended Rate Selection.

When the Rate Select declaration bits (page 00h, byte 221, bits 2 and 3) have the values of 1 and 0 respectively, the Application Select method defined in Page 01h is used.

The host reads the entire application select table on page 01h to determine the capabilities of the transceiver. The host controls each channel separately by writing a Control Mode and Table Select (TS) byte to bytes 89-92 and bytes 94-97. The bits of the Rx_Application Select and the Tx_Application Select registers are defined in the following Table.

7	6	5	4	3	2	1	0
Control Mode		Table Select, TS					

Control Mode defines the application control mode. Table Select selects module behavior from the AST among 63 possibilities (000000 to 111110). Note that (111111) is invalid.

By Application Table		
Data Address	Name of Field	Note and additional description
Control Bytes (Lower Memory Map)		
92 all Bits	Rx1_Application_Select	Software Application Select per SFF-8079, Rx Channel 1 (Optional)
91 all Bits	Rx2_Application_Select	Software Application Select per SFF-8079, Rx Channel 2 (Optional)
90 all Bits	Rx3_Application_Select	Software Application Select per SFF-8079, Rx Channel 3 (Optional)
89 all Bits	Rx4_Application_Select	Software Application Select per SFF-8079, Rx Channel 4 (Optional)
97 all Bits	Tx1_Application_Select	Software Application Select per SFF-8079, Tx Channel 1 (Optional)
96 all Bits	Tx2_Application_Select	Software Application Select per SFF-8079, Tx Channel 2 (Optional)
95 all Bits	Tx3_Application_Select	Software Application Select per SFF-8079, Tx Channel 3 (Optional)
94 all Bits	Tx4_Application_Select	Software Application Select per SFF-8079, Tx Channel 4 (Optional)

6.3.5 Optional Channel Control

Tx Input Equalization, Rx Output Pre-Emphasis and Rx Output Amplitude are optional channel controls.

The table below shows the corresponding MSA memory mapping for the previously explained modules.

Controls Tab		
Optional channel controls(Page 03 Bytes 226-241)		
Data Address	Name of Field	Note and additional description

234 Bit 7-4	Tx1 input equalization control	Read/write bit that allows software disable of transmitters
86 Bit 1	Tx2_Disable	Read/write bit that allows software disable of transmitters
86 Bit 2	Tx3_Disable	Read/write bit that allows software disable of transmitters
86 Bit 3	Tx4_Disable	Read/write bit that allows software disable of transmitters
Optional Channel Controls and Monitor Masks (Upper Memory, Page 03h)		
241 Bit 4	Rx1_Output_Disable	Rx Output Disable, channel 1 (optional)
241 Bit 5	Rx2_Output_Disable	Rx Output Disable, channel 2 (optional)
241 Bit 6	Rx3_Output_Disable	Rx Output Disable, channel 3 (optional)
241 Bit 7	Rx4_Output_Disable	Rx Output Disable, channel 4 (optional)
Squelch Disable		
240 Bit 0	Tx1_SQ_Disable	Tx Squelch Disable, channel 1 (optional)
240 Bit 1	Tx2_SQ_Disable	Tx Squelch Disable, channel 2 (optional)
240 Bit 2	Tx3_SQ_Disable	Tx Squelch Disable, channel 3 (optional)
240 Bit 3	Tx4_SQ_Disable	Tx Squelch Disable, channel 4 (optional)
240 Bit 4	Rx1_SQ_Disable	Rx Squelch Disable, channel 1 (optional)
240 Bit 5	Rx2_SQ_Disable	Rx Squelch Disable, channel 2 (optional)
240 Bit 6	Rx3_SQ_Disable	Rx Squelch Disable, channel 3 (optional)
240 Bit 7	Rx4_SQ_Disable	Rx Squelch Disable, channel 4 (optional)
Power		
Upper Memory Map Page 00h		
129 bit 7-6	00	Power Class 1 Module (1.5 W max. power consumption)
	01	Power Class 2 Module (2.0 W max. power consumption)
	10	Power Class 3 Module (2.5 W max. power consumption)
	11	Power Class 4 Module (3.5 W max. power consumption)
Power Control: Set PWM (GUI Function)	In the QSFP Host GUI the user have the ability to set the power consumption manually. By setting the PWM value. (Range 0 to 255).	
Rate Select		
By Rate Range		

87 Bit 1,0	Rx1_Rate_Select	Software Rate Select, Rx channel 1 msb , 1 lsb (Optional)
87 Bit 3,2	Rx2_Rate_Select	Software Rate Select, Rx channel 2 msb , 2 lsb (Optional)
87 Bit 5,4	Rx3_Rate_Select	Software Rate Select, Rx channel 3 msb , 3 lsb (Optional)
87 Bit 7,6	Rx4_Rate_Select	Software Rate Select, Rx channel 4 msb , 4 lsb (Optional)
88 Bit 1,0	Tx1_Rate_Select	Software Rate Select, Tx channel 1 msb , 1 lsb (Optional)
88 Bit 3,2	Tx2_Rate_Select	Software Rate Select, Tx channel 2 msb , 2 lsb (Optional)
88 Bit 5,4	Tx3_Rate_Select	Software Rate Select, Tx channel 3 msb , 3 lsb (Optional)
88 Bit 7,6	Tx4_Rate_Select	Software Rate Select, Tx channel 4 msb , 4 lsb (Optional)

6.4 Identification

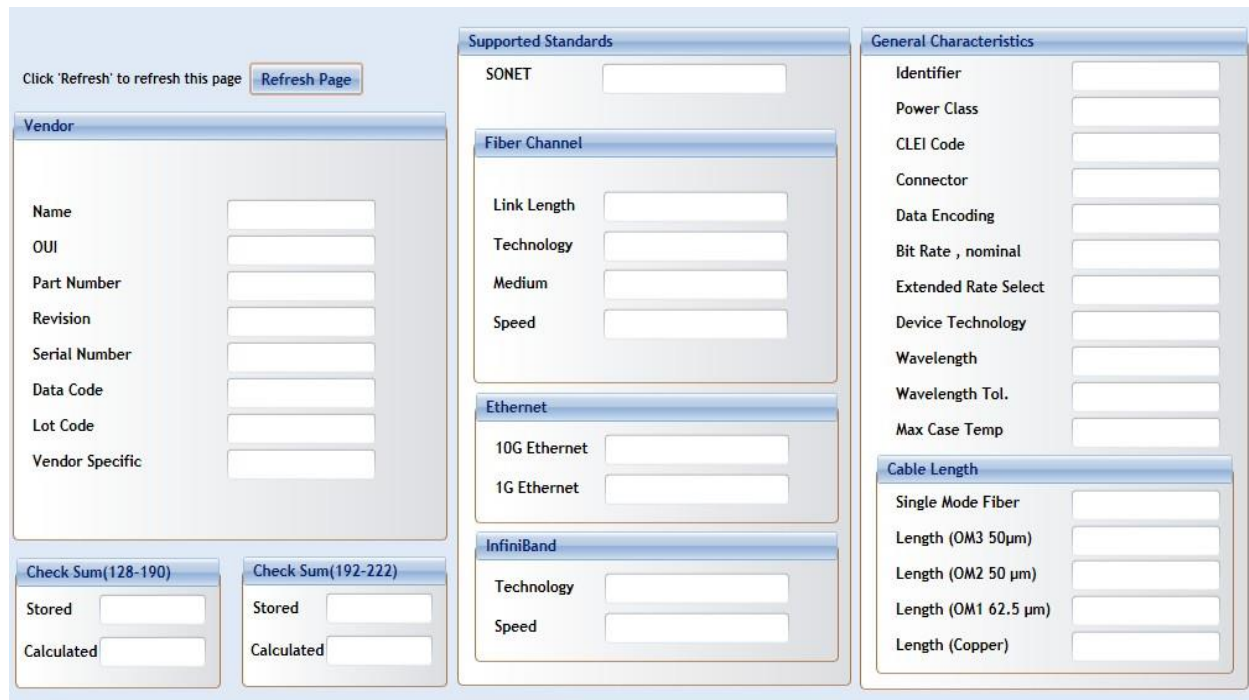


Figure 5: Identification page

The following table shows the corresponding ID registers, along with their names and description.

Identification Tab			
Data Address	Name of Field	Note and additional description	
148-163	Name	Vendor name (MultiLane SAL)	QSFP vendor name (ASCII)

165-167	OUI	Vendor OUI	QSFP vendor IEEE company ID
168-183	Part Number	Vendor part Number: ML4002	Part number provided by QSFP vendor (ASCII)
184-185	Revision	Vendor revision	Revision level for part number provided by vendor (ASCII)
196-211	Serial Number	Vendor Serial number	Serial number provided by vendor (ASCII)
212-219	Data Code	Ordering information part number: ML4002-X-Y	Vendor's manufacturing date code
218-219	Lot Code	ASCII code, vendor specific lot code, may be blank	vendor specific lot code (ASCII)
224-255	Vendor Specific	Firmware revision	Vendor Specific EEPROM
Supported Standards			
132	Sonet	Not Applicable	
133		Not Applicable	
Fiber Channel			
135	Link Length	Not Applicable	
135	Technology	Not Applicable	
136		Not Applicable	
138	Speed	Not Applicable	
Ethernet			
131	10G Ethernet	Bit 4 is "1" then 10GBASE-SR	
134	1G Ethernet	(blank)	
Infiniband			
164	Technology	Not Applicable	
	Speed	Not Applicable	
General Characteristics			

128	Identifier	Identifier Type of serial transceiver		
129 bit 7-6	Power Class	<p>Depending on the Part number choosen.</p> <p>00: Power Class 1 Module (1.5 W max. power consumption)</p> <p>01: Power Class 2 Module (2.0 W max. power consumption)</p> <p>10: Power Class 3 Module (2.5 W max. power consumption)</p> <p>11: Power Class 4 Module (3.5 W max. power consumption)</p>		
129 bit 4	CLEI Code	0: No CLEI code present in Page 02h		
130	Connector	Code for connector type		
		<table border="1"> <thead> <tr> <th>Value</th> <th>Description of Connector</th> </tr> </thead> <tbody> <tr> <td>80-FFh</td> <td>Vendor specific</td> </tr> </tbody> </table>	Value	Description of Connector
Value	Description of Connector			
80-FFh	Vendor specific			
139	Data Encoding	Code for serial encoding algorithm		
		<table border="1"> <thead> <tr> <th>Code</th> <th>Description of encoding mechanism</th> </tr> </thead> <tbody> <tr> <td>03h</td> <td>NRZ</td> </tr> </tbody> </table>	Code	Description of encoding mechanism
Code	Description of encoding mechanism			
03h	NRZ			
140	Bit Rate, nominal	<p>Nominal bit rate (per channel), units of 100 Mbits/s.</p> <ul style="list-style-type: none"> • 103 (decimal) – 10000Mb/s (actual 10312Mb/s), 10GE 		
141	Extended Rate Select Compliance	Not Applicable		
147	Device Tech	Not Applicable		
	Wavelength	Not Applicable		
188-189	Wavelength Tol.	Not Applicable		
190	Max Case Temp	<p>Maximum Case Temperature in Degrees C.</p> <ul style="list-style-type: none"> • 70C (all QSFP+ modules and cables) 		
Cable length				
142	Single Mode Fiber	Not Applicable		
143	Length (OM3 50µm)	Not Applicable		
144	Length (OM2 50 µm)	Not Applicable		
145	Length (OM1 62.5 µm)	Not Applicable		
146	Length (Copper)	Not Applicable		

6.5 Options Available

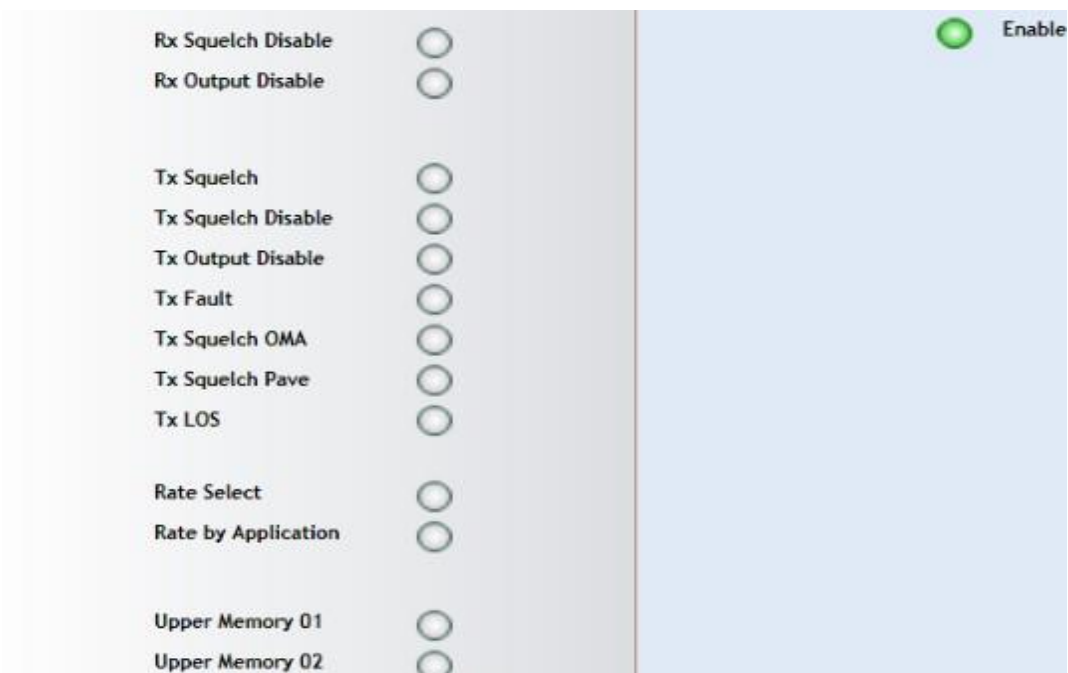


Figure 6 : Options available page

This tab shows which of the above stated options are supported by the module.

6.6 Load/Save

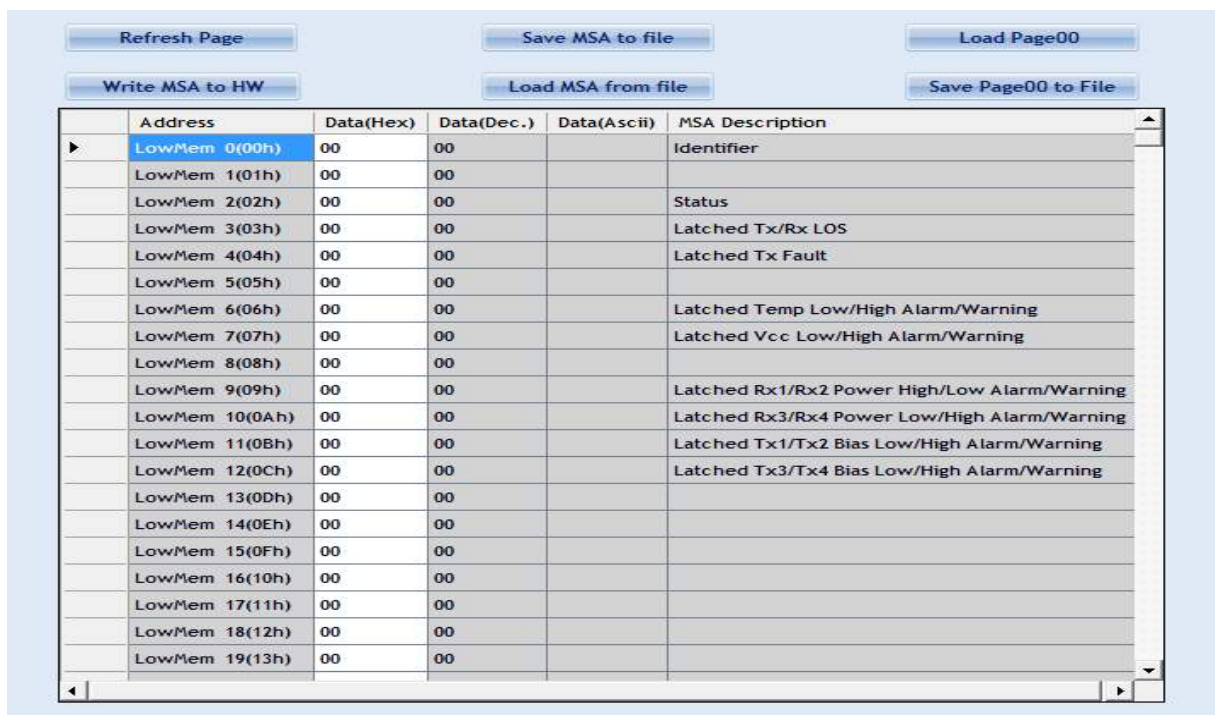


Figure 7: Load/Save page

This screen allows user to Load or Save his custom MSA configuration.

Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value, MSA description.

- **Refresh Page** button: Read MSA Registers, and refresh values.
- **Write MSA to HW** button: Write the current MSA configuration to QSFP module.
- **Save MSA to file** button: saves the current MSA memory to a file using Comma separated values (CSV) format.
- **Load MSA from file** button: Loads MSA values from file and map it to MSA memory.
- **Load Page00** button: same as Load MSA from file, but loads only page 0 data.
- **Save Page00 to file** button: same as Save MSA to file, but saves only page0 data.

6.7 AOC

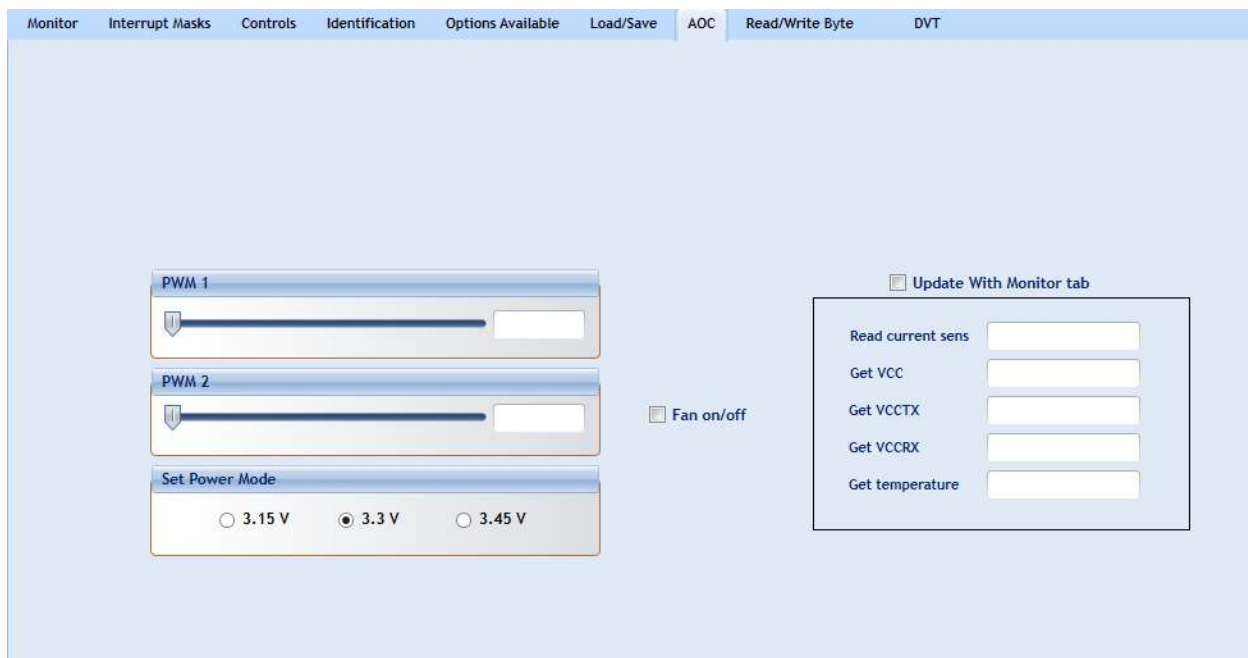


Figure 8: GUI_ AOC mode

All these measurements are available in Active Optical Cable (AOC) mode, while only the current sense and the temperature are available in normal Mode.

Set Power Mode group box is used to change VCC level supplied to the QSFP module; this is only available in AOC Mode.

6.8 DVT

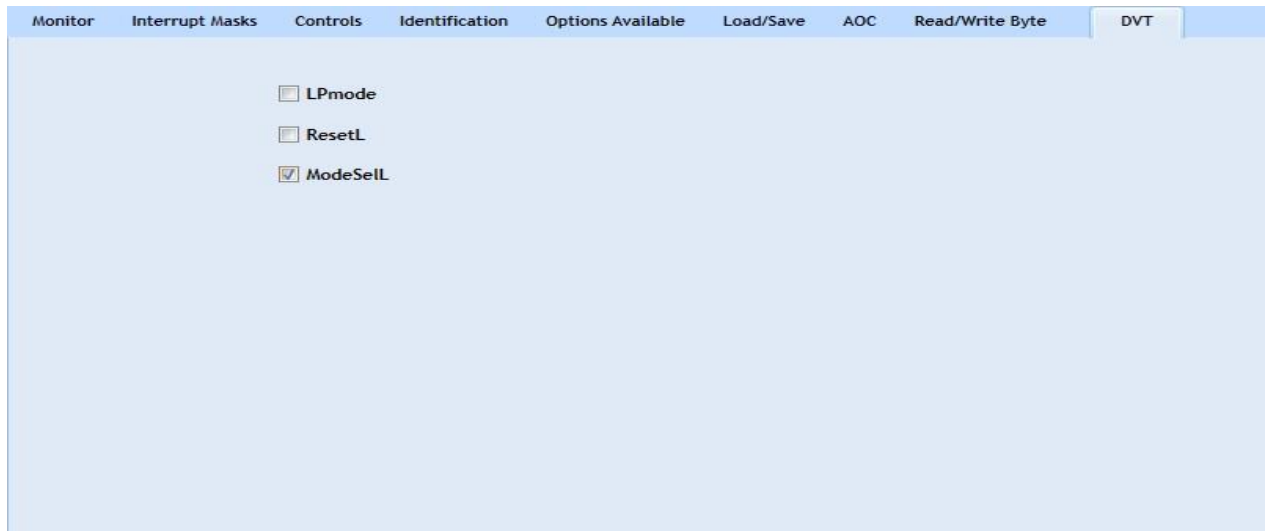


Figure 9-DVT Tab

7. AOC VS normal mode

This guide describes the difference between operation in normal mode and AOC mode for the ML4021 (QSFP+ Host).

7.1 Operation in normal mode

Host boards assembled to work in normal mode will have resistor **R61** (0 ohm) populated on the board, and **R60** (0 ohm) DNP.

For Power up, turn on the power supply voltage (**3.3V**), and connect it to the banana plugs (**U5 and U6**) as shown below.

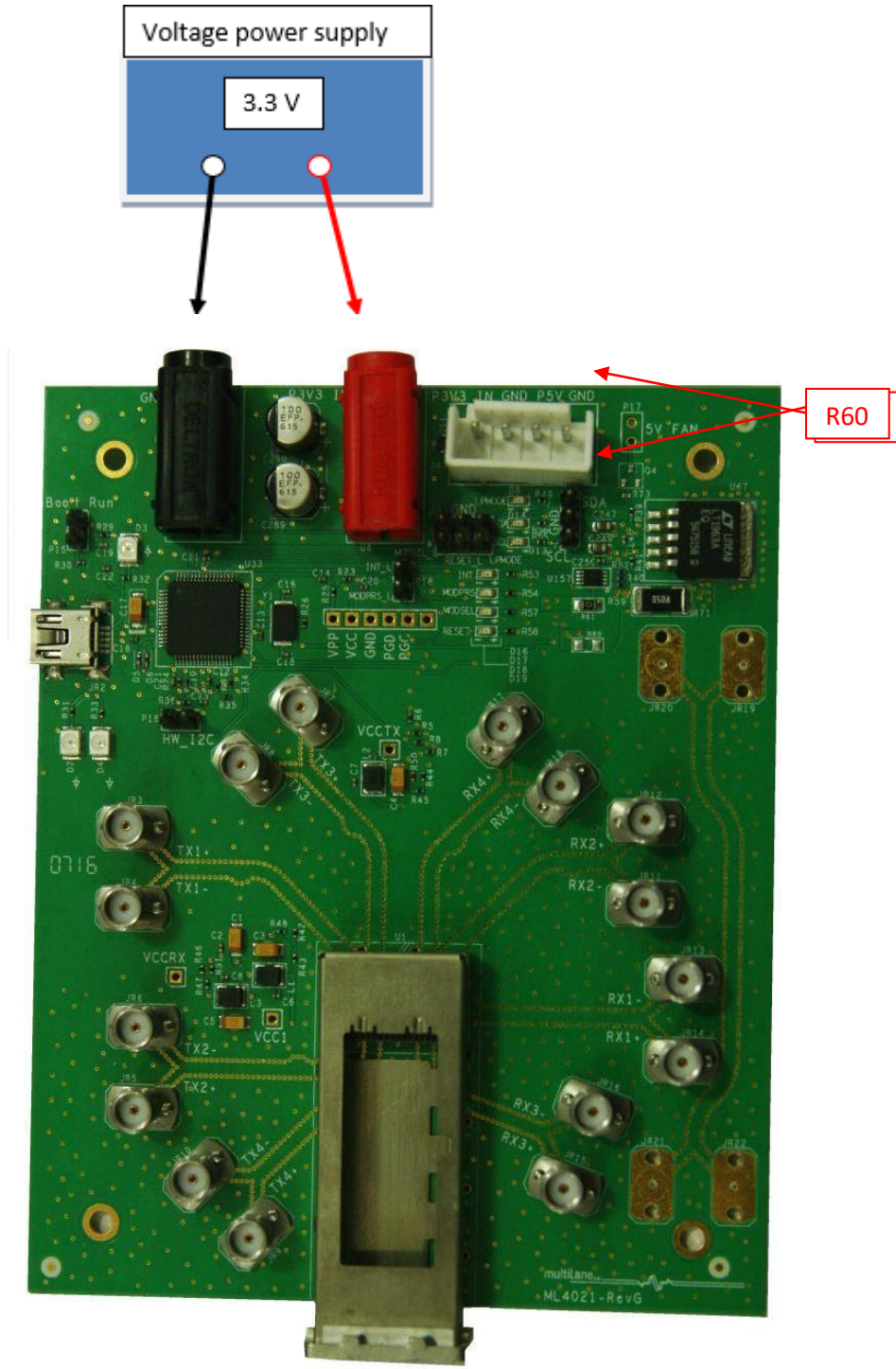


Figure 10: Normal Mode

7.2 Operation in AOC mode

Host boards assembled to work in AOC mode will have resistor **R60** (0 ohm) populated on the board, and **R61** (0 ohm) DNP.

For Power up, turn on the power supply voltages (**5 V and 3.3V**), and connect them to **J43** connector as shown below.

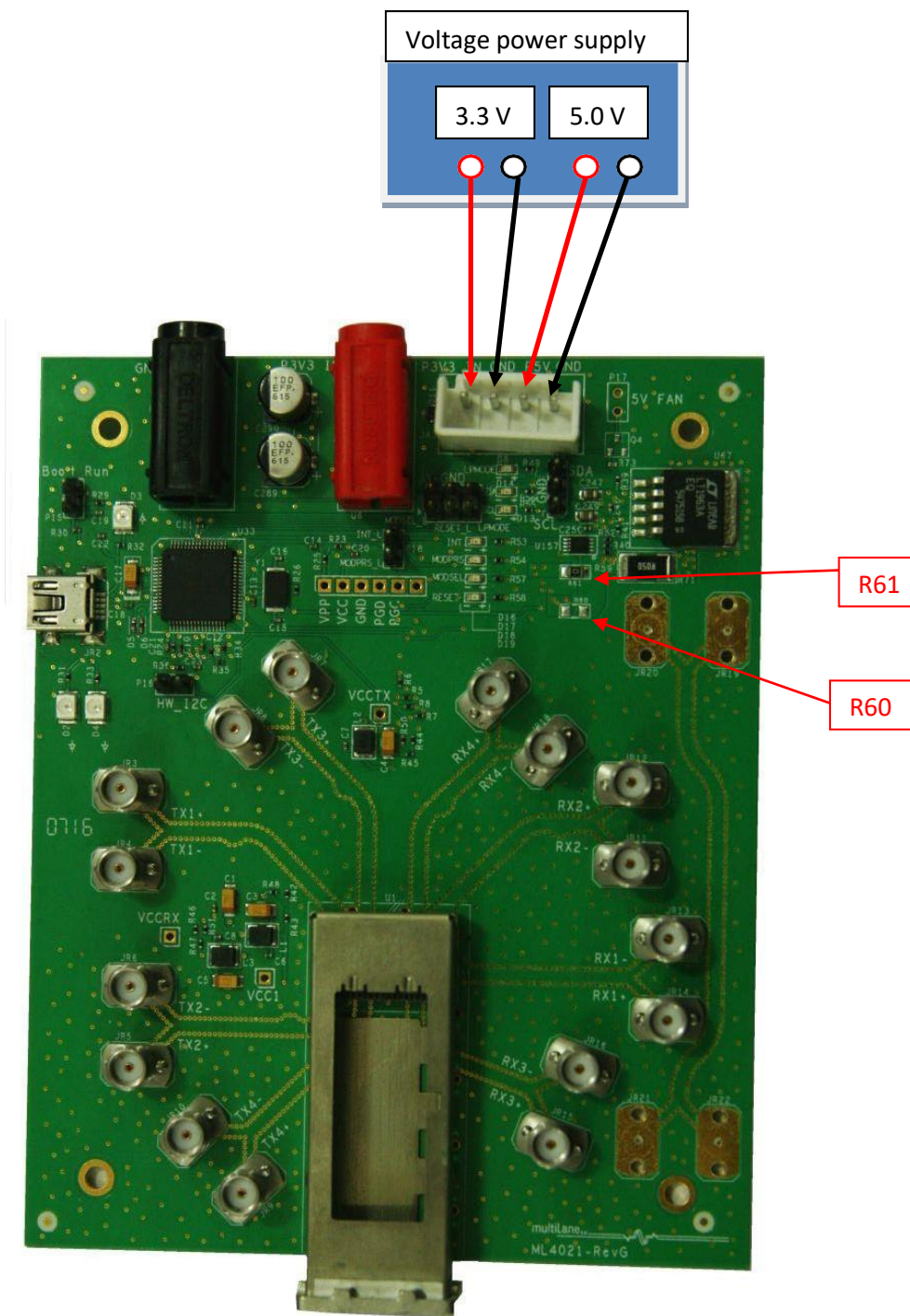


Figure 11: AOC mode

Revision Information

Revision number	Description	Date
1.0	<ul style="list-style-type: none"> ▪ Preliminary revision 	2015/06/19
2.0	<ul style="list-style-type: none"> ▪ Added TX_Power monitoring (SFF8636) 	
2.1	<ul style="list-style-type: none"> ▪ Fixed the ML4020 typo ▪ Updated the pictures of the boards ▪ Some paragraphs are omitted ▪ LED indications 	2016/04/15
2.2	<ul style="list-style-type: none"> ▪ Added USB instance 	2016/08/22
2.3	<ul style="list-style-type: none"> ▪ Added HW signaling pins 	2016/09/01
2.4	<ul style="list-style-type: none"> ▪ Monitor tab - power display 	2017/03/28
2.5	<ul style="list-style-type: none"> ▪ Update Control Tab and add DVT 	2018/02/23

North America

48521 Warm Springs Blvd. Suite 310
 Fremont, CA 94539
 USA
 +1 510 573 6388

Worldwide

Houmal Technology Park
 Askarieh Main Road
 Houmal, Lebanon
 +961 5 941 668

Asia

14F-5/ Rm.5, 14F., No 295
 Sec.2, Guangfu Rd. East Dist.,
 Hsinchu City 300, Taiwan (R.O.C)
 +886 3 5744 591