SLASER3A – JULY 2018 – REVISED NOVEMBER 2018

DACx1408 8-Channel, 16-,14-,12-Bit, High-Voltage Output DACs with Internal Reference

1 Features

- Performance
  - Specified Monotonic at 16-Bit Resolution
  - INL: ±1 LSB Maximum at 16-Bit Resolution
  - TUE: ±0.1% of FSR Maximum
- Integrated 2.5-V Precision Internal Reference
  - Initial Accuracy: ±2.5 mV Maximum
  - Low Drift: 5 ppm/°C Typical
- Flexible Output Configuration
  - Output Range: ±2.5 V, ±5 V, ±10 V, ±20 V 0 to 5 V, 0 to 10 V, 0 to 20 V, 0 to 40 V
  - Differential Output Mode
- High Drive Capability: ±25 mA with 1.5 V from Supply Rails
- Three Dedicated A-B Toggle Pins for Dither Signal Generation
- Analog Temperature Output
  - Sensor Gain of –4 mV/°C
- 50-MHz SPI Compatible Serial Interface
  - 4-Wire Mode, 1.7-V to 5.5-V Operation
  - Daisy Chain Operation
  - CRC Error Check
- Temperature Range: –40°C to +125°C
- Small Package
  - 6 mm × 6 mm, 40-Pin VQFN

2 Applications

- Optical Networking: Mach-Zehnder Modulator Bias Control
- Industrial Automation
- Test and Measurement

3 Description

The DAC81408, DAC71408, and DAC61408 (DACx1408) are a pin-compatible family of 8-channel, buffered, high-voltage output digital-to-analog converters (DACs) with 16-, 14- and 12-bit resolution. The DACx1408 includes a low drift, 2.5-V internal reference, eliminating the need for an external precision reference in most applications. These devices are specified monotonic and provide high linearity of ±1 LSB INL.

A user selectable output configuration enables full-scale bipolar output voltages: ±20 V, ±10 V, ±5 V or ±2.5 V and full-scale unipolar output voltages: 40 V, 20 V, 10 V or 5 V. The full-scale output range for each DAC channel is independently programmable. The integrated DAC output buffers can sink or source up to 25 mA thus limiting the need of additional operational amplifiers. Each pair of channels can be configured to provide a differential output with offset calibration. The three dedicated A-B toggle pins enable dither signal generation with up to three possible frequencies.

The DACx1408 incorporates a power-on-reset circuit that connects the DAC outputs to ground at power-up. The outputs remain at this state until the device registers are properly configured for operation.

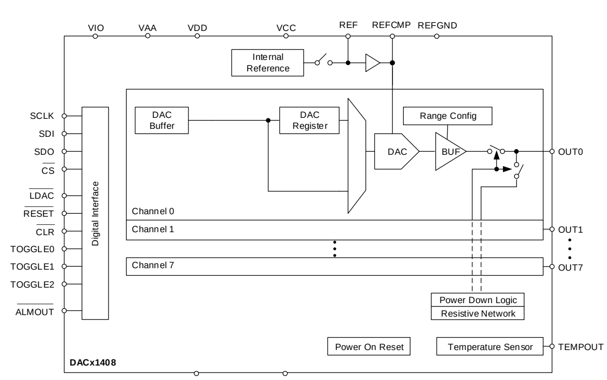
Communication to the DACx1408 is performed through a 4-wire serial interface that supports operation from 1.7 V to 5.5 V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC81408 DAC71408 DAC61408	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

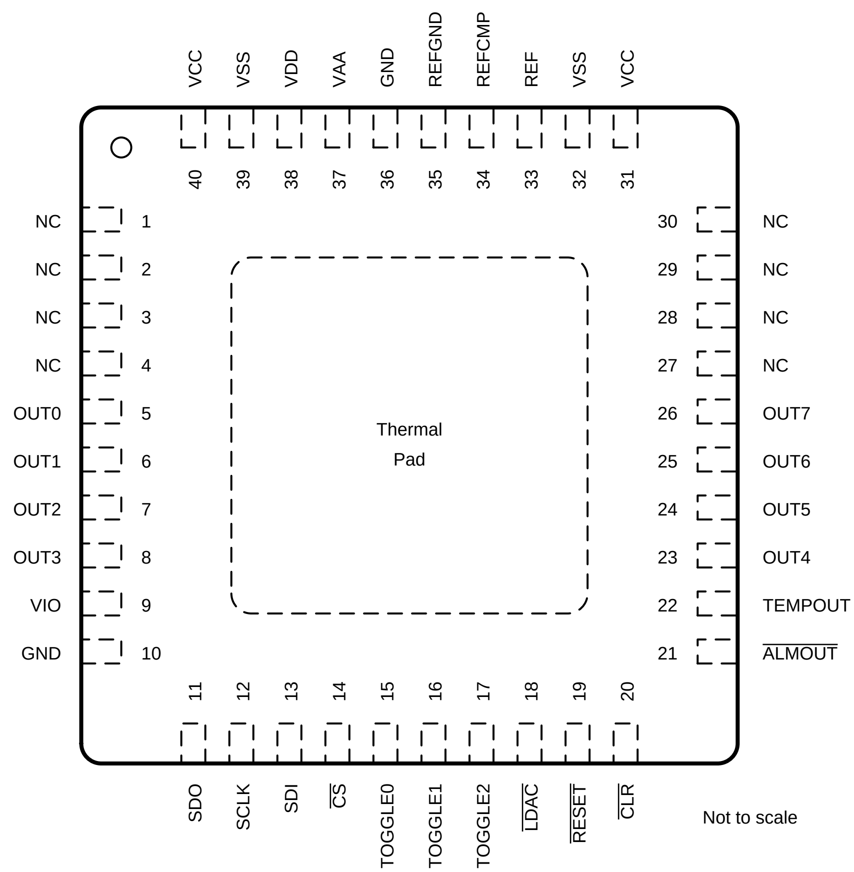
Changes from Original (July 2018) to Revision A	Page
• Changed DAC81408 from Advance Information to Production Data	1
• Changed DAC71408 and DAC61408 from Product Preview to Production Data	1

5 Device Comparison Table

DEVICE	RESOLUTION
DAC81408	16-Bit
DAC71408	14-Bit
DAC61408	12-Bit

6 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT[0:7]	5 - 8, 23 - 26	O	Analog DAC output voltages.
NC	1, 2, 3, 4, 27, 28, 29, 30	O	No connection.
VIO	9	PWR	IO supply voltage. (1.7 V to 5.5 V). This pin sets the I/O operating voltage for the device.
GND	10, 36	GND	Ground reference point for all circuitry on the device.
SDO	11	O	Serial interface data output. The SDO pin must be enabled before operation by setting the SDO-EN bit. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit (rising edge by default).
SCLK	12	I	Serial interface clock.
SDI	13	I	Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
$\overline{CS}$	14	I	Active low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, it enables the serial interface input shift register.
TOGGLE0	15	I	Toggle pins. Control signals for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE pins to ground if not using the toggle operation.
TOGGLE1	16	I	
TOGGLE2	17	I	
$\overline{LDAC}$	18	I	Active low synchronization signal. When the $\overline{LDAC}$ pin is low, the DAC outputs of those channels configured in synchronous mode are updated simultaneously. Connect to VIO if unused.
$\overline{RESET}$	19	I	Active low reset input. Logic low on this pin causes the device to issue a power-on-reset event.
$\overline{CLR}$	20	I	Active low clear input. Logic low on this pin clears all DAC outputs to their clear code. Connect to VIO if unused.
$\overline{ALMOUT}$	21	O	$\overline{ALMOUT}$ is an open drain alarm output. An external 10-kΩ pull-up resistor to a voltage no higher than V_{IO} is required.
TEMPOUT	22	O	Analog temperature monitor output.
VCC	31, 40	PWR	Output positive analog power supply (9 V to 41.5 V).
VSS	32, 39	PWR	Output negative analog power supply (-21.5 V to 0 V).
REF	33	I/O	Reference input to the device when operating with external reference. When using internal reference, this is the reference output voltage pin. Connect a 150-nF capacitor to ground.
REFCMP	34	I/O	Reference compensation capacitor connection. Connect a 330-pF capacitor between REFCMP and REFGND.
REFGND	35	GND	Ground reference point for the internal reference.
VAA	37	PWR	Analog supply voltage (4.5 V to 5.5 V). This pin must be at the same potential as the VDD pin.
VDD	38	PWR	Digital supply voltage (4.5 V to 5.5 V). This pin must be at the same potential as the VAA pin.
THERMAL PAD	–	–	The thermal pad is located on the package underside. The thermal pad should be connected to any internal PCB ground plane through multiple vias for good thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD} to GND	-0.3	6	V
	V_{IO} to GND	-0.3	6	V
	V_{CC} to GND	-0.3	44	V
	V_{SS} to GND	-22	0.3	V
	REFGND to GND	-0.3	0.9	V
	V_{DD} to V_{AA}	-0.3	0.3	V
	V_{CC} to V_{SS}	-0.3	44	V
Pin voltage	DAC outputs to GND	V_{SS} - 0.3	V_{CC} + 0.3	V
	TEMPOUT to GND	-0.3	V_{DD} + 0.3	V
	REF and REFCMP to GND	-0.3	V_{DD} + 0.3	V
	Digital inputs to GND	-0.3	V_{IO} + 0.3	V
	SDO to GND	-0.3	V_{IO} + 0.3	V
	$\overline{\text{ALARMOUT}}$ to GND	-0.3	6	V
Operating junction temperature, T_J		-40	150	°C
Storage temperature, T_{stg}		-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{AA} (1)		4.5		5.5	V
V_{DD} (1)		4.5		5.5	V
V_{IO}		1.7		5.5	V
V_{CC}		9		41.5	V
V_{SS} (2)		-21.5		0	V
$V_{CC} – V_{SS}$		9		43	V
Digital input voltage		0		V_{IO}	V
V_{REFIN}	Reference input voltage to V_{REFGND}	2.49	2.5	2.51	V
V_{REFGND} (3)	REFGND pin voltage	0	0	0.6	V
T_A	Operating ambient temperature	-40		125	°C

(1) V_{AA} and V_{DD} must be at the same potential.
(2) V_{SS} is only connected to GND when all DAC outputs are unipolar.
(3) If V_{REFGND} is not connected to GND, a buffered source must be used to drive it.

7.4 Thermal Information

THERMAL METRIC(1)		DACx1408 RHA (VQFN) 40 PINS
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	26.8
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1
$R_{\Theta JB}$	Junction-to-board thermal resistance	3.4
Ψ_{JT}	Junction-to-top characterization parameter	0.2
Ψ_{JB}	Junction-to-board characterization parameter	3.4
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

all minimum/maximum specifications at T_A = -40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = -21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC81408	Resolution		16			Bits
	Integral nonlinearity (INL)	All ranges, except 0 to 40 V and ±2.5 V	-1	±0.5	1	LSB
		0 to 40 V and ±2.5 V range	-2	±1	2	LSB
	Differential nonlinearity (DNL)	Specified 16-bit monotonic	-1	±0.5	1	LSB
DAC71408	Resolution		14			Bits
	Integral nonlinearity (INL)	All ranges	-1	±0.5	1	LSB
	Differential nonlinearity (DNL)	Specified 14-bit monotonic	-1	±0.5	1	LSB
DAC61408	Resolution		12			Bits
	Integral nonlinearity (INL)	All ranges	-1	±0.5	1	LSB
	Differential nonlinearity (DNL)	Specified 12-bit monotonic	-1	±0.5	1	LSB
TUE	Total unadjusted error	All ranges, except ±2.5 V	-0.1	±0.01	0.1	%FSR
		±2.5 V range	-0.2	±0.02	0.2	
	Unipolar offset error	All unipolar ranges	-0.03	±0.015	0.03	%FSR
	Unipolar zero-code error	All unipolar ranges	0	0.04	0.1	%FSR
	Bipolar zero error	All bipolar ranges	-0.2	±0.02	0.2	%FSR
	Full-scale error	All ranges	-0.2	±0.075	0.2	%FSR
	Gain error	All ranges, except ±2.5 V	-0.1	±0.02	0.1	%FSR
		±2.5 V range	-0.2	±0.02	0.2	
	Unipolar offset error drift	All unipolar ranges		±2		ppm of FSR/°C
	Bipolar zero error drift	All bipolar ranges		±2		ppm of FSR/°C
	Gain error drift	All ranges		±2		ppm of FSR/°C
	Output voltage drift over time	T_A = 40°C, Full-scale code, 1900 hours		5		ppm of FSR
DIFFERENTIAL MODE PERFORMANCE(1)						
TUE	Total unadjusted error	All ranges	-0.1	±0.01	0.1	%FSR
		±2.5 V range	-0.2	±0.02	0.2	
	Common mode error	All bipolar ranges. Midscale code	-0.1	±0.01	0.1	%FSR
OUTPUT CHARACTERISTICS						
	Output voltage headroom	to V_{SS} and V_{CC} (-10 mA ≤ I_{OUT} ≤ 10 mA)	1			V
		to V_{SS} and V_{CC} (-15 mA ≤ I_{OUT} ≤ 15 mA)	1.5			
	Short circuit current(2)	Full-scale output shorted to V_{SS}		40		mA
		Zero-scale output shorted to V_{CC}		40		
	Load regulation	Midscale code, -15 mA ≤ I_{OUT} ≤ 15 mA		70		µV/mA
	Maximum capacitive load(3)	R_{LOAD} = open	0		1	nF
	DC output impedance	Midscale code		0.05		Ω
		Full-scale code		40		

(1) End point fit between codes. 16-bit: Code 256 to 65280, 14-bit: Code 128 to 16256, 12-bit: Code 32 to 4064.
(2) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
(3) Specified by design and characterization, not production tested.

Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = -40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = -21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling time to ±1 LSB, ±10 V range, R_L = 5 kΩ, C_L = 200 pF		12		µs
	Slew rate	0 to 5 V range		1		V/µs
		All other output ranges		4		
	Power-on glitch magnitude	Power-down to active DAC output. ±20 V range, midscale code, R_L = 5 kΩ, C_L = 200 pF		0.3		V
	Output noise	0.1 Hz to 10 Hz, midscale code, 0 to 5 V range		15		µVpp
	Output noise density	1 kHz, midscale code, 0 to 5 V range		78		nV/Hz
	AC PSRR	Midscale code, frequency = 60 Hz, amplitude 200 mVpp superimposed on V_{DD}, V_{CC} or V_{SS}		1		LSB/V
	DC PSRR	Midscale code, V_{DD} = 5 V ± 5%, V_{CC} = 20 V, V_{SS} = -20 V		1		LSB/V
		Midscale code, V_{DD} = 5 V, V_{CC} = 20 V ± 5%, V_{SS} = -20 V		1		
		Midscale code, V_{DD} = 5 V, V_{CC} = 20 V, V_{SS} = -20 V ± 5%		1		
	Code change glitch impulse	1 LSB change around major carrier, 0 to 5 V range		4		nV-s
	Channel to Channel AC crosstalk	0 to 5 V range. Measured channel at midscale. Full-scale swing on all other channels		4		nV-s
	Channel to Channel DC crosstalk	0 to 5 V range. Measured channel at midscale. All other channels at full-scale		0.25		LSB
	Digital feedthrough	0 to 5 V range. Midscale code, f_{SCLK} = 1 MHz		1		nV-s

Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = -40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = -21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL REFERENCE INPUT						
V_{REFIN}	Reference input voltage range	to V_{REFGND}	2.49	2.5	2.51	V
	Reference input current			50		µA
	Reference input impedance			50		kΩ
	Reference input capacitance			20		pF
INTERNAL REFERENCE						
V_{REFOUT}	Reference output voltage range	T_A = 25°C	2.4975		2.5025	V
	Reference output drift			5	15	ppm/°C
	Reference output impedance			0.1		Ω
	Reference output noise	0.1 Hz to 10 Hz		12		µVpp
	Reference output noise density	10 kHz, REF_{LOAD} = 10 nF		150		nV/Hz
	Reference load current			5		mA
	Reference load regulation	Source		80		µV/mA
	Reference line regulation			20		µV/V
	Reference output drift over time	T_A = 25°C, 1900 hours		250		µV
	Reference thermal hysteresis	First cycle		±700		µV
		Additional cycle		±50		
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage				0.3 × V_{IO}	V
	Input current			±2		µA
	Input pin capacitance			2		pF
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA	V_{IO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 0.2 mA			0.4	V
	Output pin capacitance			5		pF
ALARM OUTPUT						
	Output pin capacitance			5		pF
V_{OL}	Low-level output voltage	I_{LOAD} = -0.2 mA			0.4	V
TEMPERATURE OUTPUT						
$V_{TEMPOUT,0C}$	Output voltage offset at 0°C			1.34		V
	Sensor gain			-4		mV/°C

Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = -40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = -21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS						
I_{DD}	V_{DD} supply current	Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static.		0.05	0.5	mA
		Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static.		0.05	0.5	mA
		Power-down mode		0.05	0.5	mA
I_{AA}	V_{AA} supply current	Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static.		20	30	mA
		Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static.		18	28	mA
		Power-down mode		2	85	µA
I_{CC}	V_{CC} supply current	Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static.		5	10	mA
		Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static.		5	10	mA
		Power-down mode		10	30	µA
I_{SS}	V_{SS} supply current	Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static.	-10	-5		mA
		Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static.	-10	-5		mA
		Power-down mode	-30	-10		µA
I_{IO}	V_{IO} supply current	SCLK and SDI toggling at 50 MHz		350	500	µA

7.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE - WRITE OPERATION						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			25	MHz
		V_{IO} = 2.7 V to 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	15			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ hight time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
$t_{DACWAIT}$	Sequential DAC update wait time	V_{IO} = 1.7 V to 2.7 V	2.4			µs
		V_{IO} = 2.7 V to 5.5 V	2.4			
$t_{BCASTWAIT}$	Broadcast DAC update wait time	V_{IO} = 1.7 V to 2.7 V	4			µs
		V_{IO} = 2.7 V to 5.5 V	4			
SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 0						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			15	MHz
		V_{IO} = 2.7 V to 5.5 V			20	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	33			ns
		V_{IO} = 2.7 V to 5.5 V	25			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	33			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	20			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	8			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDOZD}	SDO tri-state to driven	V_{IO} = 1.7 V to 2.7 V	0		20	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
t_{SDODLY}	SDO output delay	V_{IO} = 1.7 V to 2.7 V	0		35	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	

Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 1						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			25	MHz
		V_{IO} = 2.7 V to 5.5 V			35	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	14			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	14			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	20			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	8			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDOZD}	SDO tri-state to driven	V_{IO} = 1.7 V to 2.7 V	0		20	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
t_{SDODLY}	SDO output delay	V_{IO} = 1.7 V to 2.7 V	0		35	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
DIGITAL LOGIC						
t_{LOGDLY}	$\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time	V_{IO} = 1.7 V to 2.7 V	40			ns
t_{LOGDLY}	$\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time	V_{IO} = 2.7 V to 5.5 V	20			
t_{LDAC}	$\overline{LDAC}$ low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
t_{CLR}	$\overline{CLR}$ low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
t_{RESET}	POR reset delay	V_{IO} = 1.7 V to 2.7 V			1	ms
		V_{IO} = 2.7 V to 5.5 V			1	
f_{TOGGLE}	TOGGLE frequency	V_{IO} = 1.7 V to 2.7 V			100	kHz
		V_{IO} = 2.7 V to 5.5 V			100	

7.7 Typical Characteristics

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. Bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

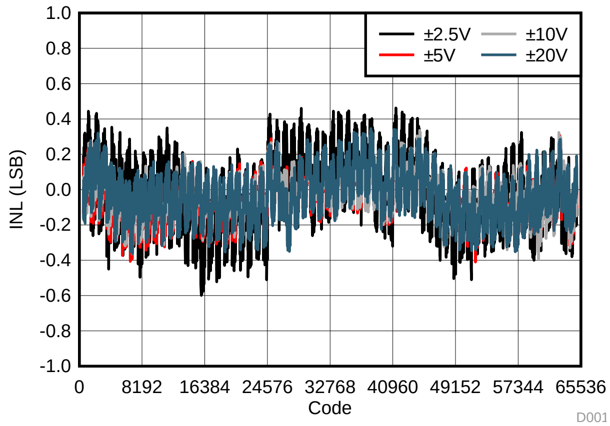


Figure 1. Integral Linearity Error vs Digital Input Code (Bipolar Outputs)

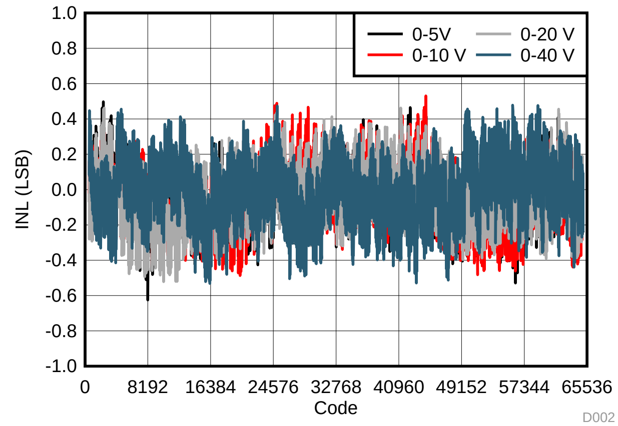


Figure 2. Integral Linearity Error vs Digital Input Code (Unipolar Outputs)

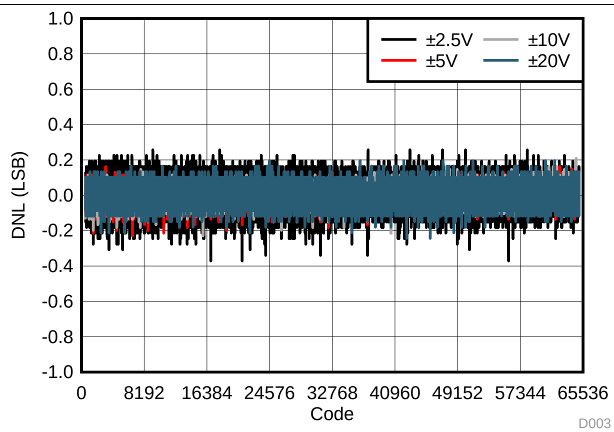


Figure 3. Differential Linearity Error vs Digital Input Code (Bipolar Outputs)

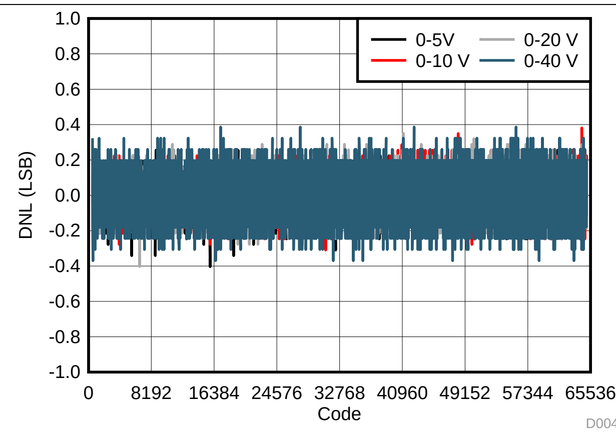


Figure 4. Differential Linearity Error vs Digital Input Code (Unipolar Outputs)

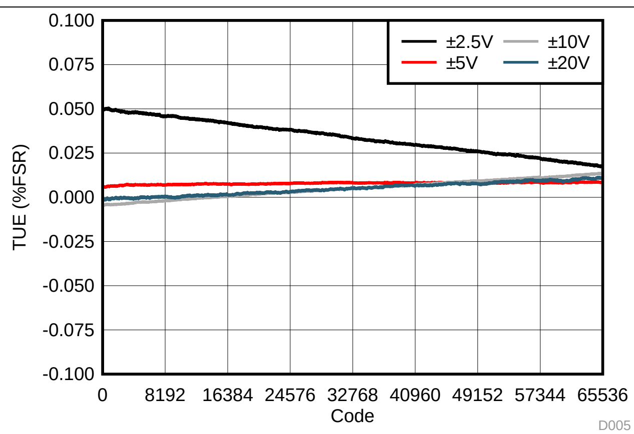


Figure 5. Total Unadjusted Error vs Digital Input Code (Bipolar Outputs)

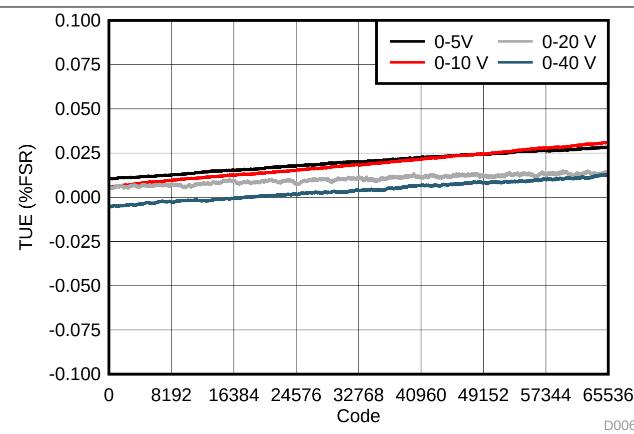


Figure 6. Total Unadjusted Error vs Digital Input Code (Unipolar Outputs)

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

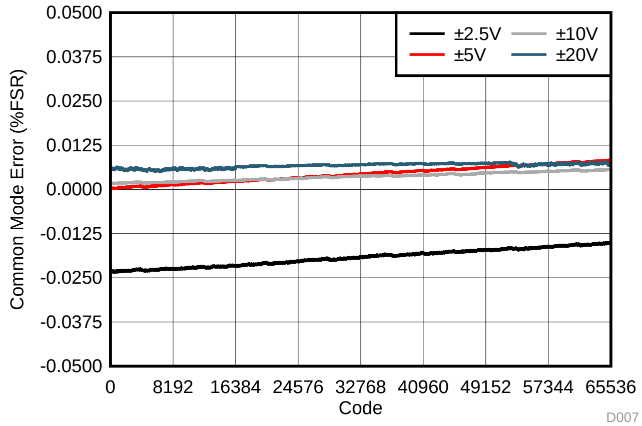


Figure 7. Common Mode Error vs Digital Input Code (Differential Bipolar Outputs)

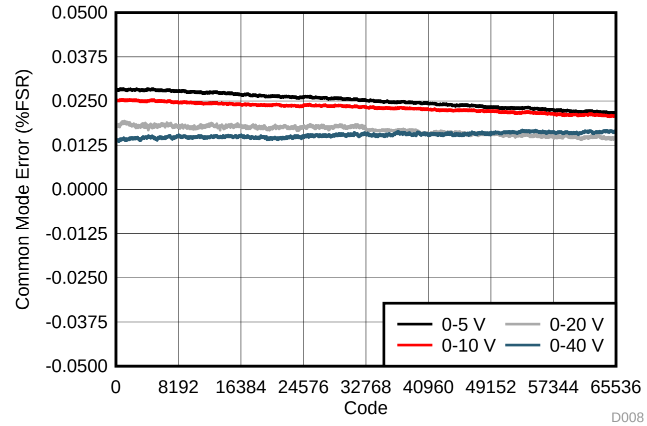
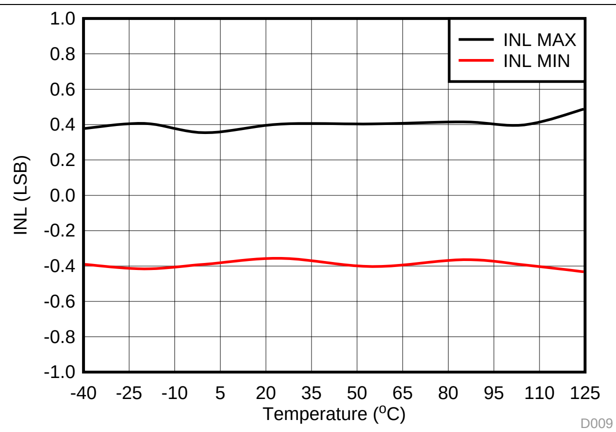
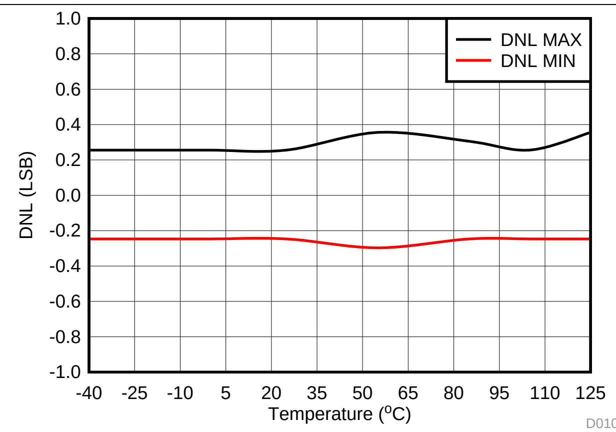


Figure 8. Common Mode Error vs Digital Input Code (Differential Unipolar Outputs)



±20-V Output Range

Figure 9. Integral Linearity Error vs Temperature



±20-V Output Range

Figure 10. Differential Linearity Error vs Temperature

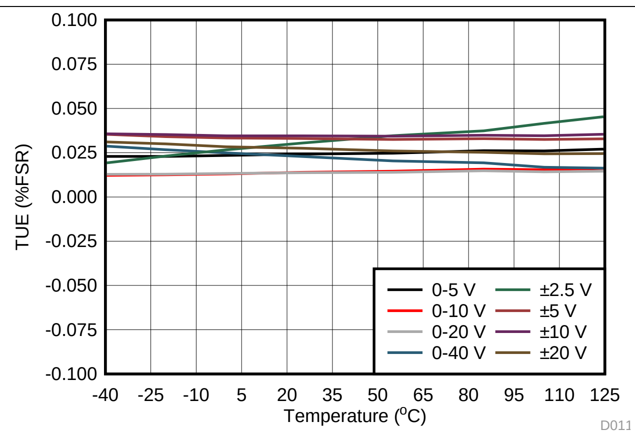


Figure 11. Total Unadjusted Error vs Temperature

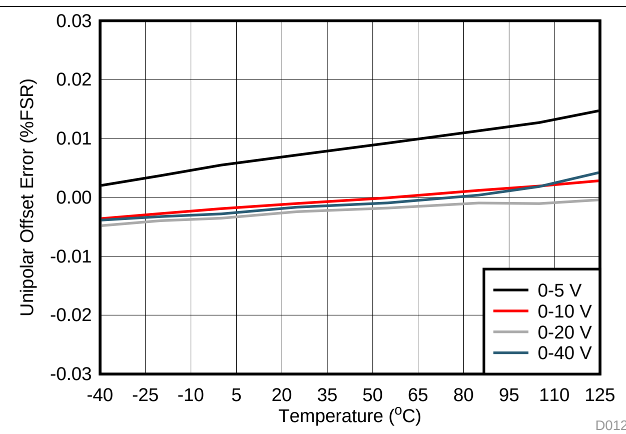


Figure 12. Unipolar Offset Error vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. Bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

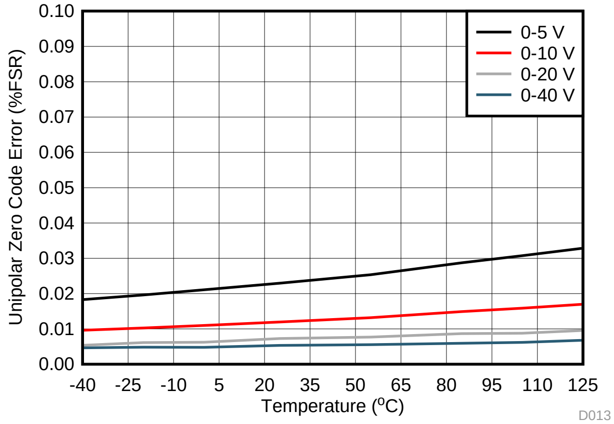


Figure 13. Unipolar Zero Code Error vs Temperature

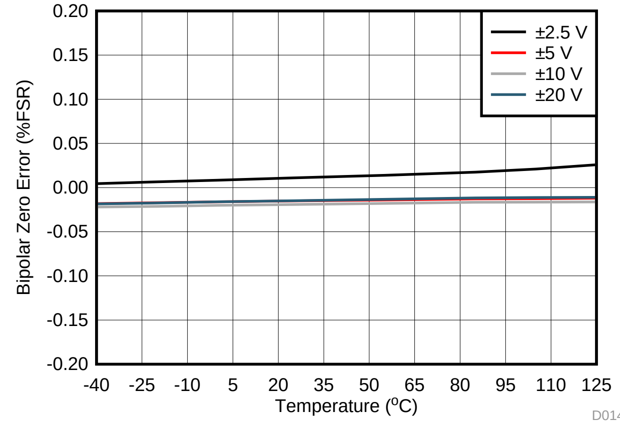


Figure 14. Bipolar Zero Error vs Temperature

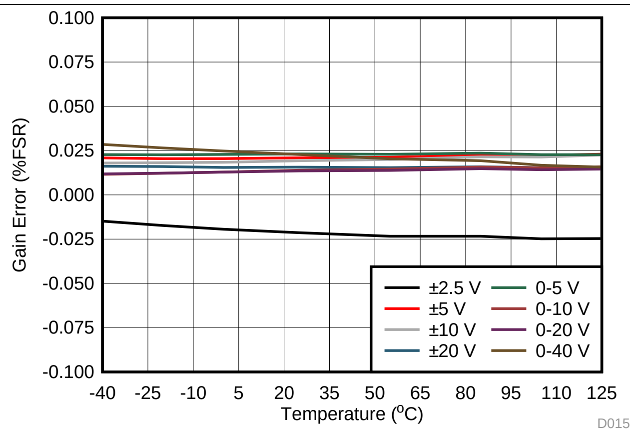


Figure 15. Gain Error vs Temperature

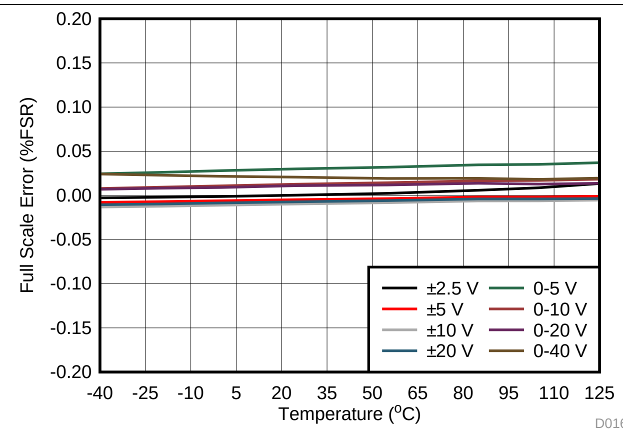


Figure 16. Full-Scale Error vs Temperature

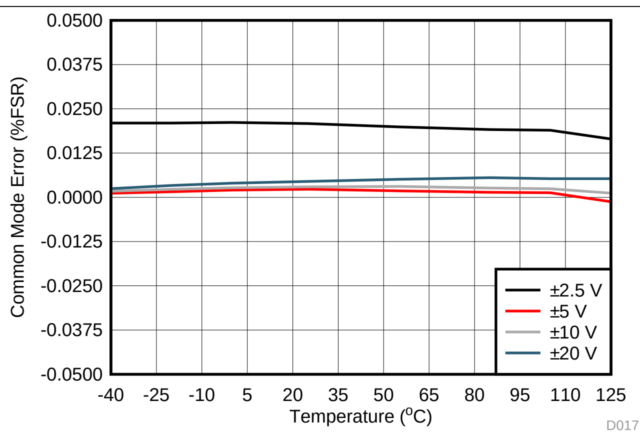


Figure 17. Common Mode Error vs Temperature (Differential Bipolar Outputs)

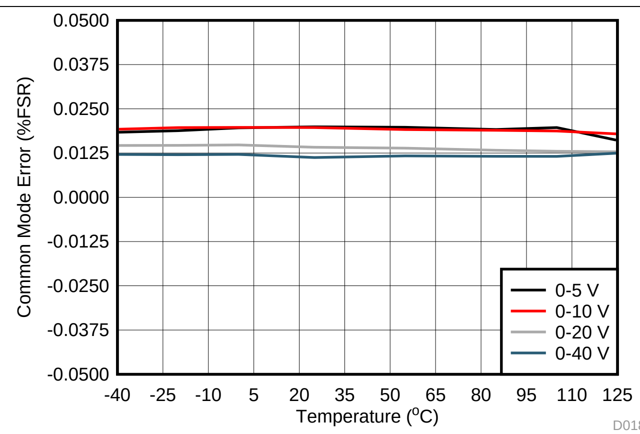
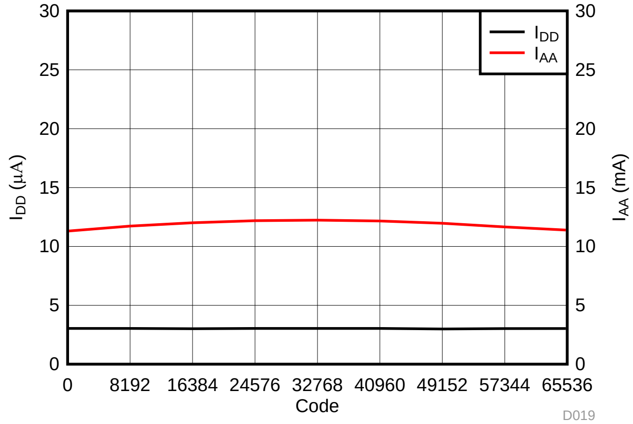


Figure 18. Common Mode Error vs Temperature (Differential Unipolar Outputs)

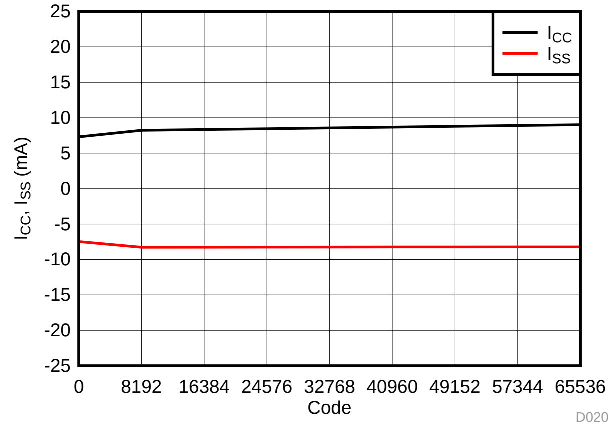
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.



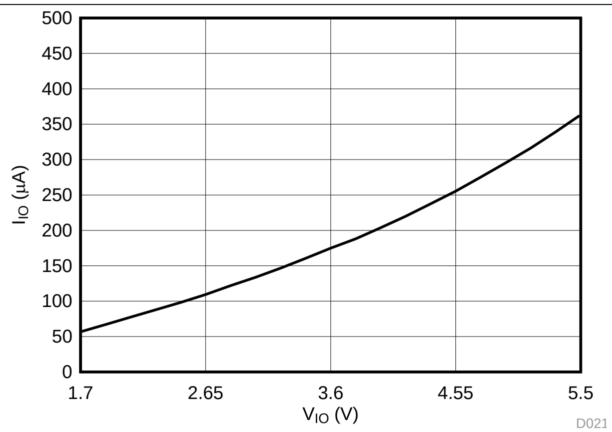
±20-V Output Range

Figure 19. Supply Current (I_{DD}, I_{AA}) vs Digital Input Code



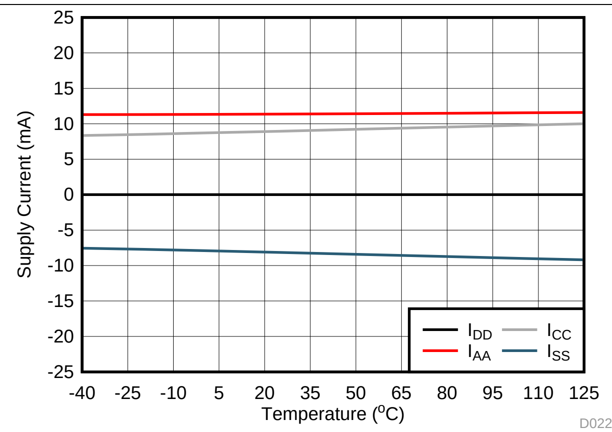
±20-V Output Range

Figure 20. Supply Current (I_{CC}, I_{SS}) vs Digital Input Code



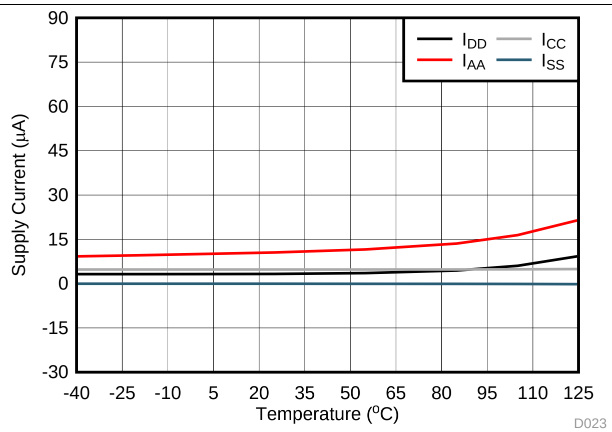
±20-V Output Range

Figure 21. Supply Current (I_{IO}) vs Supply Voltage



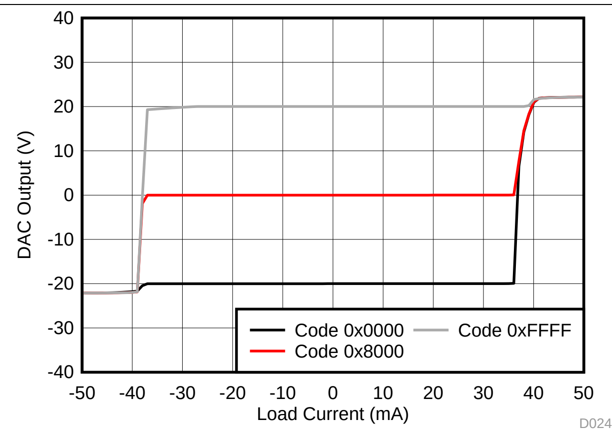
±20-V Output Range

Figure 22. Supply Current vs Temperature



±20-V Output Range

Figure 23. Power-Down Current vs Temperature

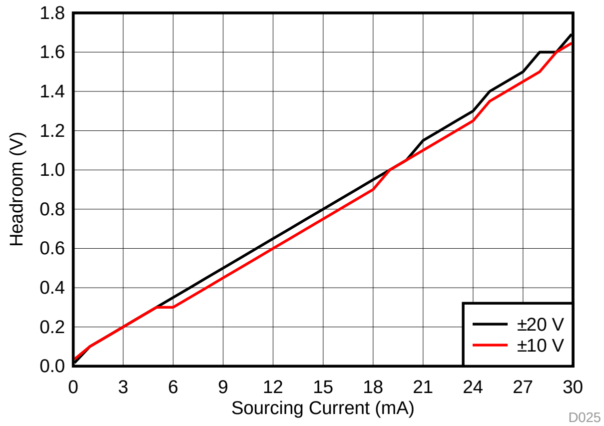


±20-V Output Range

Figure 24. Source and Sink Capability

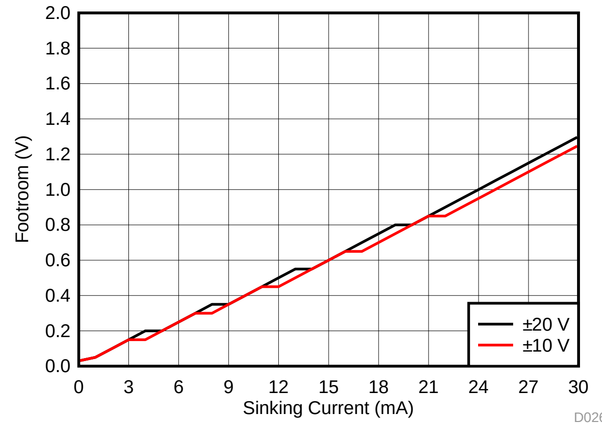
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.



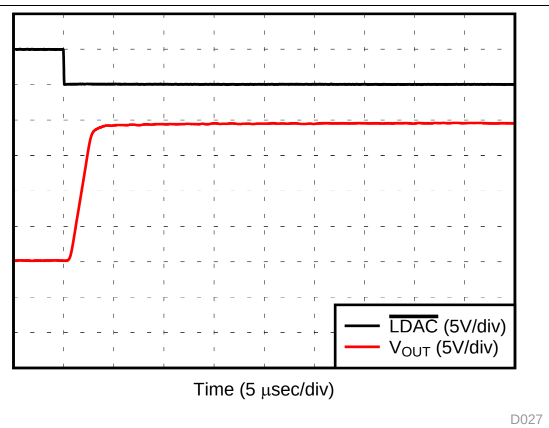
Full-scale Code

Figure 25. V_{CC} Headroom vs Sourcing Current



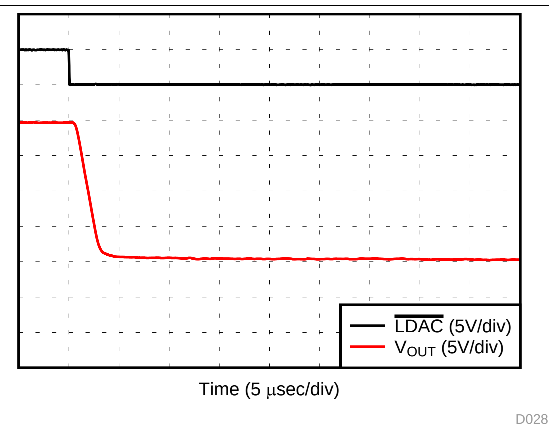
Zero Code

Figure 26. V_{SS} Footroom vs Sinking Current



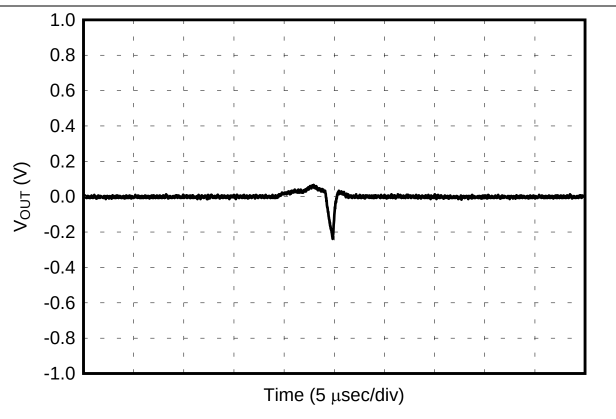
±20-V Output Range

Figure 27. Full-Scale Settling Time, Rising Edge



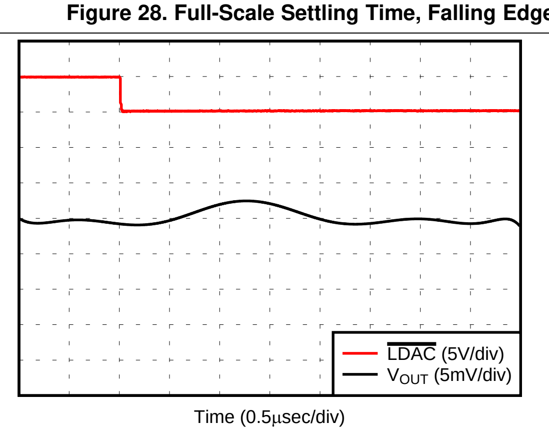
±20-V Output Range

Figure 28. Full-Scale Settling Time, Falling Edge



Power-down to Active DAC Mode
±20-V Output Range

Figure 29. DAC Output Enable Glitch

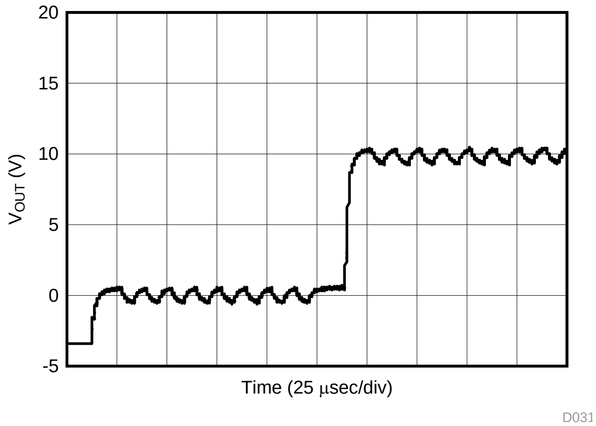


0 to 5-V Output Range

Figure 30. Glitch Impulse, 1 LSB Step

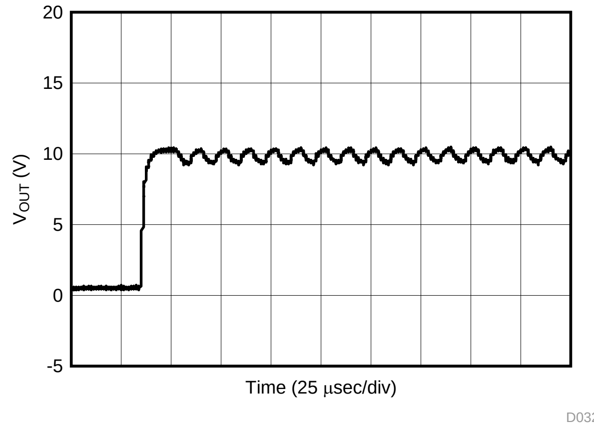
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.



±20-V Output Range
Toggle signal: 1 V_{PP}
DC Change: Midscale to 3/4 Full-scale

Figure 31. Toggle Output Change Response



±20-V Output Range
Toggle signal: 1 V_{PP}
DC value: 3/4 Full-scale

Figure 32. Toggle Enable Response

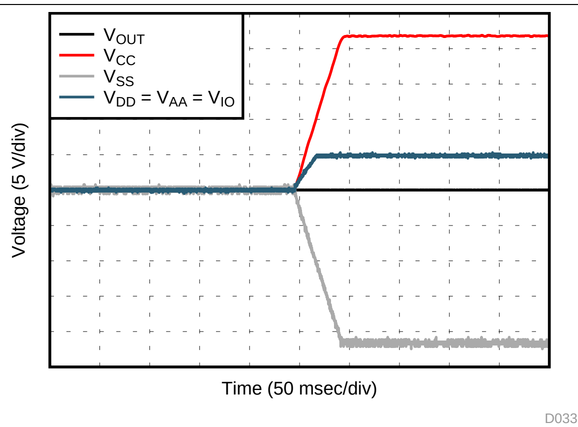


Figure 33. Power-Up Response

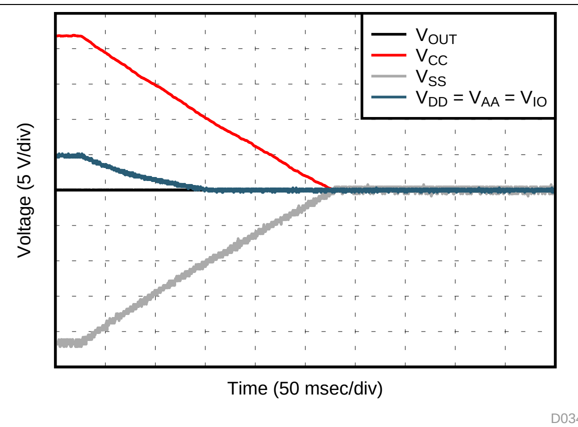
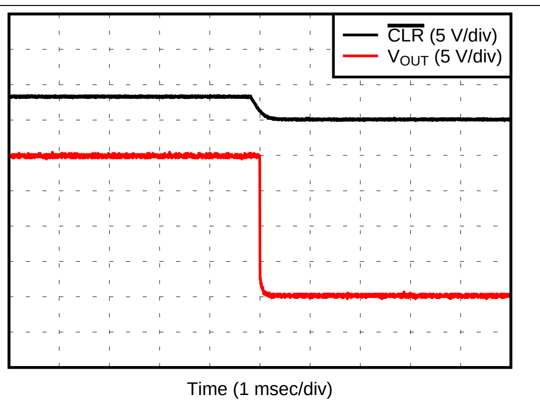
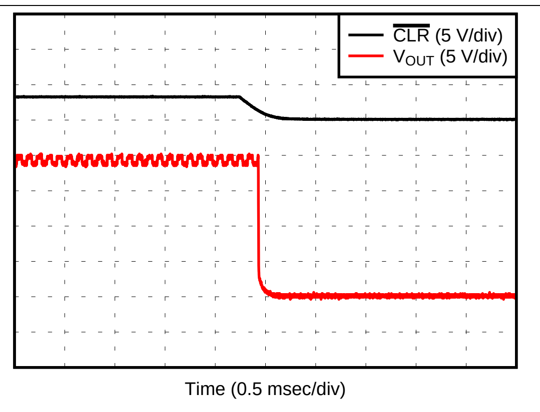


Figure 34. Power-Down Response



±20-V Output Range
Full-scale Code to 0 V

Figure 35. Clear Command Response

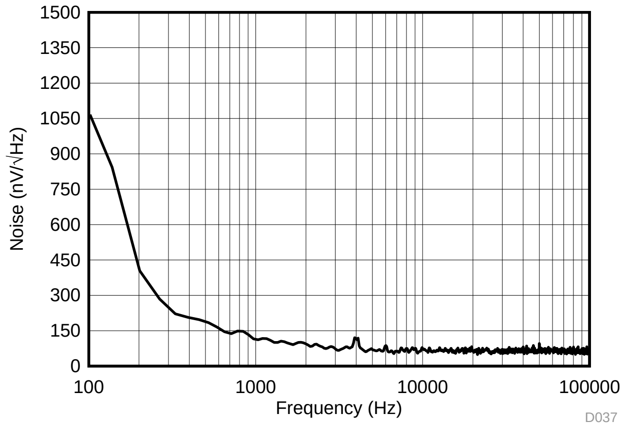


±20-V Output Range
Toggle signal: 1 V_{PP}
DC value at 20 V

Figure 36. Clear Command Response in Toggle Mode

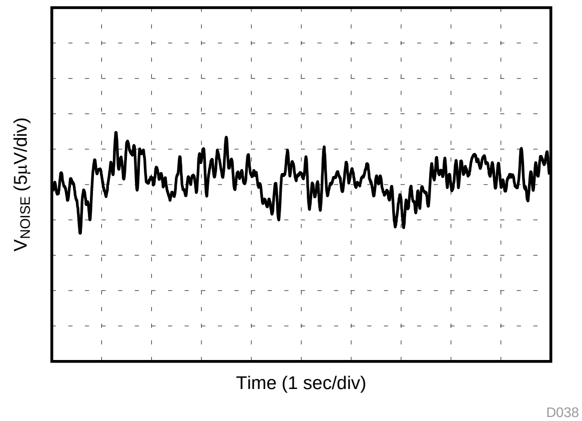
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. Bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.



0 to 5-V Output Range
Midscale Code

Figure 37. DAC Output Noise Density vs Frequency



0 to 5-V Output Range
Midscale Code

Figure 38. DAC Output Noise

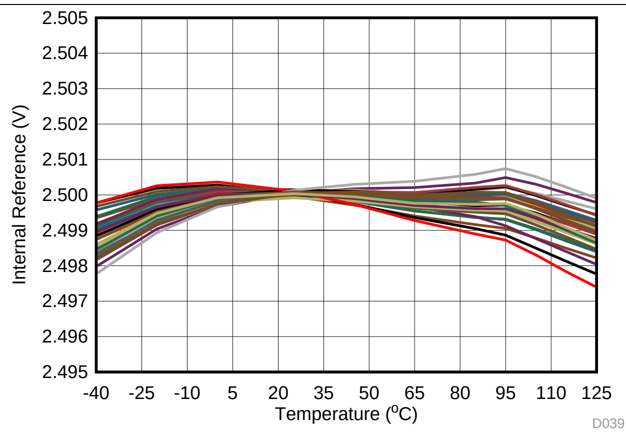


Figure 39. Internal Reference Voltage vs Temperature

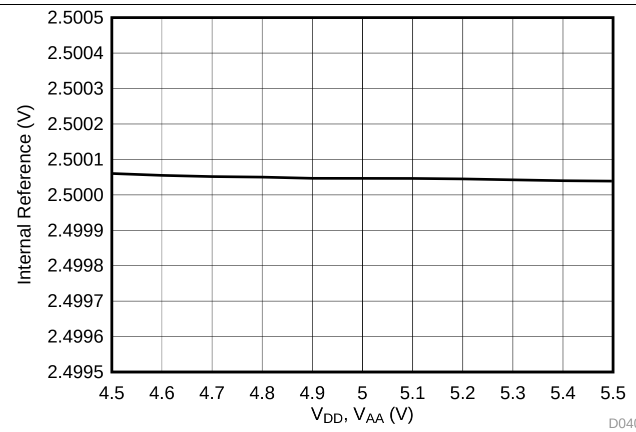


Figure 40. Internal Reference Voltage vs Supply Voltage

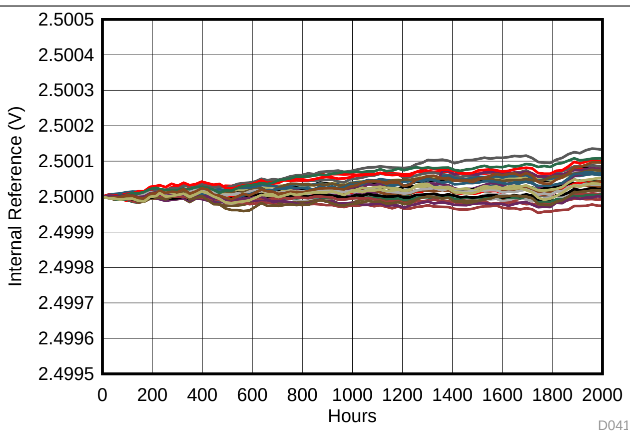


Figure 41. Internal Reference Voltage vs Time

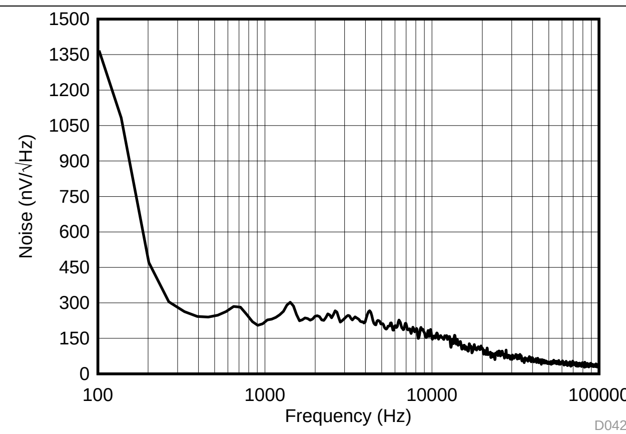


Figure 42. Internal Reference Noise Density vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V. Unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. Bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

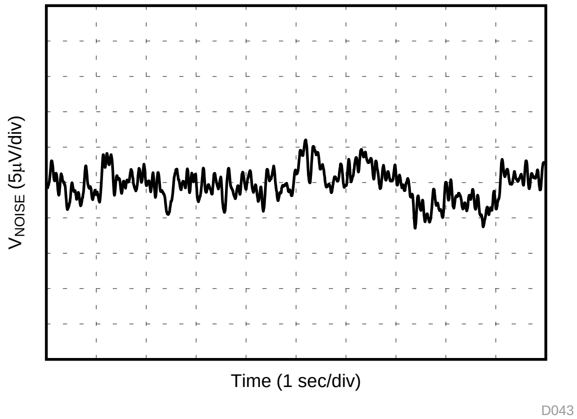


Figure 43. Internal Reference Noise

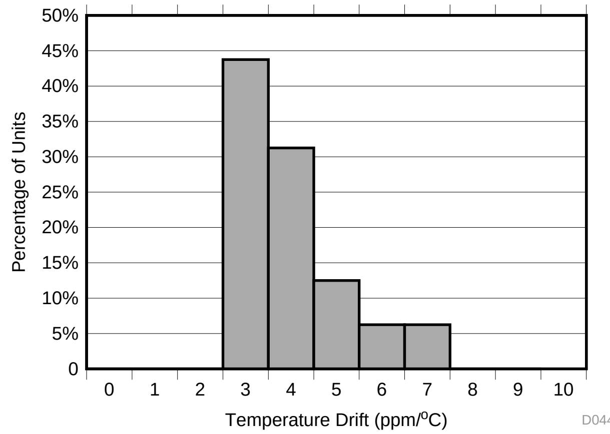


Figure 44. Internal Reference Temperature Drift Histogram

8 Parameter Measurement Information

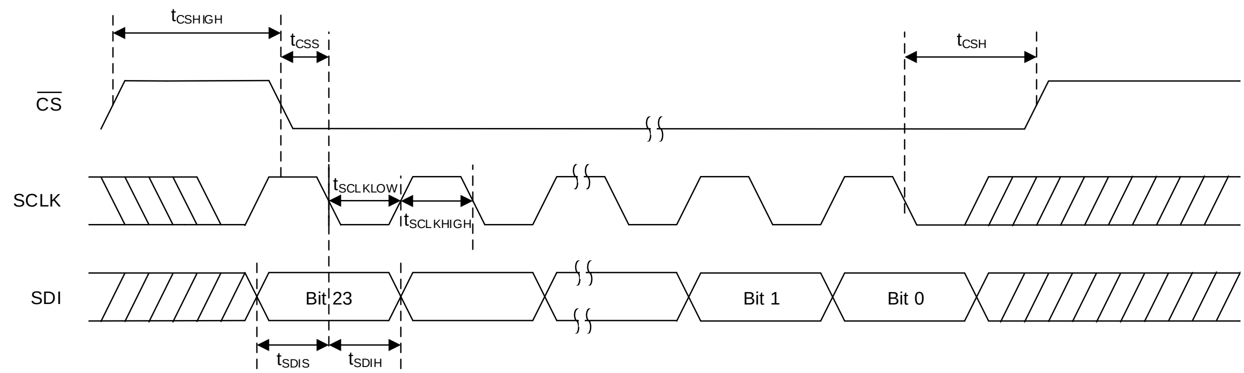


Figure 45. Serial Interface Write Timing Diagram

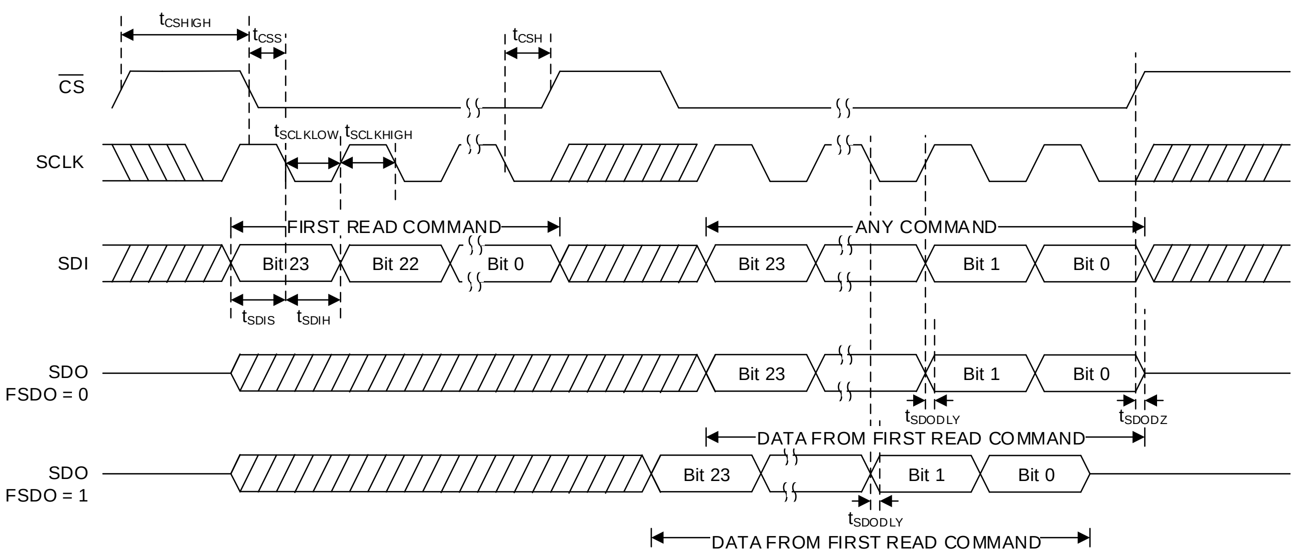


Figure 46. Serial Interface Read Timing Diagram

9 Detailed Description

9.1 Overview

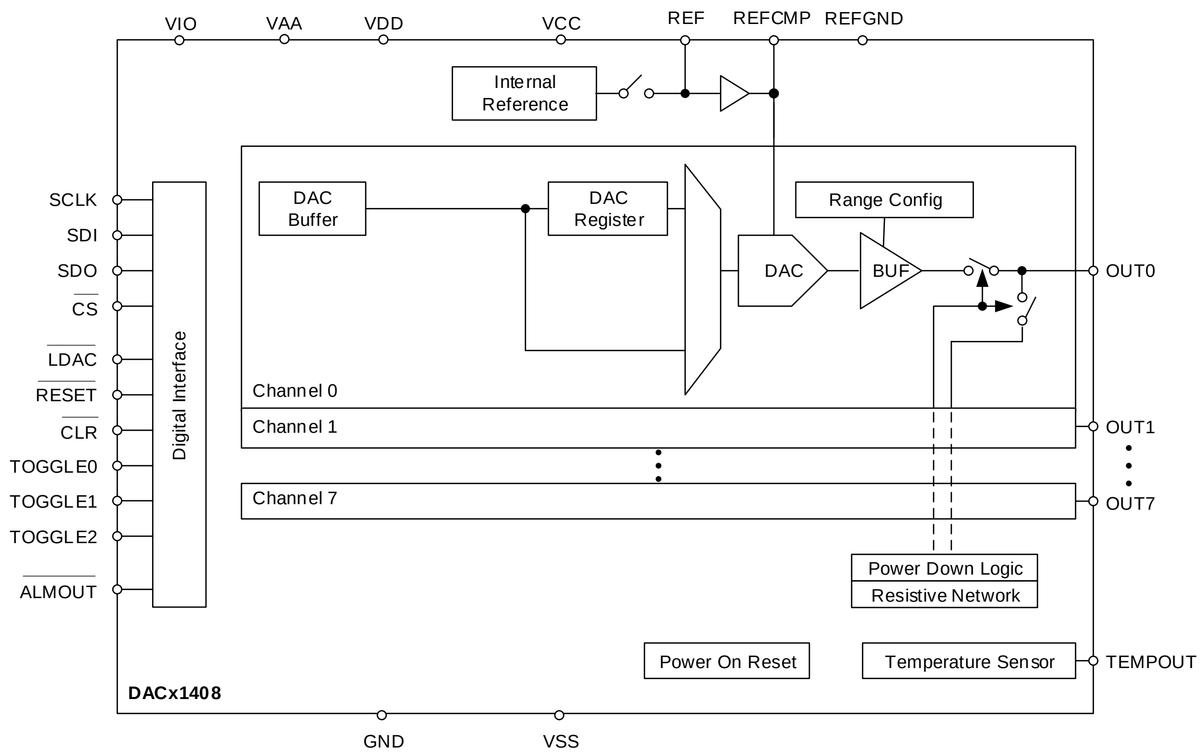
The DACx1408 is a pin-compatible family of 8-channel, buffered, high-voltage output digital-to-analog converters (DACs) with 16-, 14- and 12-bit resolution. The DACx1408 includes a 2.5-V internal reference. A user selectable output configuration enables full-scale bipolar output voltages: ±20 V, ±10 V, ±5 V or ±2.5 V and full-scale unipolar output voltages: 40 V, 20 V, 10 V or 5 V. The full-scale output range for each DAC channel is independently programmable. In addition, each pair of DAC channels can be configured to provide a differential output. Three dedicated A-B toggle pins enable dither signal generation with up to three possible frequencies.

The DACx1408 operates from five supply voltages: V_{DD}, V_{AA}, V_{CC}, V_{SS} and V_{IO}. V_{DD} and V_{AA} are the digital and analog supplies for the DACs, internal reference and other low voltage components and must be set at the same potential. V_{CC} and V_{SS} are the positive and analog supplies for the DAC output amplifiers. V_{IO} sets the logic levels for the digital inputs and outputs.

Communication to the DACx1408 is performed through a 4-wire serial interface that supports stand-alone and daisy-chain operation. The optional frame-error checking provides added robustness to the DACx1408 serial interface.

The DACx1408 incorporates a power-on-reset circuit that connects the DAC outputs to ground at power-up. The outputs remain at this state until the device registers are properly configured for operation.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Digital-to-Analog Converters (DACs) Architecture

Each output channel in the DACx1408 consists of an R-2R ladder architecture followed by an output buffer amplifier capable of rail-to-rail operation. The output amplifiers can drive 25 mA with 1.5-V headroom from either V_{CC} or V_{SS} while maintaining the specified TUE specification for the device. The full-scale output voltage for each channel can be individually configured to the following ranges:

- -20 V to +20 V
- -10 V to +10 V
- -5 V to +5 V
- -2.5 V to +2.5 V
- 0 V to +40V
- 0 V to +20 V
- 0 V to +10 V
- 0 V to +5 V

Figure 47 shows a block diagram of the DAC architecture.

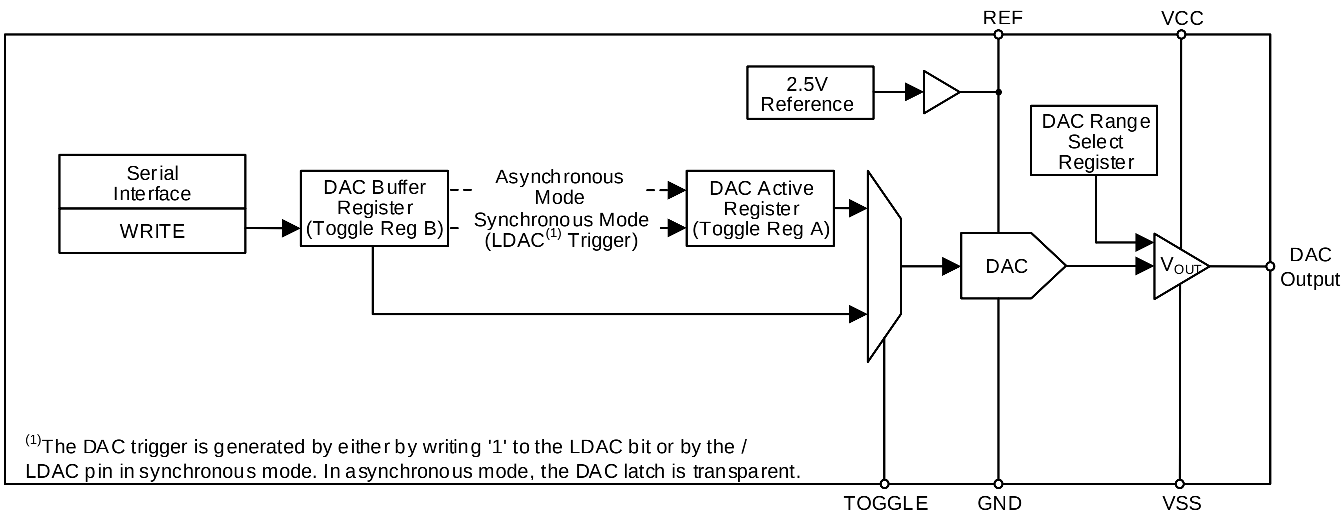


Figure 47. DACx1408 DAC Block Diagram

9.3.1.1 DAC Transfer Function

The input data are written to the individual DAC Data registers in straight binary format for all output ranges. The DAC transfer function is given by Equation 1.

$$V_{OUT} = \left(\frac{CODE}{2^n} \times FSR \right) + V_{MIN} \quad (1)$$

where

- CODE is the decimal equivalent of the binary code that is loaded to the DAC register. CODE range is from 0 to $2^n - 1$.
- n is the DAC resolution in bits. Either 12 (DAC61408), 14 (DAC71408) or 16 (DAC81408).
- FSR is the DAC full-scale range. Equal to $V_{MAX} - V_{MIN}$ for the selected DAC output range.
- V_{MIN} is the lowest voltage for the selected DAC output range.

Feature Description (continued)

9.3.1.2 DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be configured to happen immediately (asynchronous mode) or initiated by a DAC trigger signal (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to the new values.

After a power-on or reset event, all DAC registers are set to zero code, the DAC output amplifiers are powered down, and the DAC outputs are clamped to ground.

9.3.1.2.1 DAC Register Synchronous and Asynchronous Updates

The update mode for each DAC channel is determined by the status of its corresponding SYNC-EN bit. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on a $\overline{CS}$ rising edge. In synchronous mode, writing to the DAC data register doe not automatically update the DAC output. Instead the update occurs only after a trigger event. A DAC trigger signal is generated either through the LDAC bit or by the $\overline{LDAC}$ pin. The synchronous update mode enables simultaneous update of multiple DAC outputs. In both update modes a minimum wait time of 1 µs is required between DAC output updates.

9.3.1.2.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write. Broadcast operation is only possible when all DAC channels are in single-ended mode operation. If one or more outputs are configured in differential mode the broadcast command is ignored.

Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BRDCAST-EN bit. A register write to the BRDCAST-DATA register forces those DAC channels that have been configured for broadcast operation to update their DAC buffer registers to this value. The DAC outputs update to the broadcast value according to their synchronous mode configuration.

9.3.1.2.3 Clear DAC Operation

The DAC outputs are set in clear mode through the $\overline{CLEAR}$ pin. In clear mode each DAC data channel is set to the clear code associated with its configuration as shown in . A $\overline{CLR}$ pin logic low forces all DAC channels to clear the contents of their buffer and active registers to the clear code, and sets the analog outputs accordingly regardless of their synchronization setting.

Table 1. Clear DAC Value

UNIPOLAR / BIPOLAR RANGE	DIFFERENTIAL MODE	CLEAR CODE
Unipolar	No	Zero code
Unipolar	Yes	Midscale code
Bipolar	No	Midscale code
Bipolar	Yes	Midscale code

When a DAC is operating in toggle mode, a clear command sets both toggle registers to the clear value.

9.3.2 Internal Reference

The DAx1408 include a 2.5-V bandgap reference with a typical temperature drift of 5 ppm/ºC. The internal reference is externally available at the REF pin. An external buffer amplifier with a high impedance input is required to drive any external load.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering. A compensation capacitor (330 pF, typical) should be connected between the REFCMP pin and REFGND.

Operation from an external reference is also supported by powering down the internal reference. The external reference is applied to the REF pin.

9.3.3 Device Reset Options

9.3.3.1 Power-on-Reset (POR)

The DACx1408 includes a power-on reset function. After the supplies have been established, a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 1 ms power-on-reset delay. After a POR event, the device is set in power-down mode where all DAC channels and internal reference are powered down and the DAC output pins are connected to ground through a 10-kΩ internal resistor.

9.3.3.2 Hardware Reset

A device hardware reset event is initiated by a minimum 500 ns logic low on the $\overline{\text{RESET}}$ pin. A hardware reset initiates a POR event.

9.3.3.3 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the $\overline{\text{CS}}$ rising edge of the instruction. A software reset initiates a POR event.

9.3.4 Thermal Protection

Due to the DACx1408 DAC channel density and high drive capability it is important to understand the effects of power dissipation on the temperature of the device and ensure it does not exceed the maximum junction temperature.

9.3.4.1 Analog Temperature Sensor: TEMPOUT Pin

The DACx1408 includes an analog temperature monitor with an unbuffered output voltage that is inversely proportional to the device junction temperature. The TEMPOUT pin output voltage has a temperature slope of -4 mV/°C and a 1.34-V offset as described by Equation 2.

$$V_{TEMPOUT} = \left(\frac{-4\ \text{mV}}{°\text{C}} \times T \right) + 1.34\ \text{V} \quad (2)$$

where:

- T is the device junction temperature in °C.
- $V_{TEMPOUT}$ is the temperature monitor output voltage.

9.3.4.2 Thermal Shutdown

The DACx1408 incorporates a thermal shutdown that is triggered when the die temperature exceeds 140ºC. A thermal shutdown sets the TEMP-ALM bit and causes all DAC outputs to power-down, however the internal reference remains powered on. The $\overline{\text{ALMOUT}}$ pin can be configured to monitor a thermal shutdown condition by setting the TEMPALM-EN bit. Once a thermal shutdown is triggered, the device stays in shutdown even after the device temperature lowers.

The die temperature must fall below 140ºC before the device can be returned to normal operation. To resume normal operation, the thermal alarm must be cleared through the ALM-RESET bit while the DAC channels are in power-down mode.

9.4 Device Functional Modes

9.4.1 Toggle Mode

Each DAC in the device can be independently configured to operate in toggle mode. A DAC channel in toggle mode incorporates two DAC registers (Register A and Register B) and can be set to switch repetitively between these two values. The DACx1408 toggle mode operation can be configured to introduce a dither signal to the DAC output, to generate a periodic signal or to implement ON/OFF signaling, among some examples.

To update the toggle registers the following sequence should be followed:

1. Set DAC channel in synchronous mode and disable toggle mode for that channel
2. Write the desired Register A value to the DAC data register
3. Issue a DAC trigger signal to load Register A
4. Write the desired Register B value to the DAC data register
5. Enable toggle mode to load Register B

Once both registers are loaded with data, any of the three TOGGLE[2:0] pins can be used to switch those DACs configured for toggle operation back and forth between the contents of their two DAC specific registers by using an external clock or logic signal. A TOGGLE pin logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. The three TOGGLE[2:0] pins give the DACx1408 the option to operate with up to three toggle rates.

Additionally, the device can be configured for software controlled toggle operation by setting the SOFTTOGGLE-EN bit. In this mode, any of the three AB-TOG[2:0] bits can be used as a toggle control signal. Setting the ABTOG bit to 1 enables Register B and clearing it to 0 enables Register A.

9.4.2 Differential Mode

Each pair of DAC channels in the device can be independently configured to operate as a differential output pair. The differential output of a *DACx-y* pair is updated by writing to the *DACx* channel. For proper operation, the two DAC pairs must be configured to the same output range prior to enabling differential mode. Figure 48 and Figure 49 show the ideal differential output voltages (V_{DIFF}) and common mode voltages (V_{CM}) for a DAC differential pair configured for ±20-V and 0 to 40-V operation, respectively.

Once configured as a differential output, the *DACx-y* pair can be set for toggle operation by updating the *DACx* toggle registers as described in Toggle Mode.

Imbalances between the two differential signals result in common-mode and amplitude errors. The device incorporates an offset register that enables the user to introduce a voltage offset to the *DACy* channel of the *DACx-y* differential pair to compensate for a DC offset error between the two channels. The offset compensation gives a ±0.2%FSR adjustment window. The differential DAC data register must be rewritten after an update to the offset register.

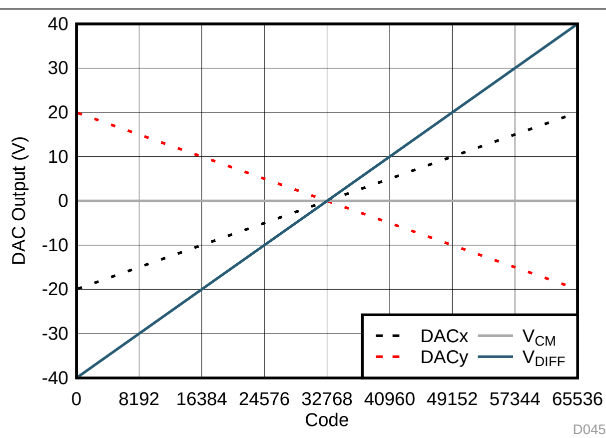


Figure 48. Differential Bipolar Output (16-Bit): ±20-V Output Range

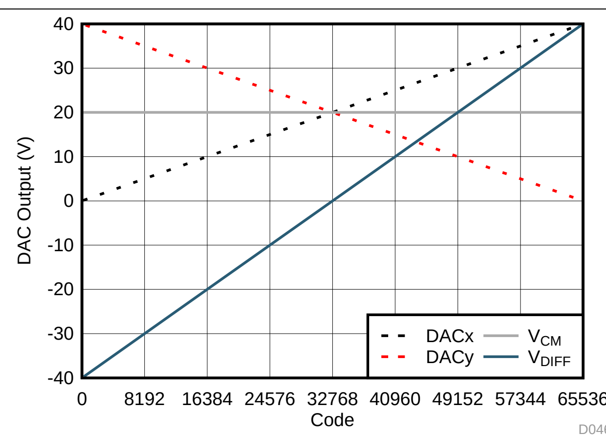


Figure 49. Differential Unipolar Output (16-Bit): 0 to 40-V Output Range

Device Functional Modes (continued)

9.4.3 Power-Down Mode

The DACx1408 DAC output amplifiers and internal reference power-down status can be individually configured and monitored though the PWDWN registers. Setting a DAC channel in power-down mode disables the output amplifier and clamps the output pin to ground through an internal 10-kΩ resistor.

The DAC data registers are not cleared when the DAC goes into power-down which makes it possible to have the same output voltage upon return to normal operation. The DAC data registers can also be updated while in power-down mode.

After a power-on or reset event all the DAC channels and the internal reference are in power-down mode. The entire device can be configured into power-down or active modes through the DEV-PWDWN bit.

9.5 Programming

The DACx1408 is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the DACx1408 registers and can be configured to daisy-chain multiple devices for write operations. The DACx1408 incorporates an optional error checking mode to validate SPI data communication integrity in noisy environments.

9.5.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled, thus the $\overline{CS}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is de-asserted high. If the access cycle contains less than then minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 or 32 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO is in a Hi-Z state.

In an error checking disabled access cycle (24 bits long) the first byte input to SDI is the instruction cycle which identifies the request as a read or write command and the 6-bit address to be accessed. The last 16 bits in the cycle form the data cycle.

Table 2. Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22	x	Don't care bit.
21-16	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
15-0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. Data are clocked out on SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

Table 3. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW from previous access cycle.
22	x	Echo bit 22 from previous access cycle.
21-16	A[5:0]	Echo address from previous access cycle.
15-0	DO[15:0]	Readback data requested on previous access cycle.

9.5.1.1 Streaming Mode Operation

Since updating the eight channels data registers requires a large amount of data to be passed to the device, the device supports streaming mode. In streaming mode the DAC data registers can be written to the device without providing an instruction command for each data register. Streaming mode is enabled by setting the STREN bit. Once enabled the streaming operation is implemented by holding the $\overline{CS}$ active and continuing to shift new data into the device.

The instruction cycle includes the starting address. The device starts writing to this address and automatically increments the address as long as $\overline{CS}$ is asserted. If the last DAC data register address has been reached and $\overline{CS}$ is still asserted, the additional data is ignored by the device.

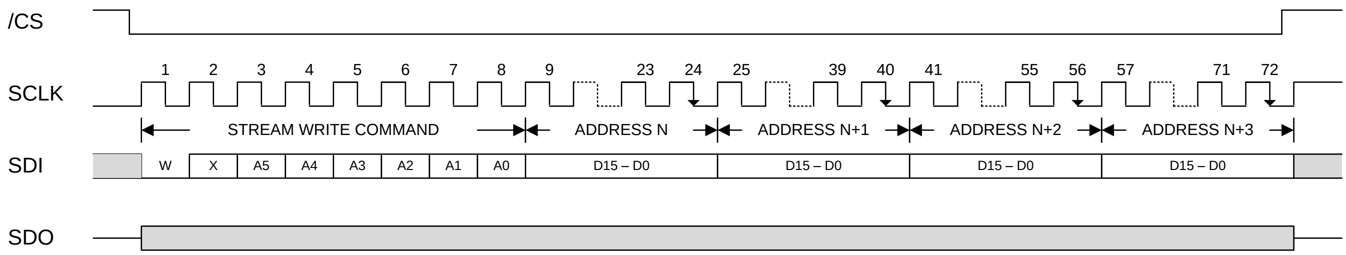


Figure 50. Serial Interface Streaming Write Cycle

9.5.2 Daisy-Chain Operation

For systems that contain more than one DACx1408 devices, the SDO pin can be used to daisy-chain them together. The SDO pin must be enabled by setting the SDO-EN bit before initiating the daisy-chain operation. Daisy-chain operation is useful in reducing the number of serial interface lines.

The first falling edge on the $\overline{CS}$ pin starts the operation cycle. If more than 24 SCLK pulses are applied while the $\overline{CS}$ pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of DACx1408 devices in the daisy chain. When the serial transfer to all devices is complete the $\overline{CS}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal registers of each device in the daisy chain and prevents any further data from being clocked into the input shift register. Daisy-chain operation is not supported while in streaming mode.

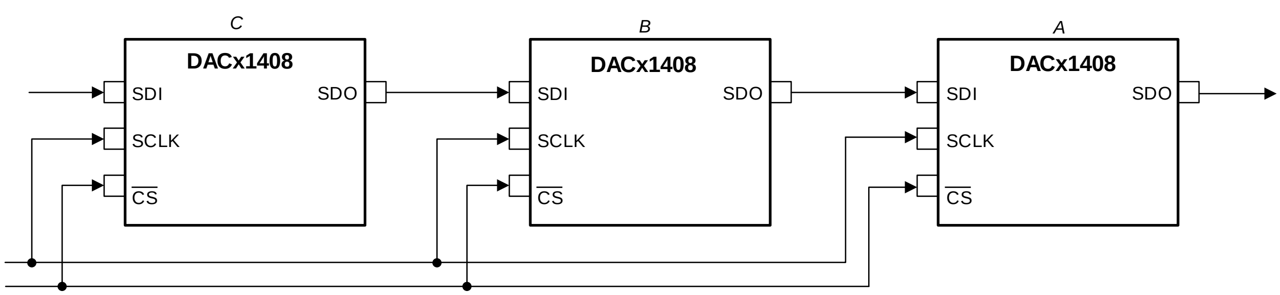


Figure 51. Daisy-Chain Layout

9.5.3 Frame Error Checking

If the DACx1408 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature is enabled by setting the CRC-EN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data is appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. In all serial interface readback operations the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

Table 4. Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29-24	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
23-8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.
7-0	CRC	8-bit CRC polynomial.

The DACx1408 decodes the 32-bit access cycle to compute the CRC remainder on CS rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking results (CRC-ERROR bit) on the SDO pin.

If there is a CRC error, the CRC-ALM bit of the status register is set to 1. The $\overline{\text{ALMOUT}}$ pin can be configured to monitor a CRC error by setting the CRCALM-EN bit.

Table 5. Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Echo data from previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

As in the case of a write operation failing the CRC check, the CRC-ALM bit of the status register is set to 1 and the $\overline{\text{ALMOUT}}$ pin, if configured for CRC alerts, is set low.

Table 6. Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 1).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Echo data from previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

9.6 Register Maps

Table 7 lists the memory-mapped registers for the device. All register offset addresses not listed in Table 7 should be considered as reserved locations and the register contents should not be modified.

Table 7. DACx1408 Registers

Offset	Acronym	Register Name	Section
00h	NOP	NOP Register	Go
01h	DEVICEID	Device ID Register	Go
02h	STATUS	Status Register	Go
03h	SPICONFIG	SPI Configuration Register	Go
04h	GENCONFIG	General Configuration Register	Go
05h	BRDCONFIG	Broadcast Configuration Register	Go
06h	SYNCCONFIG	Sync Configuration Register	Go
07h	TOGGCONFIG0	DAC[7:4] Toggle Configuration Register	Go
08h	TOGGCONFIG1	DAC[3:0] Toggle Configuration Register	Go
09h	DACPWDWN	DAC Power-Down Register	Go
0Bh	DACRANGE0	DAC[7:4] Range Register	Go
0Ch	DACRANGE1	DAC[3:0] Range Register	Go
0Eh	TRIGGER	Trigger Register	Go
0Fh	BRDCAST	Broadcast Data Register	Go
14h	DAC0	DAC0 Data Register	Go
15h	DAC1	DAC1 Data Register	Go
16h	DAC2	DAC2 Data Register	Go
17h	DAC3	DAC3 Data Register	Go
18h	DAC4	DAC4 Data Register	Go
19h	DAC5	DAC5 Data Register	Go
1Ah	DAC6	DAC6 Data Register	Go
1Bh	DAC7	DAC7 Data Register	Go
21h	OFFSET0	DAC[6-7;4-5] Differential Offset Register	Go
22h	OFFSET1	DAC[2-3;0-1] Differential Offset Register	Go

Complex bit access types are encoded to fit into small table cells. Table 8 shows the codes that are used for access types in this section.

Table 8. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

9.6.1 NOP Register (Offset = 00h) [reset = 0000h]

NOP is shown in Figure 52 and described in Table 9.

Return to Summary Table.

Figure 52. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
W-0h															

Table 9. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	W	0h	No operation. Write 0000h for proper no-operation command.

9.6.2 DEVICEID Register (Offset = 01h) [reset = ----h]

DEVICEID is shown in Figure 53 and described in Table 10.

Return to Summary Table.

Figure 53. DEVICEID Register

15	14	13	12	11	10	9	8
DEVICEID							
R----h							
7	6	5	4	3	2	1	0
DEVICEID						VERSIONID	
R----h						R-0h	

Table 10. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	DEVICEID	R	---h	Device ID DAC81408: 298h DAC71408: 288h DAC61408: 248h
1-0	VERSIONID	R	0h	Version ID. Subject to change.

9.6.3 STATUS Register (Offset = 02h) [reset = 0000h]

STATUS is shown in Figure 54 and described in Table 11.

Return to Summary Table.

Figure 54. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CRC-ALM	DAC-BUSY	TEMP-ALM
R-0h					R-0h	R-0h	R-0h

Table 11. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	This bit is reserved.
2	CRC-ALM	R	0h	CRC-ALM = 1 indicates a CRC error.
1	DAC-BUSY	R	0h	DAC-BUSY = 1 indicates DAC registers are not ready for updates.
0	TEMP-ALM	R	0h	TEMP-ALM = 1 indicates die temperature is over +140°C. A thermal alarm event forces the DAC outputs to go into power-down mode.

9.6.4 SPICONFIG Register (Offset = 03h) [reset = 0A24h]

SPICONFIG is shown in Figure 55 and described in Table 12.

Return to Summary Table.

Figure 55. SPICONFIG Register

15	14	13	12	11	10	9	8
RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED
R-0h				R/W-1h	R/W-0h	R/W-1h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	SOFTTOGGLE-EN	DEV-PWDWN	CRC-EN	STR-EN	SDO-EN	FSDO	RESERVED
R-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R-0h

Table 12. SPICONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	This bit is reserved.
11	TEMPALM-EN	R/W	1h	When set to 1 a thermal alarm triggers the $\overline{\text{ALMOUT}}$ pin.
10	DACBUSY-EN	R/W	0h	When set to 1 the $\overline{\text{ALMOUT}}$ pin is set between DAC output updates. Contrary to other alarm events, this alarm resets automatically.
9	CRCALM-EN	R/W	1h	When set to 1 a CRC error triggers the $\overline{\text{ALMOUT}}$ pin.
8	RESERVED	R	0h	This bit is reserved.
7	RESERVED	R	1h	This bit is reserved.
6	SOFTTOGGLE-EN	R/W	0h	When set to 1 enables soft toggle operation.
5	DEV-PWDWN	R/W	1h	DEV-PWDWN = 1 sets the device in power-down mode DEV-PWDWN = 0 sets the device in active mode
4	CRC-EN	R/W	0h	When set to 1 frame error checking is enabled.
3	STR-EN	R/W	0h	When set to 1 streaming mode operation is enabled.
2	SDO-EN	R/W	1h	When set to 1 the SDO pin is operational.
1	FSDO	R/W	0h	Fast SDO bit (half-cycle speedup). When 0, SDO updates during SCLK rising edges. When 1, SDO updates during SCLK falling edges.
0	RESERVED	R	0h	This bit is reserved.

9.6.5 GENCONFIG Register (Offset = 04h) [reset = 7F00h]

GENCONFIG is shown in Figure 56 and described in Table 13.

Return to Summary Table.

Figure 56. GENCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	REF-PWDWN	RESERVED					
R-0h	R/W-1h	R-1h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RESERVED	DAC-6-7-DIFF-EN	DAC-4-5-DIFF-EN	DAC-2-3-DIFF-EN	DAC-0-1-DIFF-EN	RESERVED	RESERVED
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h

Table 13. GENCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	This bit is reserved.
14	REF-PWDWN	R/W	1h	REF-PWDWN = 1 powers down the internal reference REF-PWDWN = 0 activates the internal reference
13-8	RESERVED	R	1h	This bit is reserved.
7	RESERVED	R	0h	This bit is reserved.
6	RESERVED	R	0h	This bit is reserved.
5	DAC-6-7-DIFF-EN	R/W	0h	When set to 1 the corresponding DAC pair is set to operate in differential mode. The DAC data registers must be rewritten after enabling or disabling differential operation.
4	DAC-4-5-DIFF-EN	R/W	0h	
3	DAC-2-3-DIFF-EN	R/W	0h	
2	DAC-0-1-DIFF-EN	R/W	0h	
1	RESERVED	R	0h	This bit is reserved.
0	RESERVED	R	0h	This bit is reserved.

9.6.6 BRDCONFIG Register (Offset = 05h) [reset = FFFFh]

BRDCONFIG is shown in Figure 57 and described in Table 14.

Return to Summary Table.

Figure 57. BRDCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	DAC7-BRDCAST-EN	DAC6-BRDCAST-EN	DAC5-BRDCAST-EN	DAC4-BRDCAST-EN
R-1h	R-1h	R-1h	R-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAC3-BRDCAST-EN	DAC2-BRDCAST-EN	DAC1-BRDCAST-EN	DAC0-BRDCAST-EN	RESERVED	RESERVED	RESERVED	RESERVED
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R-1h	R-1h	R-1h	R-1h

Table 14. BRDCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1h	This bit is reserved.
14	RESERVED	R	1h	This bit is reserved.
13	RESERVED	R	1h	This bit is reserved.
12	RESERVED	R	1h	This bit is reserved.
11	DAC7-BRDCAST-EN	R/W	1h	When set to 1 the corresponding DAC is set to update its output to the value set in the BRDCAST register. All DAC channels must be configured in single-ended mode for broadcast operation. If one or more outputs are configured in differential mode the broadcast mode is ignored. When cleared to 0 the corresponding DAC output remains unaffected by a BRDCAST command.
10	DAC6-BRDCAST-EN	R/W	1h	
9	DAC5-BRDCAST-EN	R/W	1h	
8	DAC4-BRDCAST-EN	R/W	1h	
7	DAC3-BRDCAST-EN	R/W	1h	
6	DAC2-BRDCAST-EN	R/W	1h	
5	DAC1-BRDCAST-EN	R/W	1h	
4	DAC0-BRDCAST-EN	R/W	1h	
3	RESERVED	R	1h	This bit is reserved.
2	RESERVED	R	1h	This bit is reserved.
1	RESERVED	R	1h	This bit is reserved.
0	RESERVED	R	1h	This bit is reserved.

9.6.7 SYNCCONFIG Register (Offset = 06h) [reset = 0000h]

SYNCCONFIG is shown in Figure 58 and described in Table 15.

Return to Summary Table.

Figure 58. SYNCCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	DAC7-SYNC-EN	DAC6-SYNC-EN	DAC5-SYNC-EN	DAC4-SYNC-EN
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAC3-SYNC-EN	DAC2-SYNC-EN	DAC1-SYNC-EN	DAC0-SYNC-EN	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h

Table 15. SYNCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	This bit is reserved.
14	RESERVED	R	0h	This bit is reserved.
13	RESERVED	R	0h	This bit is reserved.
12	RESERVED	R	0h	This bit is reserved.
11	DAC7-SYNC-EN	R/W	0h	When set to 1 the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0 the corresponding DAC output is set to update immediately (asynchronous mode).
10	DAC6-SYNC-EN	R/W	0h	
9	DAC5-SYNC-EN	R/W	0h	
8	DAC4-SYNC-EN	R/W	0h	
7	DAC3-SYNC-EN	R/W	0h	
6	DAC2-SYNC-EN	R/W	0h	
5	DAC1-SYNC-EN	R/W	0h	
4	DAC0-SYNC-EN	R/W	0h	
3	RESERVED	R	0h	This bit is reserved.
2	RESERVED	R	0h	This bit is reserved.
1	RESERVED	R	0h	This bit is reserved.
0	RESERVED	R	0h	This bit is reserved.

9.6.8 TOGGCONFIG0 Register (Offset = 07h) [reset = 0000h]

TOGGCONFIG0 is shown in Figure 59 and described in Table 16.

Return to Summary Table.

Figure 59. TOGGCONFIG0 Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED		RESERVED		RESERVED	
R-0h		R-0h		R-0h		R-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAC7-AB-TOGG-EN		DAC6-AB-TOGG-EN		DAC5-AB-TOGG-EN		DAC4-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 16. TOGGCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	This bit is reserved.
13-12	RESERVED	R	0h	This bit is reserved.
11-10	RESERVED	R	0h	This bit is reserved.
9-8	RESERVED	R	0h	This bit is reserved.
7-6	DAC7-AB-TOGG-EN	R/W	0h	Enables toggle mode operation and configures the toggle pin or soft toggle bit: 0h = Toggle mode disabled 1h = Toggle mode enabled: TOGGLE0 2h = Toggle mode enabled: TOGGLE1 3h = Toggle mode enabled: TOGGLE2
5-4	DAC6-AB-TOGG-EN	R/W	0h	
3-2	DAC5-AB-TOGG-EN	R/W	0h	
1-0	DAC4-AB-TOGG-EN	R/W	0h	

9.6.9 TOGGCONFIG1 Register (Offset = 08h) [reset = 0000h]

TOGGCONFIG1 is shown in Figure 60 and described in Table 17.

Return to Summary Table.

Figure 60. TOGGCONFIG1 Register

15	14	13	12	11	10	9	8
DAC3-AB-TOGG-EN		DAC2-AB-TOGG-EN		DAC1-AB-TOGG-EN		DAC0-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RESERVED		RESERVED		RESERVED	
R-0h		R-0h		R-0h		R-0h	

Table 17. TOGGCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DAC3-AB-TOGG-EN	R/W	0h	Enables toggle mode operation and configures the toggle pin or soft toggle bit: 0h = Toggle mode disabled 1h = Toggle mode enabled: TOGGLE0 2h = Toggle mode enabled: TOGGLE1 3h = Toggle mode enabled: TOGGLE2
13-12	DAC2-AB-TOGG-EN	R/W	0h	
11-10	DAC1-AB-TOGG-EN	R/W	0h	
9-8	DAC0-AB-TOGG-EN	R/W	0h	
7-6	RESERVED	R	0h	This bit is reserved.
5-4	RESERVED	R	0h	This bit is reserved.
3-2	RESERVED	R	0h	This bit is reserved.
1-0	RESERVED	R	0h	This bit is reserved.

9.6.10 DACPWDWN Register (Offset = 09h) [reset = FFFFh]

DACPWDWN is shown in Figure 61 and described in Table 18.

Return to Summary Table.

Figure 61. DACPWDWN Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	DAC7-PWDWN	DAC6-PWDWN	DAC5-PWDWN	DAC4-PWDWN
R-1h	R-1h	R-1h	R-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAC3-PWDWN	DAC2-PWDWN	DAC1-PWDWN	DAC0-PWDWN	RESERVED	RESERVED	RESERVED	RESERVED
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R-1h	R-1h	R-1h	R-1h

Table 18. DACPWDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1h	This bit is reserved.
14	RESERVED	R	1h	This bit is reserved.
13	RESERVED	R	1h	This bit is reserved.
12	RESERVED	R	1h	This bit is reserved.
11	DAC7-PWDWN	R/W	1h	When set to 1 the corresponding DAC is in power-down mode and its output is connected to GND through a 10-kΩ internal resistor.
10	DAC6-PWDWN	R/W	1h	
9	DAC5-PWDWN	R/W	1h	
8	DAC4-PWDWN	R/W	1h	
7	DAC3-PWDWN	R/W	1h	
6	DAC2-PWDWN	R/W	1h	
5	DAC1-PWDWN	R/W	1h	
4	DAC0-PWDWN	R/W	1h	
3	RESERVED	R	1h	This bit is reserved.
2	RESERVED	R	1h	This bit is reserved.
1	RESERVED	R	1h	This bit is reserved.
0	RESERVED	R	1h	This bit is reserved.

9.6.11 DACRANGEn Register (Offset = 0Bh - 0Ch) [reset = 0000h]

DACRANGEn is shown in Figure 62 and described in Table 19.

Return to Summary Table.

Figure 62. DACRANGEn Register

15	14	13	12	11	10	9	8
DACa-RANGE[3:0]				DACb-RANGE[3:0]			
W-0h				W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACc-RANGE[3:0]				DACd-RANGE[3:0]			
W-0h				W-0h			

Table 19. DACRANGEn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DACa-RANGE[3:0]	W	0h	Sets the output range for the corresponding DAC. 0000 = 0 to 5 V 0001 = 0 to 10 V 0010 = 0 to 20 V 0100 = 0 to 40 V 1001 = -5 V to +5 V 1010 = -10 V to +10 V 1100 = -20 V to +20 V 1110 = -2.5 V to +2.5 V All others: invalid The two outputs of a differential DAC pair must be configured to the same output range prior to setting them up as a differential pair. a: 7 or 3; b: 6 or 2; c: 5 or 1; d: 4 or 0
11-8	DACb-RANGE[3:0]	W	0h	
7-4	DACc-RANGE[3:0]	W	0h	
3-0	DACd-RANGE[3:0]	W	0h	

9.6.12 TRIGGER Register (Offset = 0Eh) [reset = 0000h]

TRIGGER is shown in Figure 63 and described in Table 20.

Return to Summary Table.

Figure 63. TRIGGER Register

15	14	13	12	11	10	9	8
RESERVED							ALM-RESET
W-0h							W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AB-TOG2	AB-TOG1	AB-TOG0	LDAC	SOFT-RESET[3:0]			
W-0h	W-0h	W-0h	W-0h	W-0h			

Table 20. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	W	0h	This bit is reserved
8	ALM-RESET	W	0h	Set this bit to 1 to clear an alarm event. Not applicable for a DAC-BUSY alarm event.
7	AB-TOG2	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 2 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A.
6	AB-TOG1	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 1 in the TOGGCONFIG register. Set to 1 to updated to Register B and clear to 0 for Register A.
5	AB-TOG0	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 0 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A.
4	LDAC	W	0h	Set this bit to 1 to synchronously load those DACs who have been set in synchronous mode in the SYNCCONFIG register.
3-0	SOFT-RESET[3:0]	W	0h	When set to the reserved code 1010 resets the device to its default state.

9.6.13 BRDCAST Register (Offset = 0Fh) [reset = 0000h]

BRDCAST is shown in Figure 64 and described in Table 21.

Return to Summary Table.

Figure 64. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[15:0]															
R/W-0h															

Table 21. BRDCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BRDCAST-DATA[15:0]	R/W	0h	Writing to the BRDCAST register forces those DAC channels that have been set to broadcast in the BRDCONFIG register to update its active register data to the BRDCAST-DATA one. Data is MSB aligned in straight binary format and follows the format below: DAC81408: { DATA[15:0] } DAC71408: { DATA[13:0], x, x } DAC61408: { DATA[11:0], x, x, x, x} x – Don 't care bits

9.6.14 DACn Register (Offset = 14h - 1Bh) [reset = 0000h]

DACn is shown in Figure 65 and described in Table 22.

Return to Summary Table.

Figure 65. DACn Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACn-DATA[15:0]															
R/W-0h															

Table 22. DACn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DACn-DATA[15:0]	R/W	0h	Stores the 16-, 14- or 12-bit data to be loaded to DACn in MSB aligned straight binary format. In differential DAC mode data is loaded into the lowest-valued DAC in the DAC pair (in pair DAC 01, data is loaded into DAC0 and writes to DAC1 are ignored). Data follows the format below: DAC81408: { DATA[15:0] } DAC71408: { DATA[13:0], x, x } DAC61408: { DATA[11:0], x, x, x, x} x – Don 't care bits

9.6.15 OFFSETn Register (Offset = 21h - 22h) [reset = 0000h]

OFFSETn is shown in Figure 66 and described in Table 23.

Return to Summary Table.

Figure 66. OFFSETn Register

15	14	13	12	11	10	9	8
OFFSETab[7:0]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSETcd[7:0]							
R/W-0h							

Table 23. OFFSETn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	OFFSETab[7:0]	R/W	0h	Provides offset adjustment to DACy in the differential DACx-y pair in two 's complement format. Data follows the format below: • DAC81408: – Format: { OFFSET[7:0] } – Range: -128 LSB to +127 LSB • DAC71408: – Format: { OFFSET[5:0], x, x } – Range: -32 LSB to +31 LSB • DAC61408: – Format: { OFFSET[3:0], x, x, x, x} – Range: -8 LSB to +7 LSB x – Don 't care bits The differential DAC data register must be rewritten after updating the offset register. ab: 6-7 or 2-3; cd: 4-5 or 0-1
7-0	OFFSETcd[7:0]	R/W	0h	

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DACx1408 family provides 8-channel high-voltage and high-current output in both single-ended and differential configurations. The outputs can be configured to multiple ranges and square waves can be generated using the toggle modes. This makes the DAC family suitable for Automatic Test Equipment (ATE) and servo control applications. In addition to these features, the low power-on glitch of this DAC makes it suitable for Motor Control applications like CNC machines as well.

10.2 Typical Application

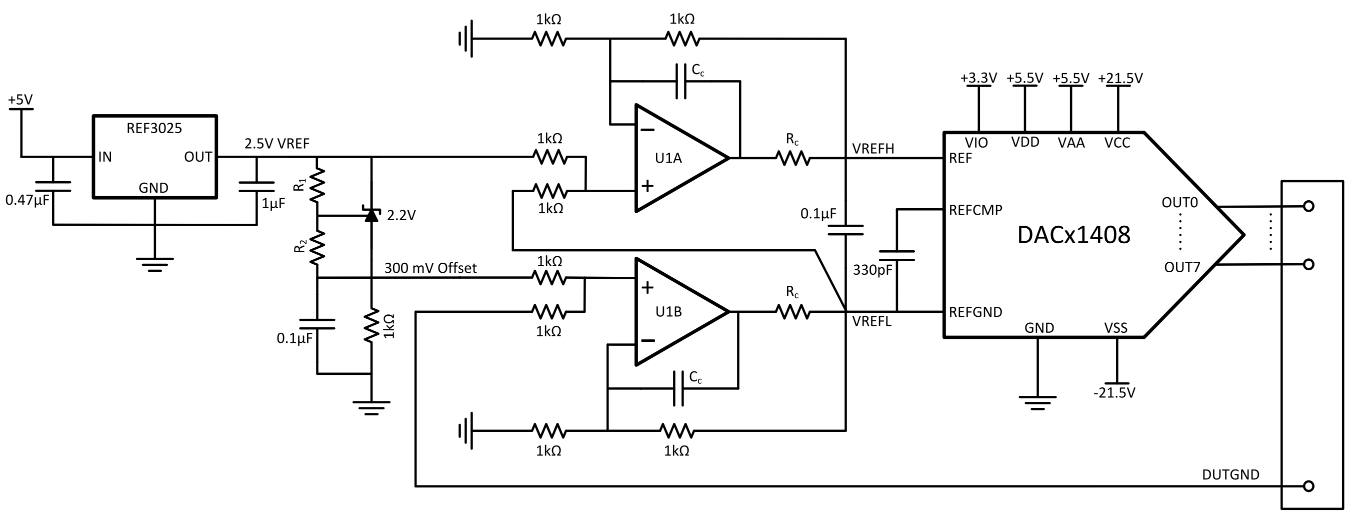


Figure 67. Schematic for Remote Ground Tracking

10.2.1 Design Requirements

In ATE and Motor Control applications, typically the systems are designed modular wherein the control module is located spatially away from the Device Under Test (DUT) module. Such a scheme allows ground potentials across modules to vary due to the impedance of the interconnects. This ground potential variation, in turn introduces inaccuracies to the DAC output when measured with respect to the remote or DUT ground. Figure 67 provides a method to compensate the variations in the remote ground. The ground variation in such applications is typically within ±300 mV that includes DC and 50 Hz/60 Hz mains frequency components. While the best way to handle this variation is to put opamps in level shifter configuration at each output, a low cost and low footprint solution is always preferable. The following sections focus on the latter approach.

Typical Application (continued)

10.2.2 Detailed Design Procedure for Remote Ground Tracking

In order to make the DAC outputs follow the remote ground, the best approach is to level shift the reference input. Figure 67 depicts a method wherein both the REF and REFGND inputs are level shifted with respect to DUTGND. However, as the DAC doesn't allow the REFGND to become negative compared to GND, an offset voltage of 300mV needs to be applied as shown. This method requires an external 2.5V reference and a way to generate a stable 300-mV reference. A dual opamp U1 is used to shift both REFGND and REF by (DUTGND + 300-mV offset). Table 24 provides the nodal analysis of the circuit. As evident, the DAC outputs track the DUTGND with an offset of 300mV. This offset can be easily compensated in software. Note that the absolute max values between REFGND and GND must be respected. When the absolute max values are reached, they should only be for a transient period and not for sustained amount of time.

Table 24. Nodal Analysis of the Circuit

DUTGND (GND±0.3V)	REFGND PIN	REF PIN	VOUT-GND AT 0V CODE	VOUT-GND AT 5V CODE	VOUT-DUTGND AT 0V CODE	VOUT-DUTGND AT 5V CODE
0V	0.3V	2.8V	0.3V	5.3V	0.3V	5.3V
0.3V	0.6V	3.1V	0.6V	5.6V	0.3V	5.3V
-0.3V	0V	2.5V	0V	5V	0.3V	5.3V

10.2.2.1 Generating 300mV Offset

There is no off-the-shelf solution for generating a 300-mV offset, unfortunately. Figure 67 depicts a method to generate it using discrete components. It uses LM4041 adjustable shunt regulator on high-side from the 2.5-V reference. It has a reference input pin that sets the voltage across this device. Given that V_{Ref} is 1.233 V, choosing R1 = 16 kΩ and R2 = 12 kΩ the voltage V_o can be calculated by superposition as 2.16 V. This will provide an offset of (2.5 V – 2.16 V) = 340 mV that will provide a safe margin from DAC ground.

10.2.2.2 Amplifier Selection

The amplifier needs to be bipolar in order to operate linearly near ground. A dual package is preferable for optimizing area. Considering these factors, TLV2442A seems to be the best option from cost and accuracy points of view. Other parts like OPA2277 can be used when higher accuracy is required.

10.2.2.3 Passive Component Selection

In order to minimize additional offset and gain error the gain resistors around the opamps need to be matched. An 8-channel resistor network can be used for better matching. R_c and C_c values can be chosen as 22 Ω and 1000 pF, respectively in order to compensate the pole caused by the large bypass capacitor at the opamp outputs.

10.2.3 Application Curves

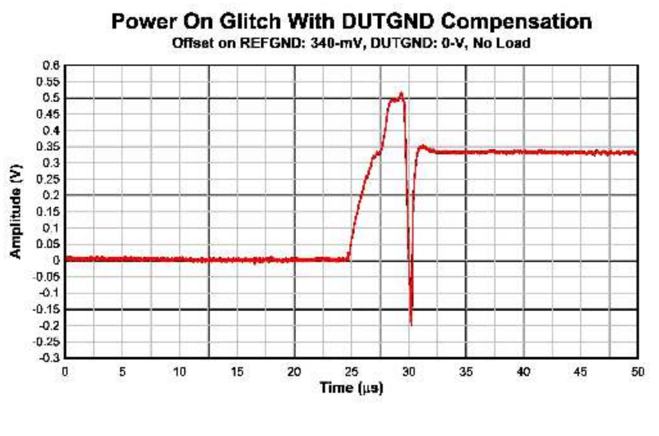


Figure 68. Power-On Glitch With DUTGND Compensation

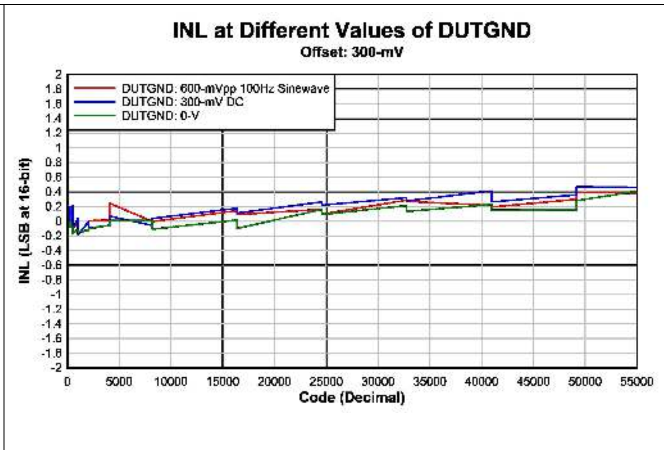


Figure 69. INL (Major Code) at Different Values of DUTGND

11 Power Supply Recommendations

The DACx1408 requires 5 power supply inputs: VIO, VDD, VAA, VCC and VSS. VDD and VAA should be at same level. Assuming VIO and VDD/VAA to be different, there are 4 separate power supply sources required. It is recommended to provide a 0.1-µF ceramic capacitor close to each power supply pin. Please note that VCC and VSS have 2 pins each. In addition, a 4.7-µF or 10-µF bulk capacitor is recommended for each power supply. Tantalum or aluminum types can be chosen for the bulk capacitors. There is no sequencing requirement for the power supplies. As the DAC output range is configurable, the power supply headroom should be taken care of for achieving linearity at codes close to power supply rails. When sourcing or sinking current from or to the DAC output, the heat dissipation needs to be considered. For example, a typical application of MZM bias with 25-mA load current from or to 12 channels with 2.5-V power supply headroom can create a power dissipation across the DAC of (12*2.5*25 mA) = 0.75 W. The thermal design to dissipate this much of power may involve inclusion of heat sinks in order to avoid thermal shutdown of the device.

12 Layout

12.1 Layout Guidelines

The pin out of DACx1408 has been designed in such a way that the analog, digital and power pins are spatially separated from each other, which makes the PCB layout simple. An example layout is shown in Figure 70. As evident, every power supply pin has a 0.1-µF capacitor close to it. The layout of the analog and digital signals should be laid out away from each other or on different PCB layers. It is recommended to provide an unbroken reference plane (either ground or VIO) for the digital signals. The higher frequency signals such as SCLK and SDI should have appropriate impedance termination in order to address signal integrity.

12.2 Layout Example

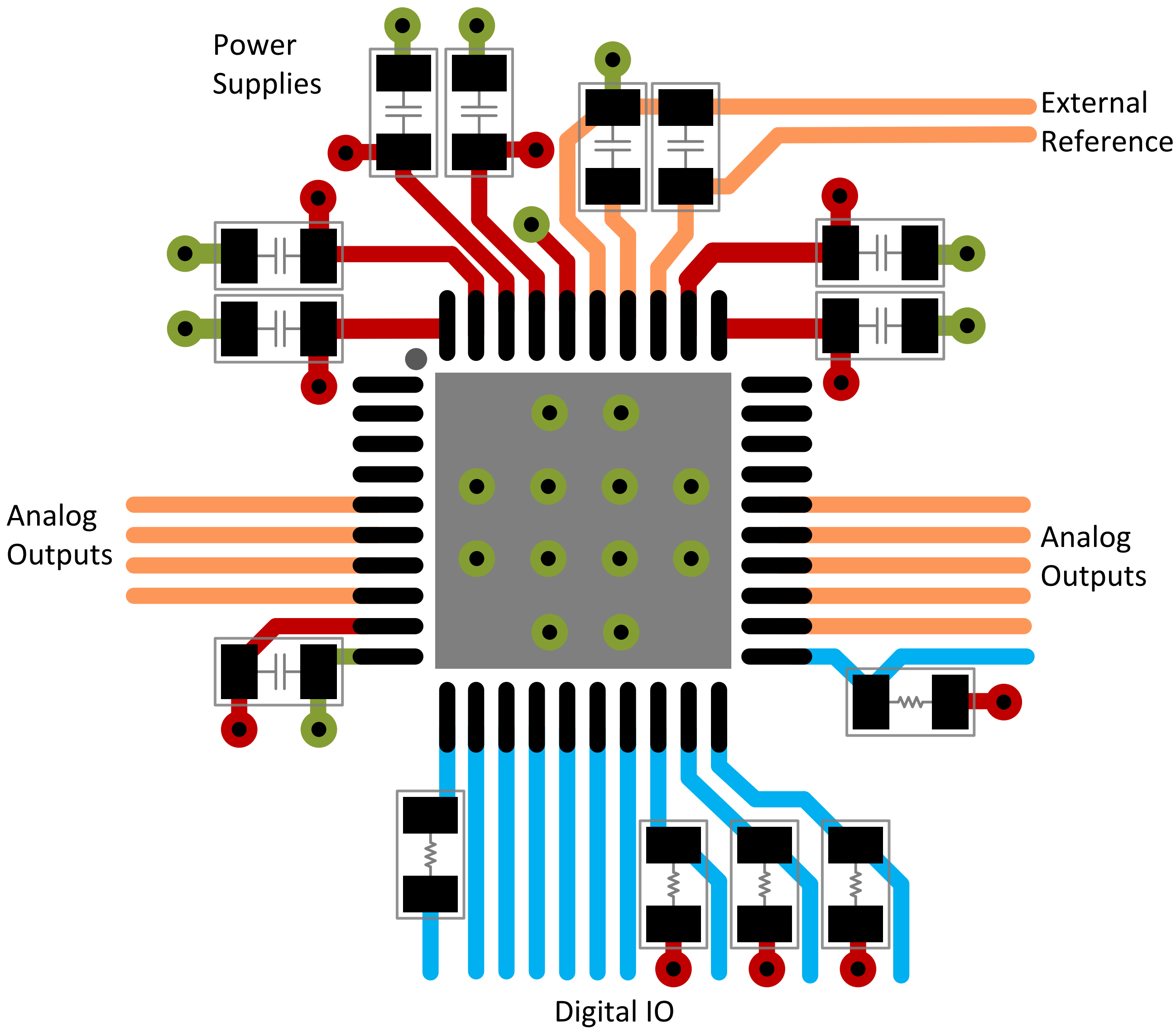


Figure 70. Example Layout

13 Device and Documentation Support

13.1 Documentation Support

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 25. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC81408	Click here	Click here	Click here	Click here	Click here
DAC71408	Click here	Click here	Click here	Click here	Click here
DAC61408	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

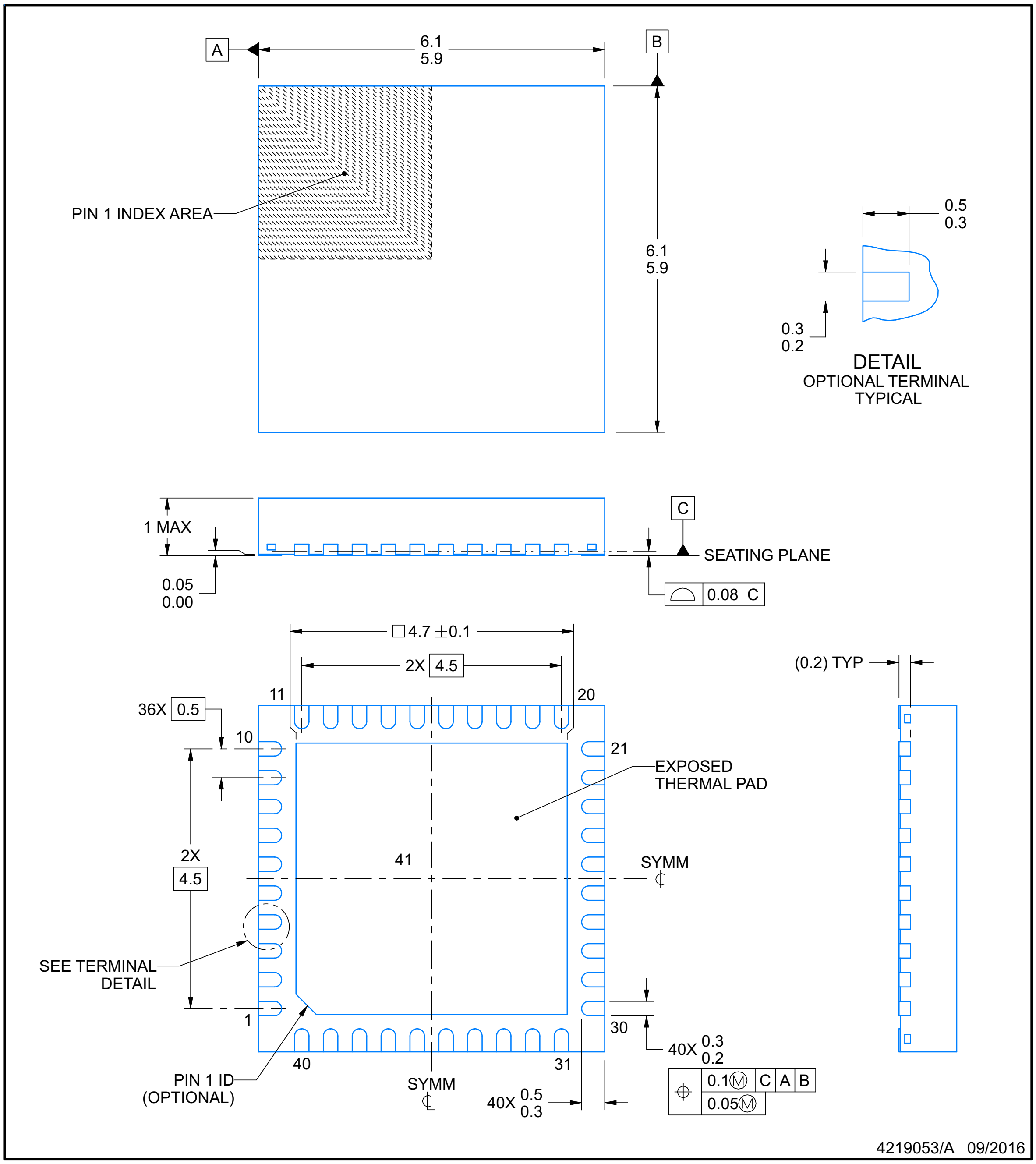
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

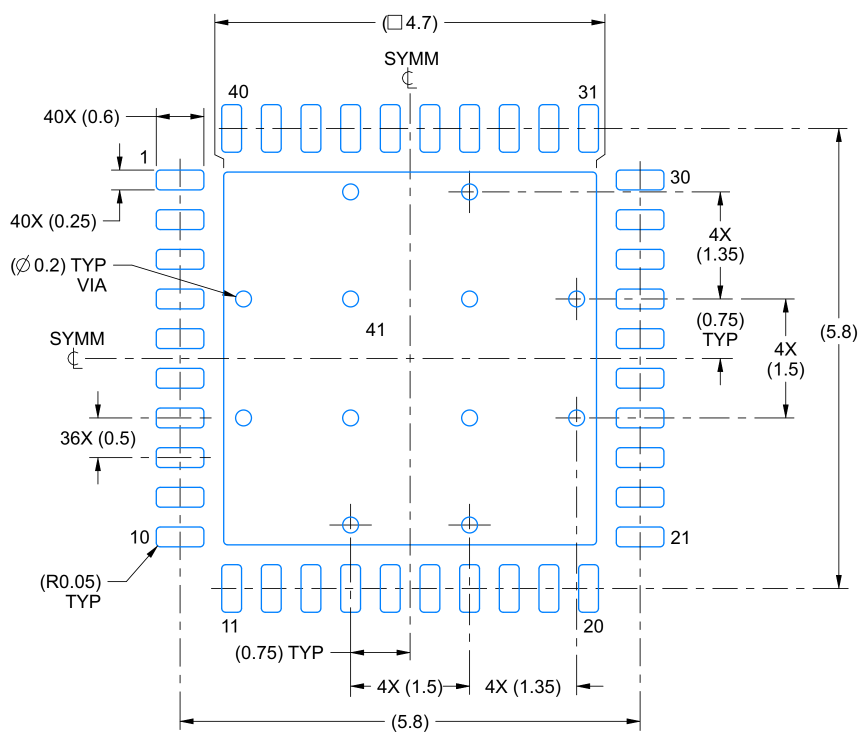
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

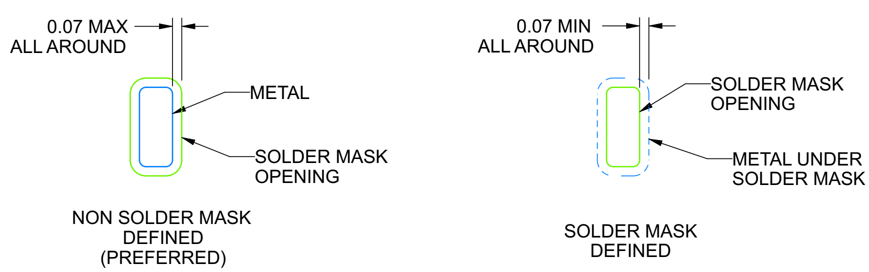
RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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NOTES: (continued)

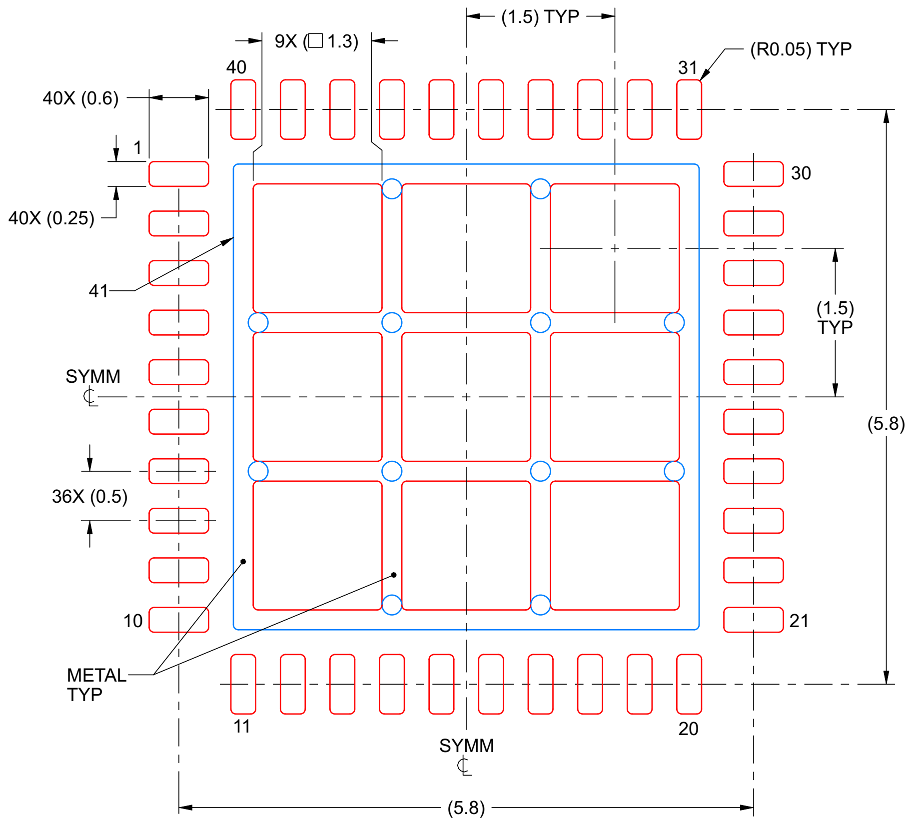
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0040C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC61408RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61408	Samples
DAC61408RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61408	Samples
DAC71408RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71408	Samples
DAC71408RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71408	Samples
DAC81408RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81408	Samples
DAC81408RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81408	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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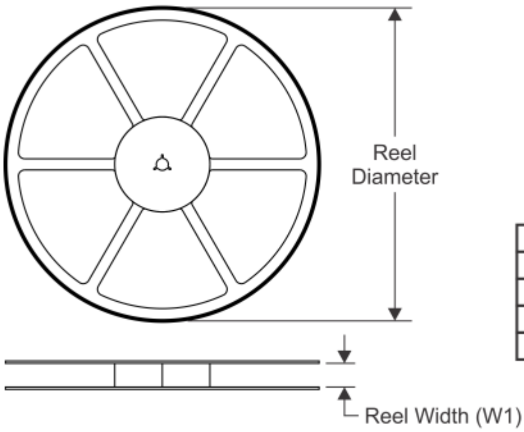
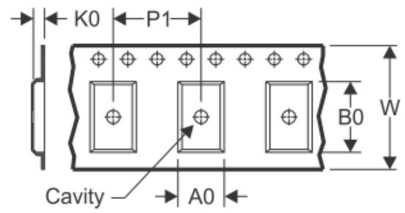
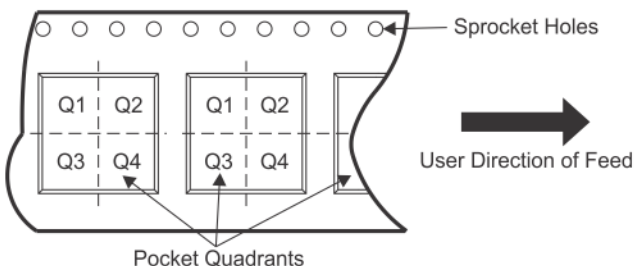
TAPE AND REEL INFORMATION





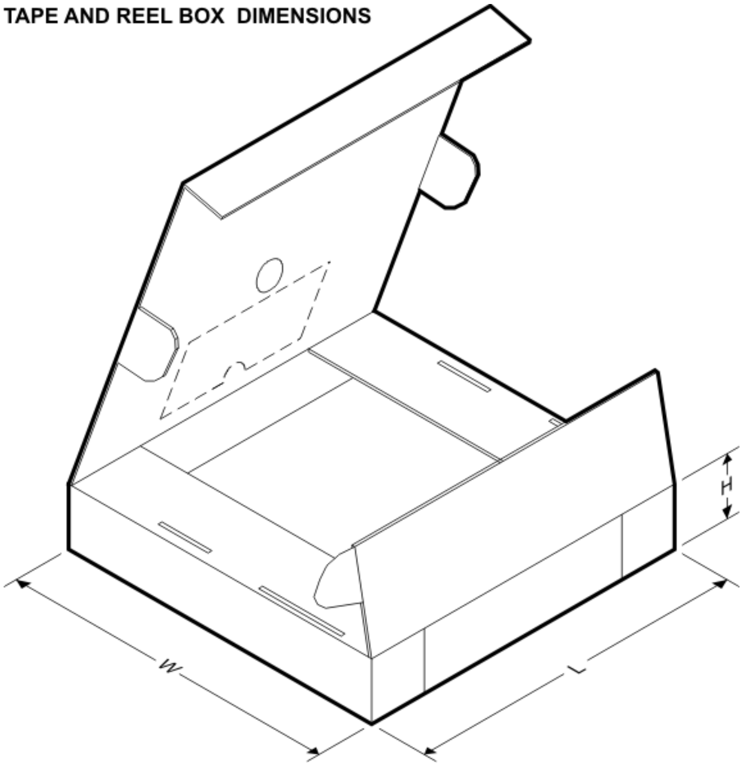
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC61408RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC61408RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC71408RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC71408RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC81408RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC81408RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC61408RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC61408RHAT	VQFN	RHA	40	250	213.0	191.0	35.0
DAC71408RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC71408RHAT	VQFN	RHA	40	250	213.0	191.0	35.0
DAC81408RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC81408RHAT	VQFN	RHA	40	250	213.0	191.0	35.0