

## 11.3-Gbps Limiting Transimpedance Amplifier With RSSI

Check for Samples: [ONET8551T](#)

### FEATURES

- 9-GHz Bandwidth
- 10-k $\Omega$  Differential Small Signal Transimpedance
- –20-dBm Sensitivity
- 0.9- $\mu$ A<sub>RMS</sub> Input Referred Noise
- 2.5-mA<sub>p-p</sub> Input Overload Current
- Received Signal Strength Indication (RSSI)
- 92-mW Typical Power Dissipation
- CML Data Outputs With On-Chip 50- $\Omega$  Back-Termination
- On Chip Supply Filter Capacitor
- Single +3.3-V Supply
- Die Size: 870  $\mu$ m x 1036  $\mu$ m

### APPLICATIONS

- 10-G Ethernet
- 8-G and 10-G Fibre Channel
- 10-G EPON
- SONET OC-192
- 6-G and 10-G CPRI and OBSAI
- PIN and APD Preamplifier-Receivers

### DESCRIPTION

The ONET8551T device is a high-speed, high-gain, limiting transimpedance amplifier used in optical receivers with data rates up to 11.3 Gbps. It features low-input referred noise, 9-GHz bandwidth, 10-k $\Omega$  small signal transimpedance, and a received signal strength indicator (RSSI).

The ONET8551T device is available in die form, includes an on-chip VCC bypass capacitor, and is optimized for packaging in a TO can.

The ONET8551T device requires a single +3.3-V supply. The power-efficient design typically dissipates less than 95 mW. The device is characterized for operation from –40°C to 100°C case (IC back-side) temperature.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

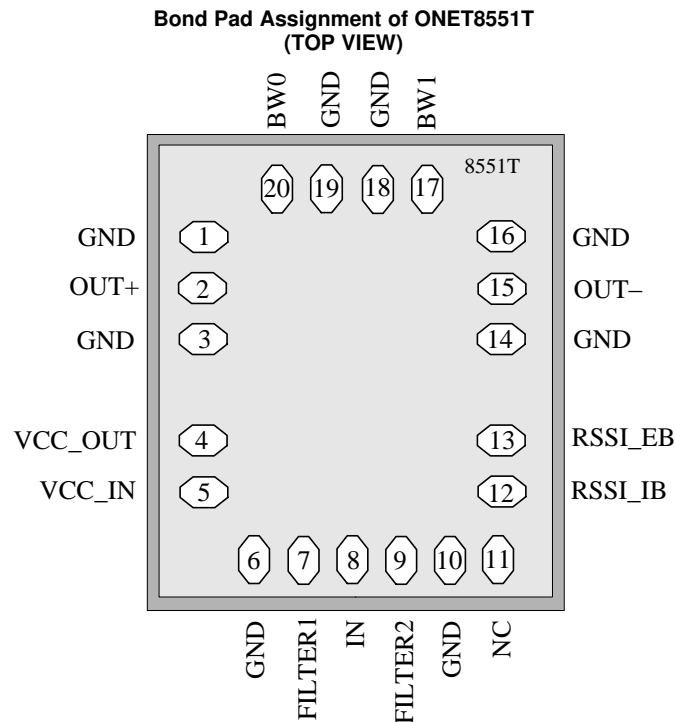
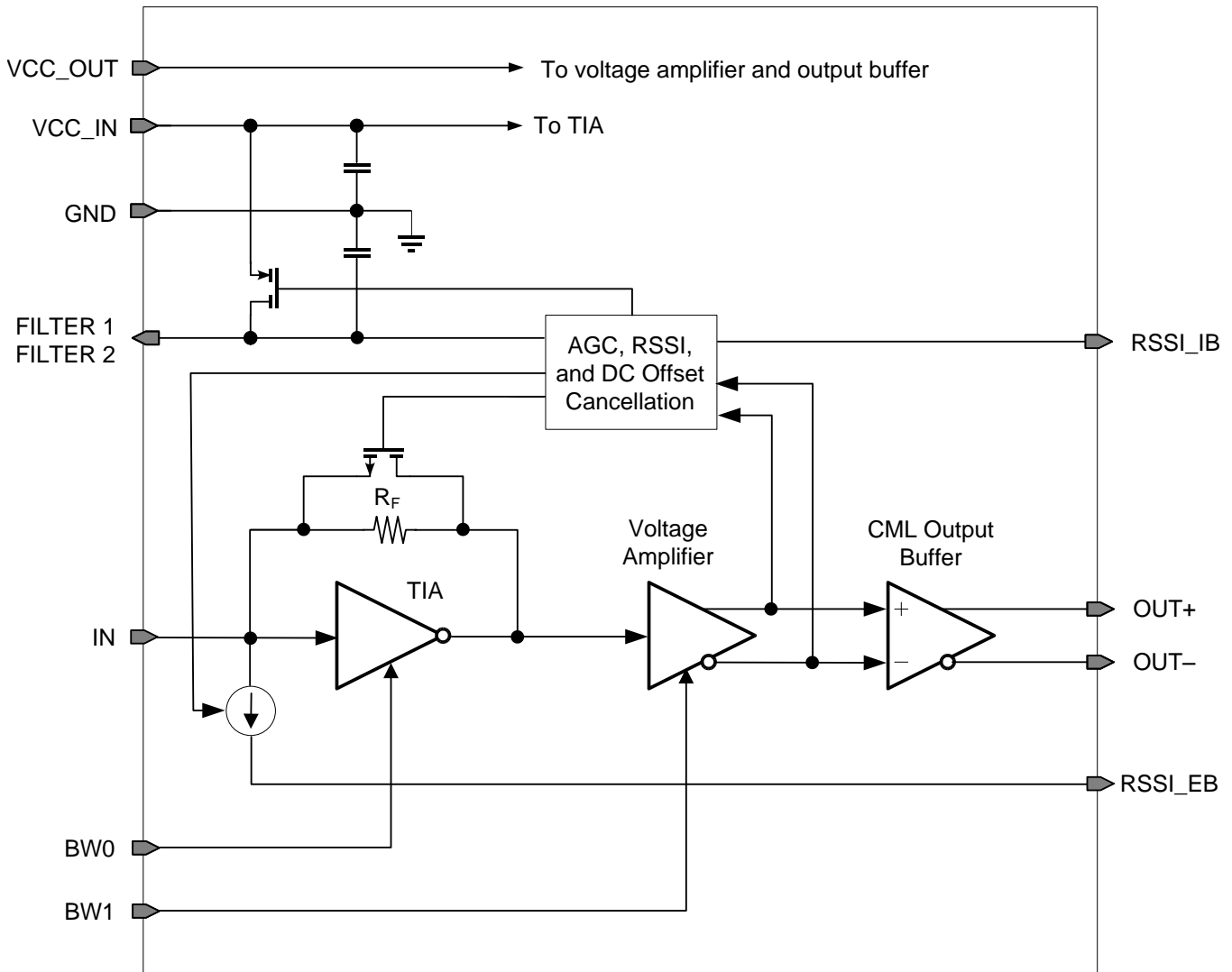


Figure 1. The ONET8551T is available in die form. Bond pad locations are shown in this top view.

Table 1. BOND PAD DESCRIPTION

| Pad                         | Symbol  | Type          | Description  |
|-----------------------------|---------|---------------|--|
| 1, 3, 6, 10, 14, 16, 18, 19 | GND     | Supply        | Circuit ground. All GND pads are connected on die. Bonding all pads is optional. However, for optimum performance, a good ground connection is mandatory.  |
| 2                           | OUT+    | Analog output | Non-inverted CML data output; on-chip 50-Ω back-terminated to V <sub>CC</sub>  |
| 4                           | VCC_OUT | Supply        | 2.8-V to 3.63-V supply voltage for AGC amplifier   |
| 5                           | VCC_IN  | Supply        | 2.8-V to 3.63-V supply voltage for input TIA stage   |
| 7, 9                        | FILTER  | Analog        | Bias voltage for photodiode cathode  |
| 8                           | IN      | Analog input  | Data input to TIA (photodiode anode)   |
| 11                          | NC      | No connect    | Do not connect   |
| 12                          | RSSI_IB | Analog output | Analog output current is proportional to the input data amplitude. It indicates the strength of the received signal (RSSI), if the photodiode is biased from the TIA. Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V <sub>CC</sub> – 0.65 V. Leave this pad open if the RSSI feature is not used.              |
| 13                          | RSSI_EB | Analog output | Optional use when operated with external PD bias (e.g. APD). Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI). Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V <sub>CC</sub> – 0.65 V. Leave this pad open if the RSSI feature is not used. |
| 15                          | OUT–    | Analog output | Inverted CML data output; on-chip 50-Ω back-terminated to V <sub>CC</sub> .  |
| 17                          | BW1     | Digital input | Bandwidth adjustment. Ground the pad to increase the bandwidth. Internally pulled-up to V <sub>CC</sub> .  |
| 20                          | BW0     | Digital input | Bandwidth adjustment. Ground the pad to increase the bandwidth. Internally pulled-up to V <sub>CC</sub> .  |
| Back-side of die            | GND     | Supply        | Conductive epoxy must be used to attach the die to ground.   |



**Figure 2. Simplified Block Diagram of the ONET8551T Device**

Figure 2 shows a simplified block diagram of the ONET8551T device.

The ONET8551T device consists of the signal path, supply filters, a control block for DC input bias, automatic gain control (AGC), and received signal strength indication (RSSI). The RSSI provides the bias for the TIA stage and the control for the AGC.

The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and a CML output buffer. The on-chip filter circuit provides a filtered VCC for the PIN photodiode and for the transimpedance amplifier.

The DC input bias circuit and automatic gain control use internal low pass filters to cancel the DC current on the input and to adjust the transimpedance amplifier gain. Furthermore, circuitry is provided to monitor the received signal strength.

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  |  | VALUE |     | UNIT     |
|--|--|-------|-----|----------|
|  |  | MIN   | MAX |          |
| $V_{CC\_IN}$ , $V_{CC\_OUT}$   | Supply voltage <sup>(2)</sup>  | -0.3  | 4.0 | V        |
| $V_{BW0}$ , $V_{BW1}$ ,<br>$V_{FILTER1}$ , $V_{FILTER2}$ ,<br>$V_{OUT+}$ , $V_{OUT-}$ ,<br>$V_{RSSI\_IB}$ , $V_{RSSI\_EB}$ | Voltage at BW0, BW1, FILTER1, FILTER2, OUT+, OUT-, RSSI_IB, and RSSI_EB <sup>(2)</sup> | -0.3  | 4.0 |          |
| $I_{IN}$   | Current into IN  | -0.7  | 4.0 | mA       |
| $I_{FILTER}$   | Current into FILTER1 and FILTER2   | -8    | 8   |          |
| $I_{OUT+}$ , $I_{OUT-}$  | Continuous current at outputs  | -8    | 8   |          |
| ESD  | ESD rating at all pins except input IN   | 2     |     | kV (HBM) |
|  | ESD rating at input IN   | 0.5   |     |          |
| $T_J$  | Maximum junction temperature   |       | 125 | °C       |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

|                         |   | MIN  | NOM | MAX                | UNIT |
|-------------------------|---|------|-----|--------------------|------|
| $V_{CC}$                | Supply voltage  | 2.80 | 3.3 | 3.63               | V    |
| $T_A$                   | Operating back-side die temperature                     | -40  |     | 100 <sup>(1)</sup> | °C   |
| $L_{FILTER}$ , $L_{IN}$ | Wire-bond inductance at pins FILTER <sub>i</sub> and IN |      | 0.3 | 0.5                | nH   |
| $C_{PD}$                | Photodiode capacitance                                  |      | 0.2 |                    | pF   |

- (1) 105°C max junction temperature.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with BW0 = GND and BW1 = Open (unless otherwise noted). Typical values are at  $V_{CC} = +3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

| PARAMETER      |   | TEST CONDITIONS                                  | MIN  | TYP  | MAX               | UNIT          |
|----------------|---|--|------|------|-------------------|---------------|
| $V_{CC}$       | Supply voltage                                      |  | 2.80 | 3.3  | 3.63              | V             |
| $I_{VCC}$      | Supply current                                      | Input current $I_{IN} < 1000\ \mu\text{A}_{P-P}$ |      | 28   | 40 <sup>(1)</sup> | mA            |
| $I_{VCC}$      | Supply current                                      | Input current $I_{IN} < 2500\ \mu\text{A}_{P-P}$ |      |      | 45 <sup>(1)</sup> | mA            |
| $V_{IN}$       | Input bias voltage                                  |  | 0.75 | 0.85 | 0.98              | V             |
| $R_{OUT}$      | Output resistance                                   | Single-ended to $V_{CC}$                         | 40   | 50   | 60                | $\Omega$      |
| $V_{FILTER}$   | Photodiode bias voltage <sup>(2)</sup>              |  | 2.55 | 3.2  |                   | V             |
| $A_{RSSI\_IB}$ | RSSI gain internal bias                             | Resistive load to GND <sup>(3)</sup>             | 0.49 | 0.51 | 0.54              | A/A           |
|                | RSSI internal bias output offset current (no light) |  | 0    | 0.9  | 2.5               | $\mu\text{A}$ |
| $A_{RSSI\_EB}$ | RSSI gain external bias                             | Resistive load to GND <sup>(3)</sup>             | 0.46 |      | 0.63              | A/A           |
|                | RSSI external bias output offset current (no light) |  |      | 25   |                   | $\mu\text{A}$ |

(1) Including RSSI current

(2) Regulated voltage typically 100 mV lower than  $V_{CC}$ .

(3) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor. However, for proper operation, ensure that the voltage at RSSI does not exceed  $V_{CC} - 0.65\text{ V}$ .

## AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with BW0 = GND and BW1 = Open (unless otherwise noted). Typical values are at  $V_{CC} = +3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

| PARAMETER         |                                     | TEST CONDITIONS   | MIN  | TYP   | MAX | UNIT              |
|-------------------|-------------------------------------|---|------|-------|-----|-------------------|
| $Z_{21}$          | Small signal transimpedance         | Differential output; Input current $i_{IN} = 20\ \mu\text{A}_{P-P}$                       | 7500 | 10000 |     | $\Omega$          |
| $f_{HSS, 3dB}$    | Small signal bandwidth              | $i_{IN} = 20\ \mu\text{A}_{P-P}$ <sup>(1)</sup>   | 7    | 9     |     | GHz               |
| $f_{L, 3dB}$      | Low frequency –3-dB bandwidth       | $16\ \mu\text{A}_{P-P} < i_{IN} < 2000\ \mu\text{A}_{P-P}$                                |      | 30    | 150 | kHz               |
| $i_{N, IN}$       | Input referred RMS noise            | 10-GHz bandwidth <sup>(2)</sup>   |      | 0.9   | 1.4 | $\mu\text{A}$     |
| $S_{US}$          | Unstressed sensitivity electrical   | 10.3125 Gbps, PRBS31 pattern, 1310 nm, extinction ratio > 9 dB, BER $10^{-12}$            |      | –20   |     | dBm               |
| DJ                | Deterministic jitter                | $25\ \mu\text{A}_{P-P} < i_{IN} < 500\ \mu\text{A}_{P-P}$ (10.3125 Gbps, K28.5 pattern)   |      | 6     | 15  | ps <sub>P-P</sub> |
|                   |                                     | $500\ \mu\text{A}_{P-P} < i_{IN} < 2500\ \mu\text{A}_{P-P}$ (10.3125 Gbps, K28.5 pattern) |      | 10    | 24  |                   |
| $V_{OUT, D, MAX}$ | Maximum differential output voltage | Input current $i_{IN} = 500\ \mu\text{A}_{P-P}$   | 180  | 300   | 420 | mV <sub>P-P</sub> |
| PSNR              | Power supply noise rejection        | $F < 10\text{ MHz}$ <sup>(3)</sup> , supply filtering according to SFF8431                |      | –15   |     | dB                |

(1) The small signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.2 pF and the bond-wire inductance is 0.3 nH. The small signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.

(2) Input referred RMS noise is (RMS output noise) divided by (gain at 100 MHz).

(3) PSNR is the differential output amplitude divided by the voltage ripple on supply. No input current at IN.

## DETAILED DESCRIPTION

### SIGNAL PATH

The first stage of the signal path is a transimpedance amplifier, which converts the photodiode current into a voltage. If the input signal current exceeds a certain value, the transimpedance gain is reduced by a nonlinear AGC circuit to limit the signal amplitude.

The second stage is a limiting voltage amplifier that provides additional limiting gain and converts the single-ended input voltage into a differential data signal. The output stage provides CML outputs with an on-chip 50- $\Omega$  back-termination to  $V_{CC}$ .

### FILTER CIRCUITRY

The FILTER pins provide a regulated and filtered VCC for a PIN photodiode bias. The supply voltages for the transimpedance amplifier are filtered by on-chip capacitors, thus an external supply filter capacitor is not necessary. The input stage has a separate VCC supply ( $V_{CC\_IN}$ ), which is not connected on chip to the supply of the limiting and CML stages ( $V_{CC\_OUT}$ ).

### AGC AND RSSI

The voltage drop across the regulated FILTER FET is monitored by the bias and RSSI control circuit block in the case where a PIN diode is biased using the FILTER pins.

If the DC input current exceeds a certain level, then it is partially cancelled by a controlled current source. This process keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance.

The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure limiting behavior of the complete amplifier.

Finally this circuit block senses the current through the FILTER FET and generates a mirrored current that is proportional to the input signal strength. The mirrored current is available at the RSSI\_IB output and can be sunk to GND using an external resistor. For proper operation, ensure that the voltage at the RSSI\_IB pad does not exceed  $V_{CC} - 0.65$  V.

If an APD or PIN photodiode is used with an external bias, then the RSSI\_EB pin can be used. However, for greater accuracy under external photodiode biasing conditions, TI recommends deriving the RSSI from the external bias circuitry.

### APPLICATION INFORMATION

Figure 3 shows the ONET8551T device used in a typical fiber optic receiver with the internal photodiode bias. The ONET8551T device converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER output provides a low-pass filtered DC bias voltage for the PIN. The photodiode must be connected to the FILTER pad for the bias to function correctly, because the bias circuit senses and uses the voltage drop across the FET.

The RSSI output is used to mirror the photodiode output current and can be connected via a resistor to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor. However, for proper operation of the ONET8551T, ensure that the voltage at RSSI never exceeds  $V_{CC} - 0.65$  V. Leave the RSSI output open, if the RSSI output is not used while operating with internal PD bias.

The OUT+ and OUT- pins are internally terminated by 50-Ω pullup resistors to VCC. The outputs must be AC coupled, for example by using 0.1-μF capacitors, to the succeeding device.

For PIN diode applications, TI recommends grounding the BW0 pin. However, for higher bandwidth, the BW1 pin, or both the BW0 and BW1 pins, can be grounded. To reduce the bandwidth, the BW0 and BW1 pins can be left open.

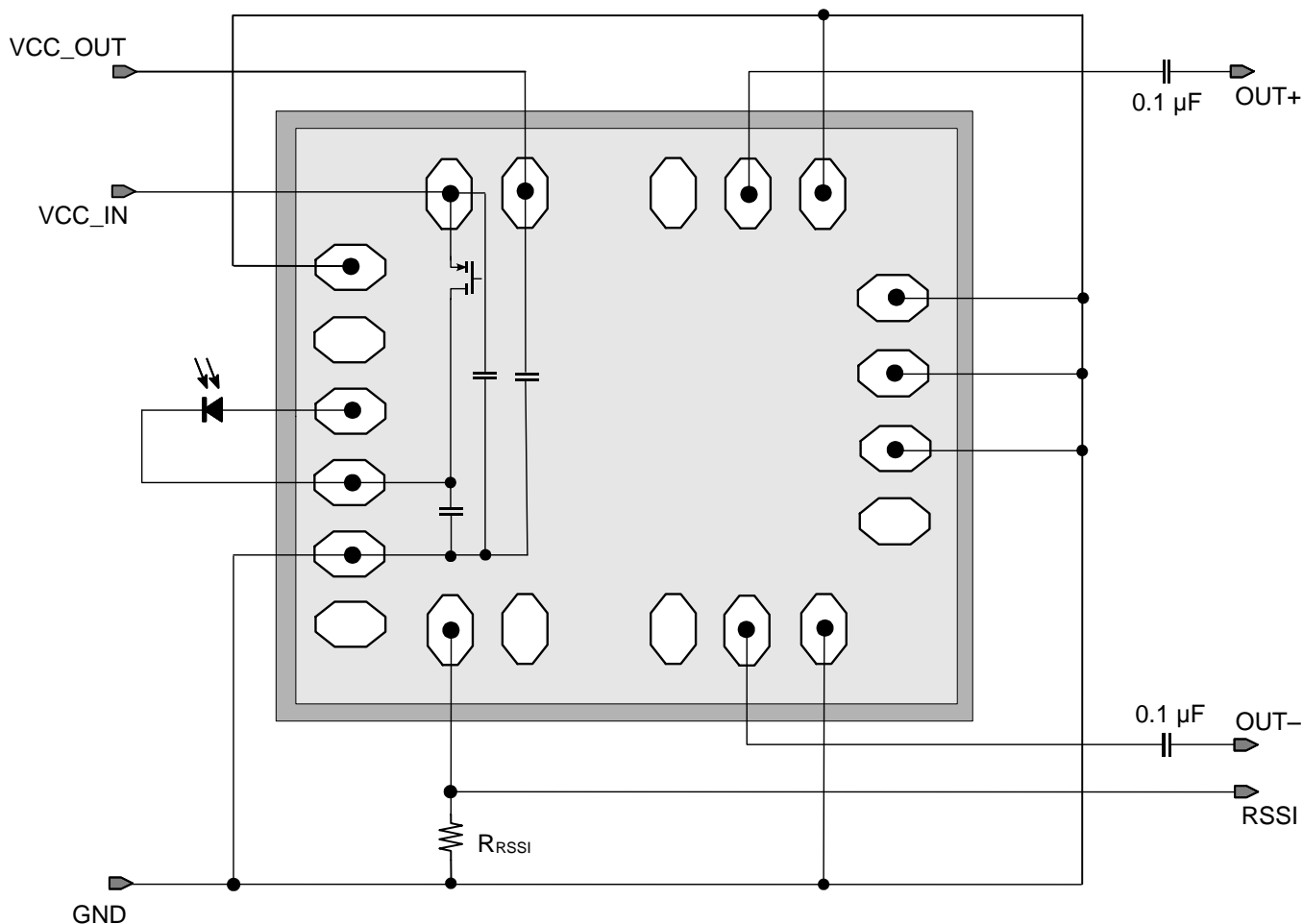
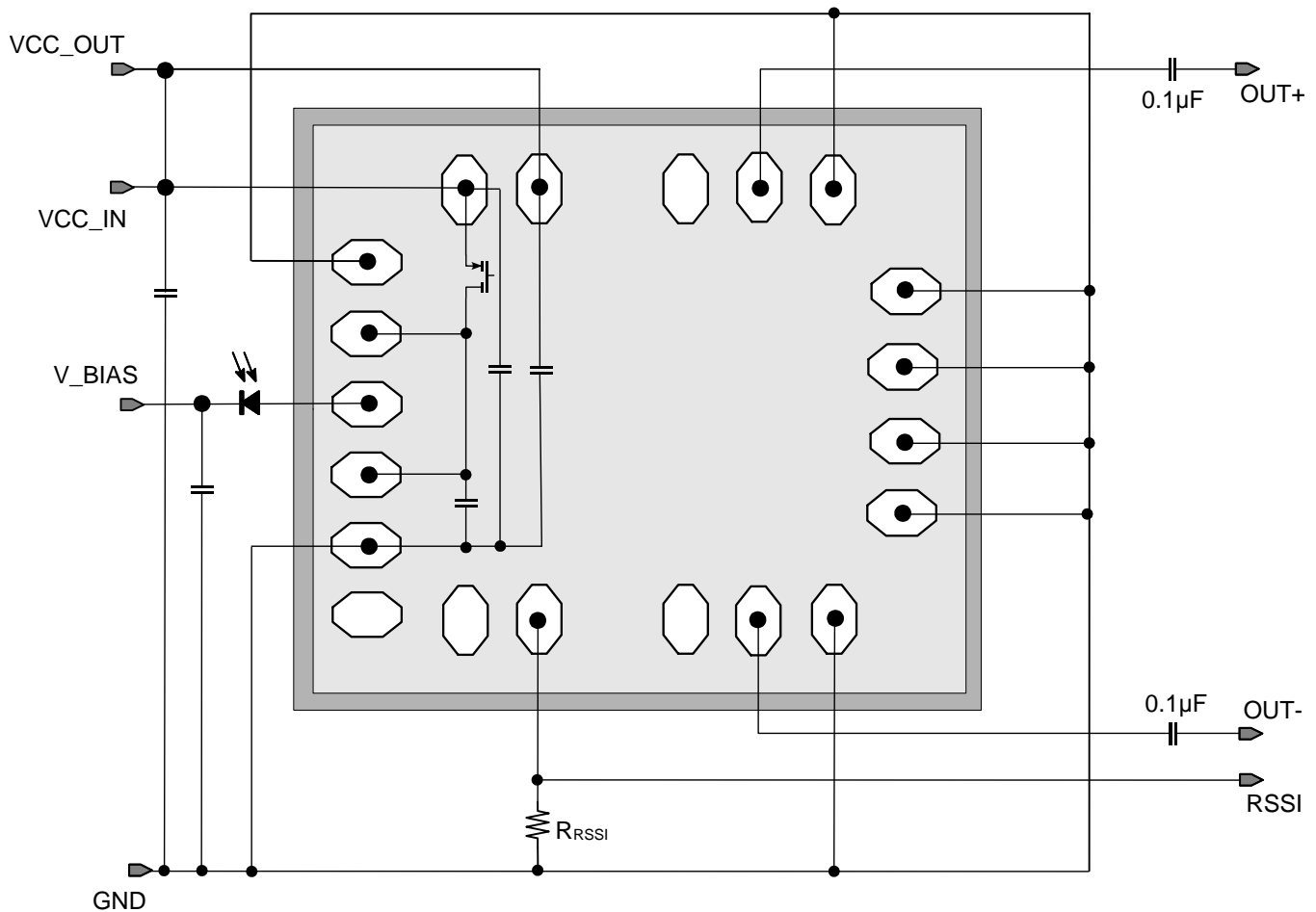


Figure 3. Basic Application Circuit for PIN Receivers

Figure 4 shows the ONET8551T device used in a typical fiber-optic receiver using an external photodiode bias for an avalanche photodiode. To increase the bandwidth using APDs, ground the BW0 and BW1 pins. This configuration can also be used for a PIN diode. However, it may be beneficial to reduce the bandwidth, and therefore the noise, by grounding only the BW0 pin. The external bias RSSI signal is based on the DC offset value and is not as accurate as the internal bias RSSI, which is based on the photodiode current.



**Figure 4. Basic Application Circuit for APD Receivers**

## DEVICE INFORMATION

### ASSEMBLY RECOMMENDATIONS

Careful attention to assembly parasitics and external components is necessary to achieve optimal performance. Recommendations that optimize performance include:

- Minimize the total capacitance on the IN pad by using a low capacitance photodiode and paying attention to stray capacitances. Place the photodiode close to the ONET8551T die in order to minimize the bond wire length, and thus the parasitic inductance.
- Use identical termination and symmetrical transmission lines at the AC coupled differential output pins, OUT+ and OUT-.
- Use short bond wire connections for the supply terminals VCC\_IN, VCC\_OUT, and GND. Supply voltage filtering is provided on chip, but filtering may be improved by using an additional external capacitor.
- The die has back-side metal. Conductive epoxy must be used to attach the die to ground.



## CHIP DIMENSIONS AND PAD LOCATIONS

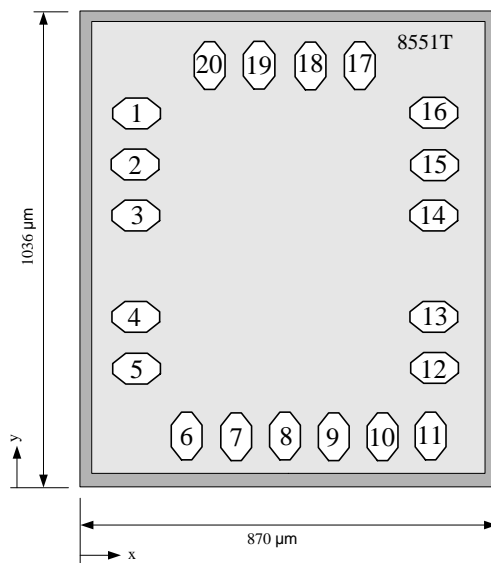
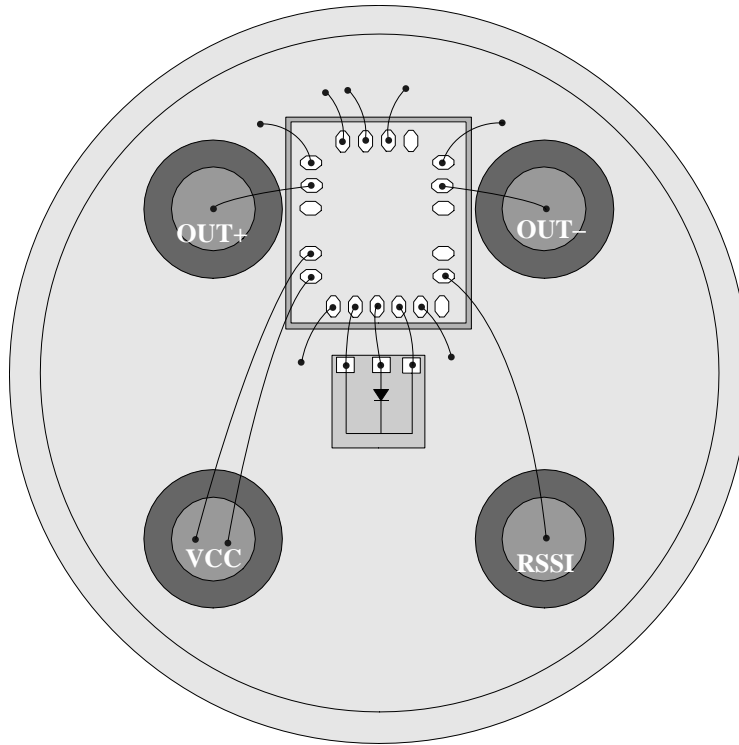


Figure 5. Die Thickness:  $203 \pm 13 \mu\text{m}$ , Pad Dimensions:  $105 \mu\text{m} \times 65 \mu\text{m}$ , and Die Size:  $870 \pm 40 \mu\text{m} \times 1036 \pm 40 \mu\text{m}$

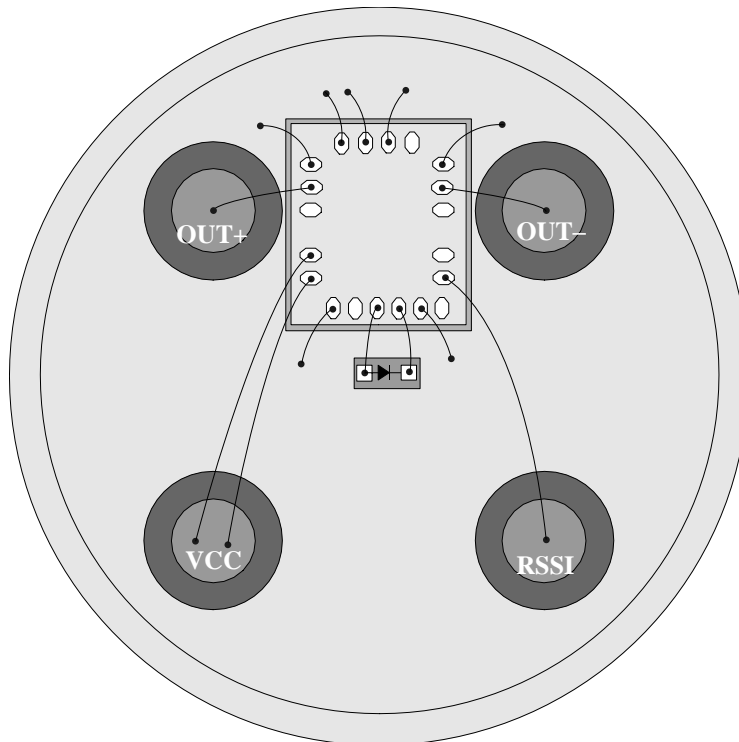
| PAD | COORDINATES (Referenced to Pad 1) |                     | SYMBOL  | TYPE          | DESCRIPTION  |
|-----|-----------------------------------|---------------------|---------|---------------|--|
|     | x ( $\mu\text{m}$ )               | y ( $\mu\text{m}$ ) |         |               |  |
| 1   | 0                                 | 0                   | GND     | Supply        | Circuit ground                                     |
| 2   | 0                                 | -115                | OUT+    | Analog output | Non-inverted data output                           |
| 3   | 0                                 | -230                | GND     | Supply        | Circuit ground                                     |
| 4   | 0                                 | -460                | VCC_OUT | Supply        | 3.3-V supply voltage                               |
| 5   | 0                                 | -575                | VCC_IN  | Supply        | 3.3-V supply voltage                               |
| 6   | 116                               | -728                | GND     | Supply        | Circuit ground                                     |
| 7   | 226                               | -728                | FILTER1 | Analog output | Bias voltage for photodiode                        |
| 8   | 336                               | -728                | IN      | Analog input  | Data input to TIA                                  |
| 9   | 446                               | -728                | FILTER2 | Analog output | Bias voltage for photodiode                        |
| 10  | 556                               | -728                | GND     | Supply        | Circuit ground                                     |
| 11  | 666                               | -728                | NC      | No connect    | Do not connect                                     |
| 12  | 671                               | -575                | RSSI_IB | Analog output | RSSI output signal for internally biased receivers |
| 13  | 671                               | -460                | RSSI_EB | Analog output | RSSI output signal for externally biased receivers |
| 14  | 671                               | -230                | GND     | Supply        | Circuit ground                                     |
| 15  | 671                               | -115                | OUT-    | Analog output | Inverted data output                               |
| 16  | 671                               | 0                   | GND     | Supply        | Circuit ground                                     |
| 17  | 508                               | 109                 | BW1     | Digital input | Bandwidth adjustment                               |
| 18  | 393                               | 109                 | GND     | Supply        | Circuit ground                                     |
| 19  | 278                               | 109                 | GND     | Supply        | Circuit ground                                     |
| 20  | 163                               | 109                 | BW0     | Digital input | Bandwidth adjustment                               |

**TO46 LAYOUT EXAMPLE**

Figure 6 shows an example of a layout using a ground-signal-ground (GSG) type PIN photodiode in a 5-pin TO46 can. Figure 7 shows an example of a PIN photodiode with two contacts on the top-side.



**Figure 6. TO46 5-Pin Layout Using the ONET8551T With a GSG PIN Diode**



**Figure 7. TO46 5-Pin Layout Using the ONET8551T With a Two-Contact PIN Diode**

Figure 8 shows an example of a layout using an external bias voltage for the photodiode in a 5-pin TO46 can. Figure 9 shows an example with a back-side cathode contact photodiode using the internal bias voltage.

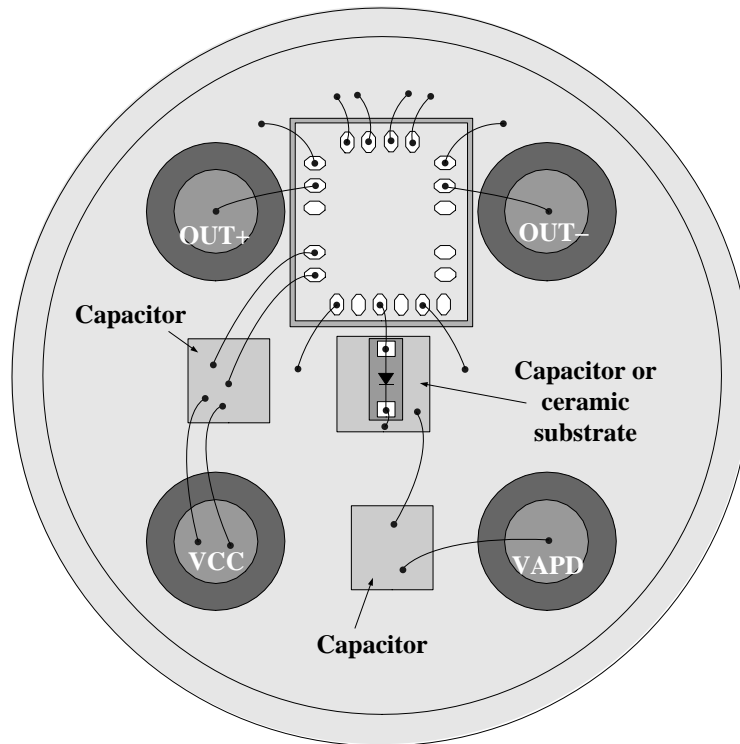


Figure 8. TO46 5-Pin Layout Using the ONET8551T With an Avalanche Photodiode

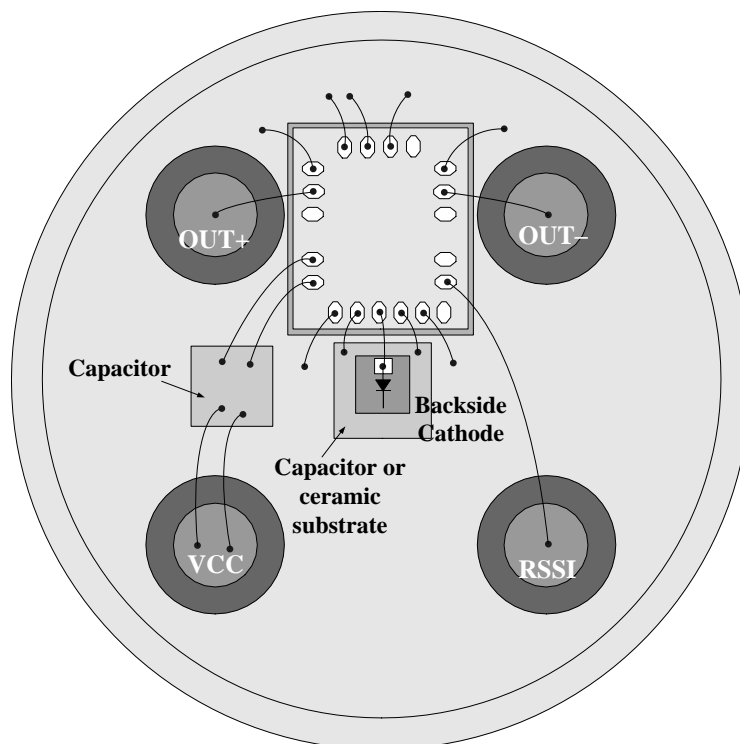
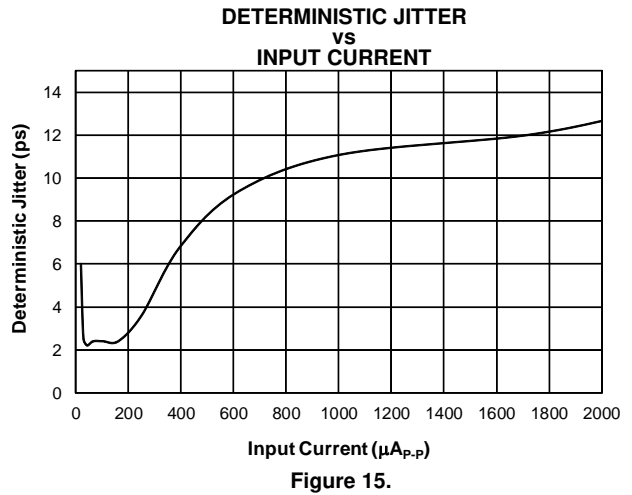
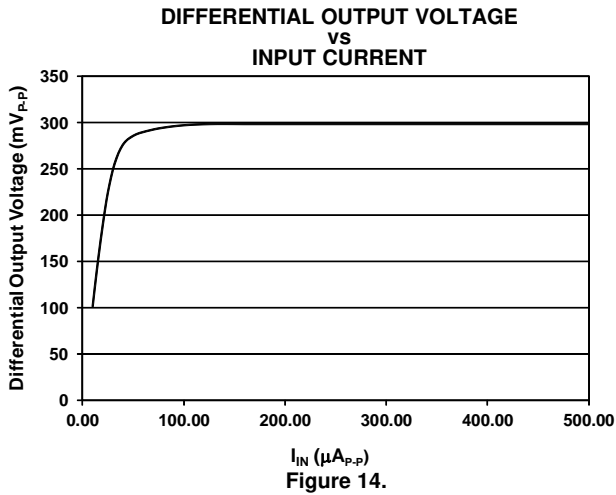
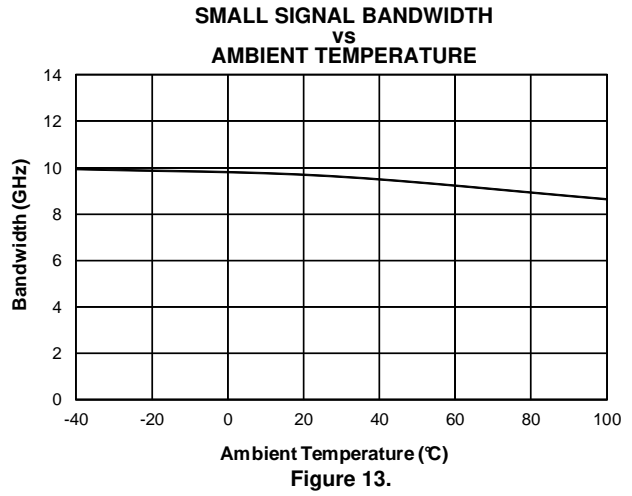
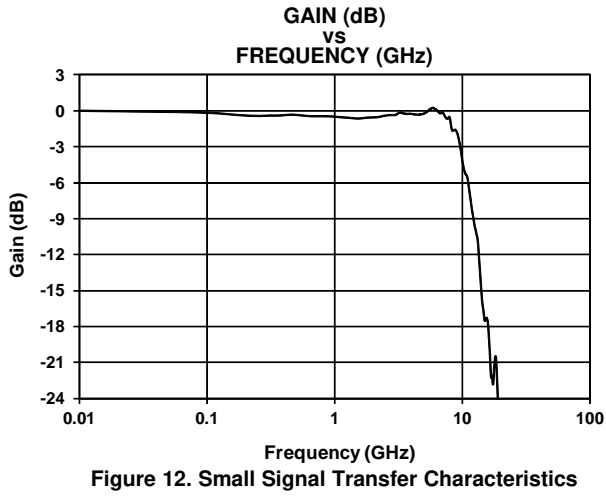
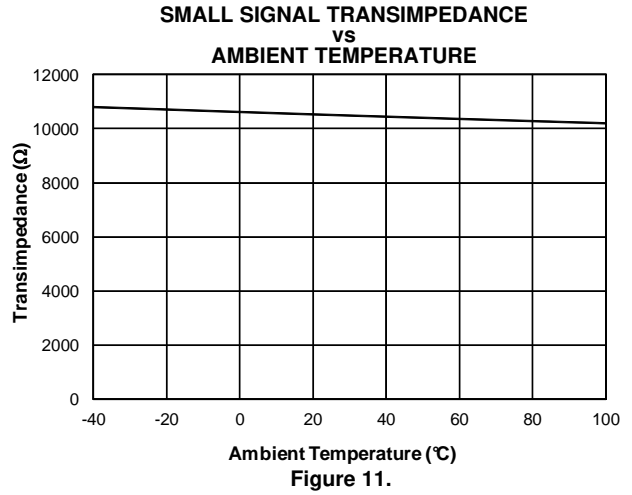
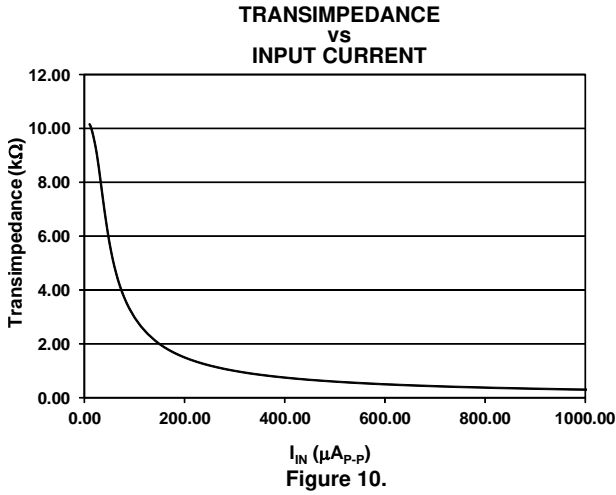


Figure 9. TO46 5-Pin Layout Using the Internal Bias Voltage for a Back-Side Cathode Contact Photodiode

**TYPICAL OPERATION CHARACTERISTICS**

Typical operating condition is at  $V_{CC} = +3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$  (unless otherwise noted).



**TYPICAL OPERATION CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = +3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$  (unless otherwise noted).

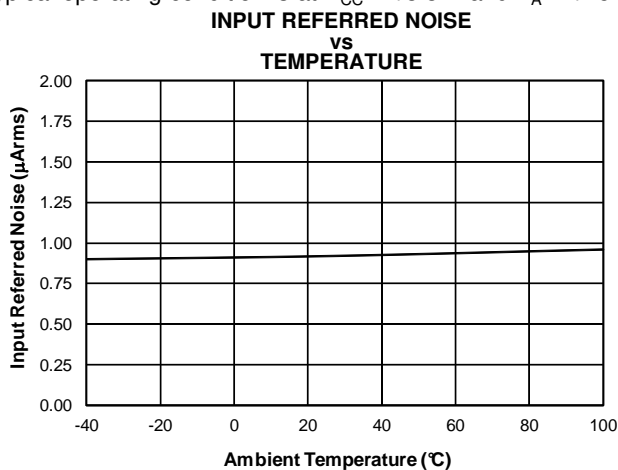


Figure 16.

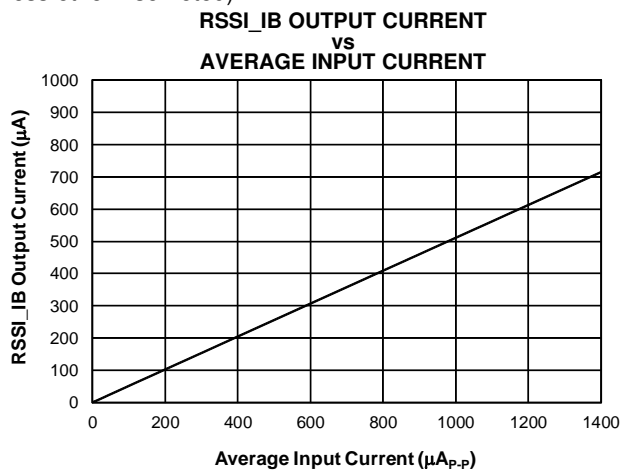
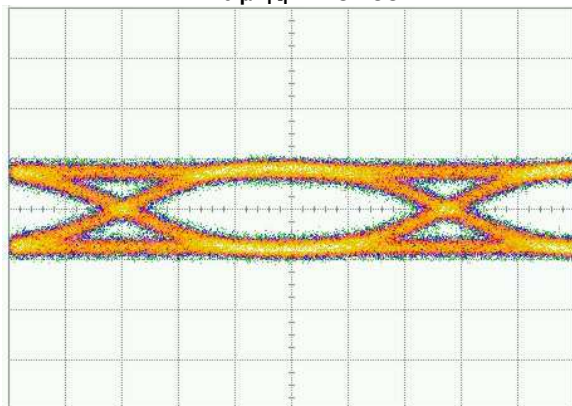


Figure 17.

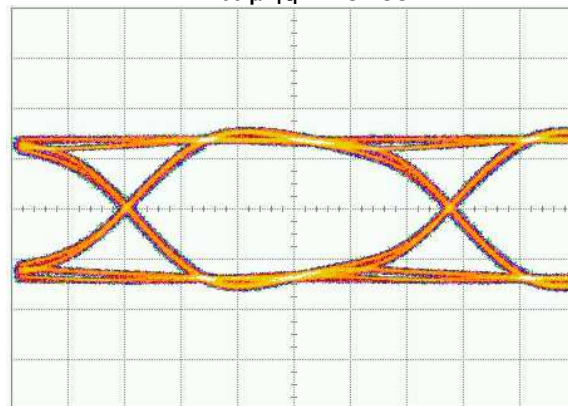
**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 20 µA<sub>p.p</sub> INPUT CURRENT**



100 mV/Div 16.8 ps/Div

Figure 18.

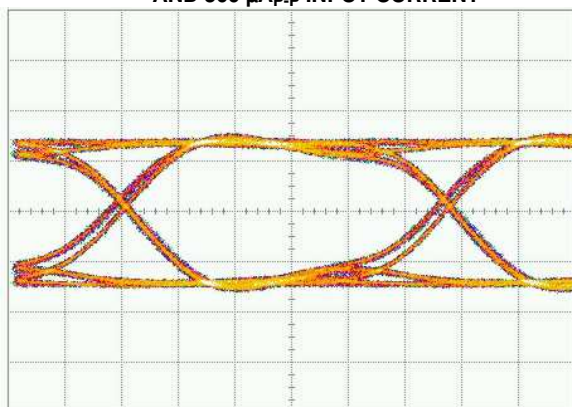
**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 100 µA<sub>p.p</sub> INPUT CURRENT**



100 mV/Div 16.8 ps/Div

Figure 19.

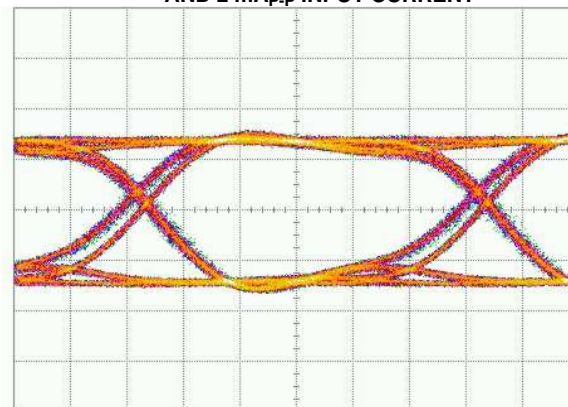
**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 500 µA<sub>p.p</sub> INPUT CURRENT**



100 mV/Div 16.8 ps/Div

Figure 20.

**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 2 mA<sub>p.p</sub> INPUT CURRENT**



100 mV/Div 16.8 ps/Div

Figure 21.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ONET8551TY       | ACTIVE        | DIESALE      | Y               | 0    | 1800        | TBD             | Call TI                 | Call TI              | -40 to 100   |                         | <a href="#">Samples</a> |
| ONET8551TYS4     | ACTIVE        | WAFERSALE    | YS              | 0    | 1           | TBD             | Call TI                 | Call TI              | -40 to 100   |                         | <a href="#">Samples</a> |
| ONET8551TYS9     | ACTIVE        | WAFERSALE    | YS              | 0    | 1           | TBD             | Call TI                 | Call TI              | -40 to 100   |                         | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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