16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet

AD9467

FEATURES

75.5 dBFS SNR to 210 MHz at 250 MSPS
90 dBFS SFDR to 300 MHz at 250 MSPS
SFDR at 170 MHz at 250 MSPS
- **92 dBFS at −1 dBFS**
- **100 dBFS at −2 dBFS**

60 fs rms jitter
Excellent linearity at 250 MSPS
- **DNL = ±0.5 LSB typical**
- **INL = ±3.5 LSB typical**

2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
Integrated input buffer
External reference support option
Clock duty cycle stabilizer
Output clock available
Serial port control
- **Built-in selectable digital test pattern generation**
- **Selectable output data format**

LVDS outputs (ANSI-644 compatible)
1.8 V and 3.3 V supply operation

APPLICATIONS

Multicarrier, multimode cellular receivers
Antenna array positioning
Power amplifier linearization
Broadband wireless
Radar
Infrared imaging
Communications instrumentation

GENERAL DESCRIPTION

The AD9467 is a 16-bit, monolithic, IF sampling analog-to-digital converter (ADC). It is optimized for high performance over wide bandwidths and ease of use. The product operates at a 250 MSPS conversion rate and is designed for wireless receivers, instrumentation, and test equipment that require a high dynamic range.

The ADC requires 1.8 V and 3.3 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are LVDS compatible (ANSI-644 compatible) and include the means to reduce the overall current needed for short trace distances.

FUNCTIONAL BLOCK DIAGRAM

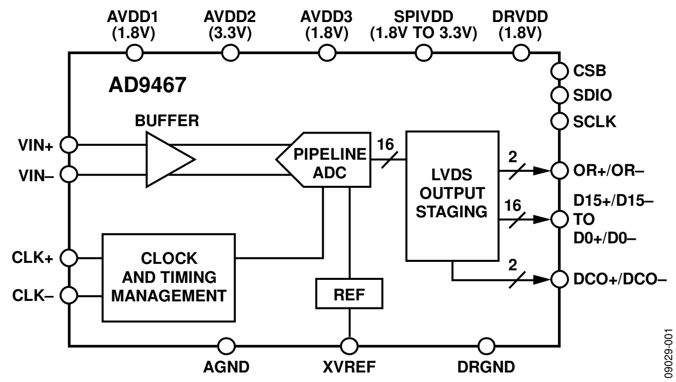

Figure 1.

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. IF optimization capability used to improve SFDR.
2. Outstanding SFDR performance for IF sampling applications such as multicarrier, multimode 3G, and 4G cellular base station receivers.
3. Ease of use: on-chip reference, high input impedance buffer, adjustable analog input range, and an output clock to simplify data capture.
4. Packaged in a Pb-free, 72-lead LFCSP package.
5. Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of input clock pulse widths.
6. Standard serial port interface (SPI) supports various product features and functions, such as data formatting (offset binary, twos complement, or Gray coding).

Rev. D Document Feedback

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REVISION HISTORY

2/13—Rev. C to Rev. D

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3/11—Rev. A to Rev. B

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2/11—Rev. 0 to Rev. A

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10/10—Revision 0: Initial Version

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

		AD9467BCPZ-200			AD9467BCPZ-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		16			16			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−150	0	+150	−150	0	+150	LSB
Gain Error	Full	−3.5	−0.2	+2.5	−3.5	−0.1	+2.5	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.8	±0.4	+0.7	−0.6	±0.5	+1.3	LSB
Integral Nonlinearity (INL)[2]	Full	−9.5	±5	+9.5	−11.8	±3.5	+9.5	LSB
TEMPERATURE DRIFT								
Offset Error	Full		±0.020			±0.023		%FSR/°C
Gain Error	Full		±0.011			±0.036		%FSR/°C
ANALOG INPUTS								
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.3			2.15		V
Differential Input Resistance	25°C		530			530		Ω
Differential Input Capacitance	25°C		3.5			3.5		pF
Full Power Bandwidth	25°C		900			900		MHz
XVREF INPUT								
Input Voltage	Full	1		1.25	1		1.25	V
Input Capacitance	Full		3			3		pF
POWER SUPPLY								
AVDD1	Full	1.75	1.8	1.85	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD1}	Full	485	536	580	514	567	618	mA
I_{AVDD2}	Full	49	55	61	49	55	61	mA
I_{AVDD3}	Full	21	24	27	27	31	35	mA
I_{DRVDD}	Full	35	38	41	36	40	43	mA
Total Power Dissipation (Including Output Drivers)	Full	1.14	1.26	1.37	1.2	1.33	1.45	W
Power-Down Dissipation	Full		4.4	90		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

		AD9467BCPZ-200			AD9467BCPZ-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		2.5	2/2.5		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 5 MHz	25°C		74.6/76.4			74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C	75.1	74.5/76.2			74.5/76.1		dBFS
f_{IN} = 97 MHz	Full	73.8						dBFS
f_{IN} = 140 MHz	25°C		74.3/76.0			74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C		74.2/75.8		74.7	74.3/75.8		dBFS
f_{IN} = 170 MHz	Full				72.3			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.5			74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.5/74.7			73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)								
f_{IN} = 5 MHz	25°C		74.6/76.3			74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C	74.7	74.5/76.2			74.4/76.0		dBFS
f_{IN} = 97 MHz	Full	73.1						dBFS
f_{IN} = 140 MHz	25°C		74.3/75.9			74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C		74.1/75.6		74.4	74.2/75.8		dBFS
f_{IN} = 170 MHz	Full				71.8			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.3			73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.3			73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 5 MHz	25°C		12.1/12.4			12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.4			12.1/12.3		Bits
f_{IN} = 97 MHz	Full							Bits
f_{IN} = 140 MHz	25°C		12.1/12.3			12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3			12.0/12.3		Bits
f_{IN} = 170 MHz	Full							Bits
f_{IN} = 210 MHz	25°C		12.0/12.2			12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.0			11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)[2]								
f_{IN} = 5 MHz	25°C		95/95			98/97		dBFS
f_{IN} = 97 MHz	25°C	86	95/95			95/93		dBFS
f_{IN} = 97 MHz	Full	83						dBFS
f_{IN} = 140 MHz	25°C		94/93			94/95		dBFS
f_{IN} = 170 MHz	25°C		95/90		84	93/92		dBFS
f_{IN} = 170 MHz	Full				84			dBFS
f_{IN} = 210 MHz	25°C		93/88			93/92		dBFS
f_{IN} = 300 MHz	25°C		92/86			93/90		dBFS
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)[2]								
f_{IN} = 5 MHz @ −2 dB Full Scale	Full		100/96			100/100		dBFS
f_{IN} = 97 MHz @ −2 dB Full Scale	Full		100/98			97/97		dBFS
f_{IN} = 140 MHz @ −2 dB Full Scale	Full		98/96			100/95		dBFS
f_{IN} = 170 MHz @ −2 dB Full Scale	Full		96/93			100/100		dBFS
f_{IN} = 210 MHz @ −2 dB Full Scale	Full		94/93			93/93		dBFS
f_{IN} = 300 MHz @ −2 dB Full Scale	Full		90/89			90/90		dBFS

Parameter[1]	Temp	AD9467BCPZ-200 Min	Typ	Max	AD9467BCPZ-250 Min	Typ	Max	Unit
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)[2]								
f_{IN} = 5 MHz	25°C		96/98			98/97		dBFS
f_{IN} = 97 MHz	25°C	86	97/97			97/93		dBFS
f_{IN} = 97 MHz	Full	83						dBFS
f_{IN} = 140 MHz	25°C		97/96			97/95		dBFS
f_{IN} = 170 MHz	25°C		98/98		90	97/93		dBFS
f_{IN} = 170 MHz	Full				87			dBFS
f_{IN} = 210 MHz	25°C		96/97			97/95		dBFS
f_{IN} = 300 MHz	25°C		95/95			97/95		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS @ 2.5 V p-p FS								
f_{IN1} = 70 MHz, f_{IN2} = 72 MHz	25°C		95			97		dBFS
f_{IN1} = 170 MHz, f_{IN2} = 172 MHz	25°C		93			91		dBFS

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] See the SFDR Optimization—Buffer Current Adjustment section for optimum settings.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 3.

Parameter[1]	Temp	AD9467BCPZ-200 Min	AD9467BCPZ-200 Typ	AD9467BCPZ-200 Max	AD9467BCPZ-250 Min	AD9467BCPZ-250 Typ	AD9467BCPZ-250 Max	Unit
CLOCK INPUTS (CLK+, CLK−)								
Logic Compliance			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			250			mV p-p
Input Common-Mode Voltage	Full		0.8			0.8		V
Input Resistance (Differential)	25°C		20			20		kΩ
Input Capacitance	25°C		2.5			2.5		pF
LOGIC INPUTS (SCLK, CSB, SDIO)								
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full			0.3			0.3	V
Input Resistance	25°C		30			30		kΩ
Input Capacitance	25°C		0.5			0.5		pF
LOGIC OUTPUT (SDIO)[3]								
Logic 1 Voltage (I_{OH} = 800 μA)	Full		1.7/3.1			1.7/3.1		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.3			0.3	V
DIGITAL OUTPUTS (D0+ to D15+, D0− to D15−, DCO+, DCO−, OR+, OR−)								
Logic Compliance			LVDS			LVDS		
Differential Output Voltage (V_{OD})	Full	247		545	247		545	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	1.125		1.375	V
Output Coding (Default)			Offset binary			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This depends on if SPIVDD is tied to a 1.8 V or 3.3 V supply.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 4.

Parameter[1]	Temp	AD9467BCPZ-200 Min	Typ	Max	AD9467BCPZ-250 Min	Typ	Max	Unit
CLOCK[2]								
Clock Rate	Full	50		200	50		250	MSPS
Clock Pulse Width High (t_{CH})	Full		2.5			2		ns
Clock Pulse Width Low (t_{CL})	Full		2.5			2		ns
OUTPUT PARAMETERS[2, 3]								
Propagation Delay (t_{PD})	25°C		3			3		ns
Rise Time (t_R) (20% to 80%)	25°C		200			200		ps
Fall Time (t_F) (20% to 80%)	25°C		200			200		ps
DCO Propagation Delay (t_{CPD})	25°C		3			3		ns
DCO to Data Delay (t_{SKEW})	Full	−200		+200	−200		+200	ps
Wake-Up Time (Power-Down)	Full		100			100		ms
Pipeline Latency	Full		16			16		Clock cycles
APERTURE								
Aperture Delay (t_A)	25°C		1.2			1.2		ns
Aperture Uncertainty (Jitter)	25°C		60			60		fs rms
Out-of-Range Recovery Time	25°C		1			1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI interface.
[3] Measurements were made using a part soldered to FR-4 material.

Timing Diagrams

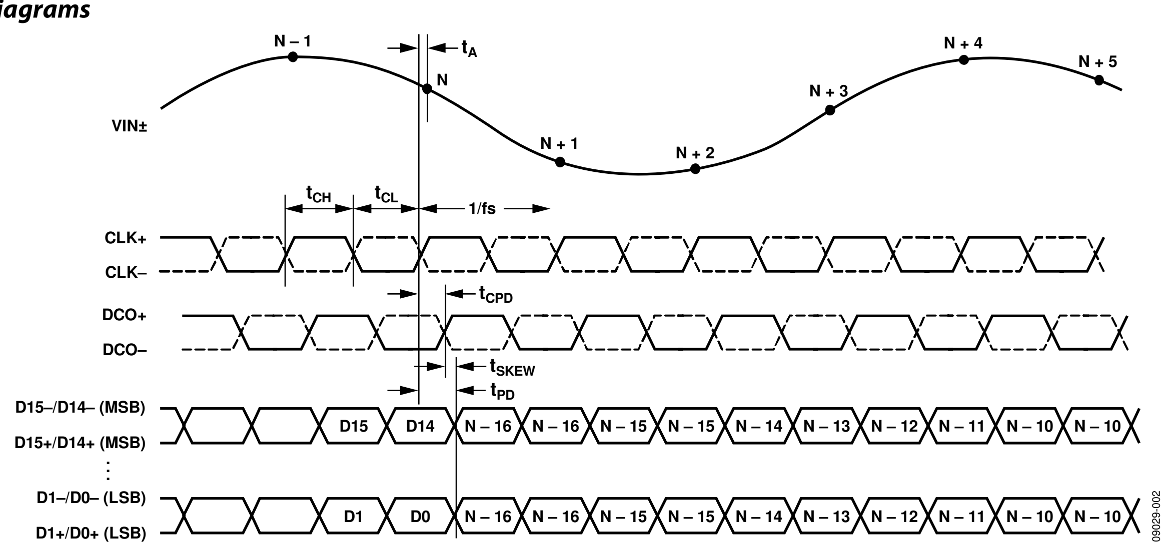

Figure 2. 16-Bit Output Data Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
Electrical		
AVDD1, AVDD3	AGND	−0.3 V to +2.0 V
AVDD2, SPIVDD	AGND	−0.3 V to +3.9 V
DRVDD	DRGND	−0.3 V to +2.0 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD2, SPIVDD	AVDD1, AVDD3	−2.0 V to +3.9 V
AVDD1, AVDD3	DRVDD	−2.0 V to +2.0 V
AVDD2, SPIVDD	DRVDD	−2.0 V to +3.9 V
Digital Outputs (Dx+, Dx−, OR+, OR−, DCO+, DCO−)	DRGND	−0.3 V to DRVDD + 0.2 V
CLK+, CLK−	AGND	−0.3 V to AVDD1 + 0.2 V
VIN+, VIN−	AGND	−0.3 V to +3.6 V
XVREF	AGND	−0.3 V to AVDD1 + 0.2 V
SCLK, CSB, SDIO	AGND	−0.3 V to SPIVDD + 0.2 V
Environmental		
Operating Temperature Range (Ambient)		−40°C to +85°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature Range (Ambient)		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JB}[1, 3, 4]	θ_{JC}[1, 5]	Unit
0.0	15.7°C/W	7.5°C/W	0.5°	°C/W
1.0	13.7°C/W	N/A	N/A	°C/W
2.5	12.3°C/W	N/A	N/A	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] N/A = not applicable.
[5] Per MIL-STD 883, Method 1012.1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

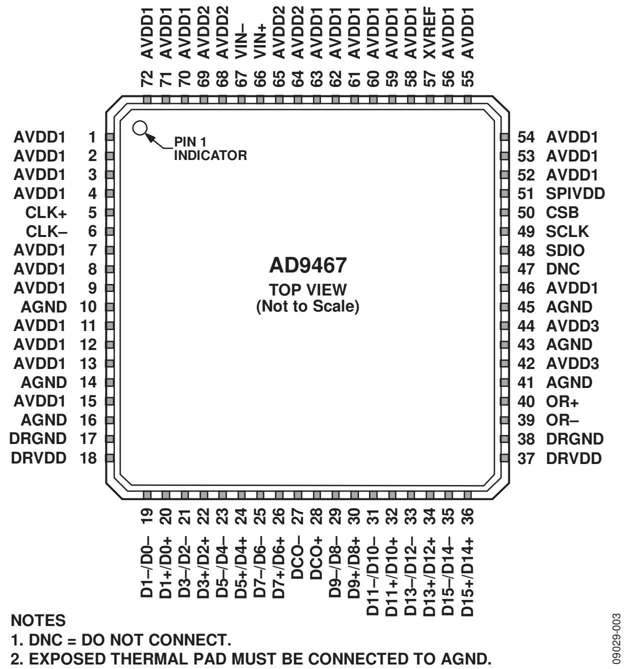

Figure 3. Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Paddle. The exposed paddle must be connected to AGND.
10, 14, 16, 41, 43, 45	AGND	Analog Ground.
1, 2, 3, 4, 7, 8, 9, 11, 12, 13, 15, 46, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 63, 70, 71, 72	AVDD1	1.8 V Analog Supply.
64, 65, 68, 69	AVDD2	3.3 V Analog Supply.
42, 44	AVDD3	1.8 V Analog Supply.
51	SPIVDD	1.8 V or 3.3 V SPI Supply
17, 38	DRGND	Digital Output Driver Ground.
18, 37	DRVDD	1.8 V Digital Output Driver Supply.
67	VIN–	Analog Input Complement.
66	VIN+	Analog Input True.
6	CLK–	Clock Input Complement.
5	CLK+	Clock Input True.
19	D1–/D0–	D1 and D0 (LSB) Digital Output Complement.
20	D1+/D0+	D1 and D0 (LSB) Digital Output True.
21	D3–/D2–	D3 and D2 Digital Output Complement.
22	D3+/D2+	D3 and D2 Digital Output True.
23	D5–/D4–	D5 and D4 Digital Output Complement.
24	D5+/D4+	D5 and D4 Digital Output True.
25	D7–/D6–	D7 and D6 Digital Output Complement.
26	D7+/D6+	D7 and D6 Digital Output True.
29	D9–/D8–	D9 and D8 Digital Output Complement.
30	D9+/D8+	D9 and D8 Digital Output True.
31	D11–/D10–	D11 and D10 Digital Output Complement.
32	D11+/D10+	D11 and D10 Digital Output True.
33	D13–/D12–	D13 and D12 Digital Output Complement.
34	D13+/D12+	D13 and D12 Digital Output True.
35	D15–/D14–	D15 (MSB) and D14 Digital Output Complement.

Pin No.	Mnemonic	Description
36	D15+/D14+	D15 (MSB) and D14 Digital Output True.
27	DCO−	Data Clock Digital Output Complement.
28	DCO+	Data Clock Digital Output True.
39	OR−	Out-of-Range Digital Output Complement.
40	OR+	Out-of-Range Digital Output True.
47	DNC	Do Not Connect (Leave Pin Floating).
48	SDIO	Serial Data Input/Output.
49	SCLK	Serial Clock.
50	CSB	Chip Select Bar.
57	XVREF	External VREF Option.

EQUIVALENT CIRCUITS

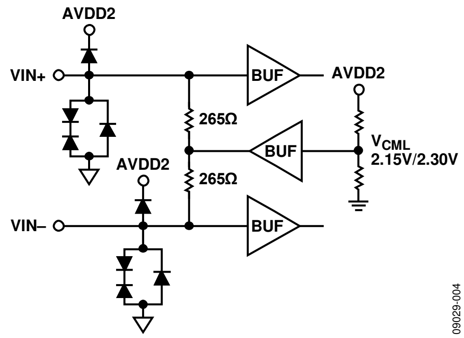

Figure 4. Equivalent Analog Input Circuit

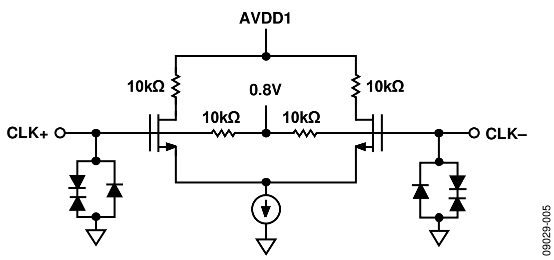

Figure 5. Equivalent Clock Input Circuit

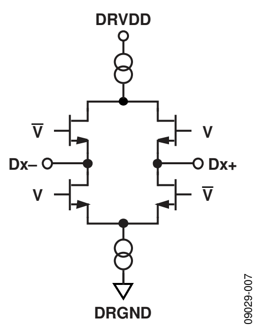

Figure 6. Equivalent Digital Output Circuit

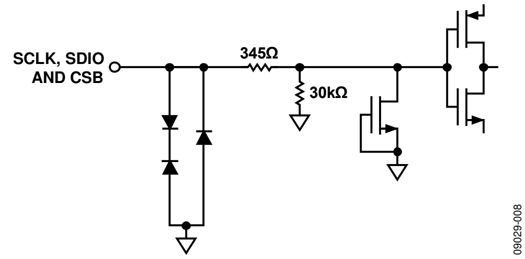

Figure 7. Equivalent SCLK, SDIO, and CSB Input Circuit

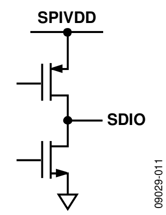

Figure 8. Equivalent SDIO Output Circuit

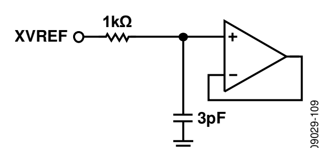

Figure 9. Equivalent External VREF Input Circuit (When Enabled)

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted, buffer current optimized for best SFDR performance.

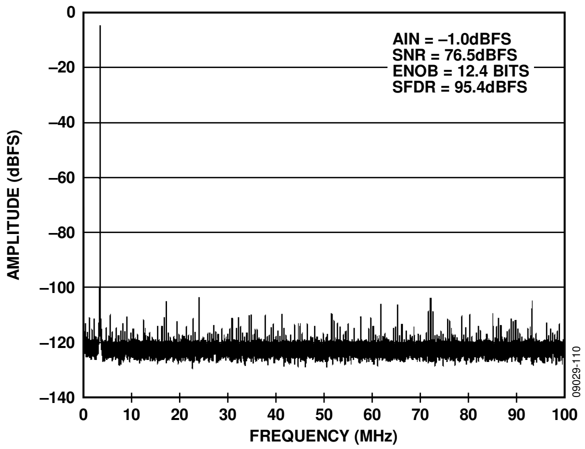

Figure 10. Single-Tone FFT with f_{IN} = 4.3 MHz, 2.5 V p-p FS, AD9467-200

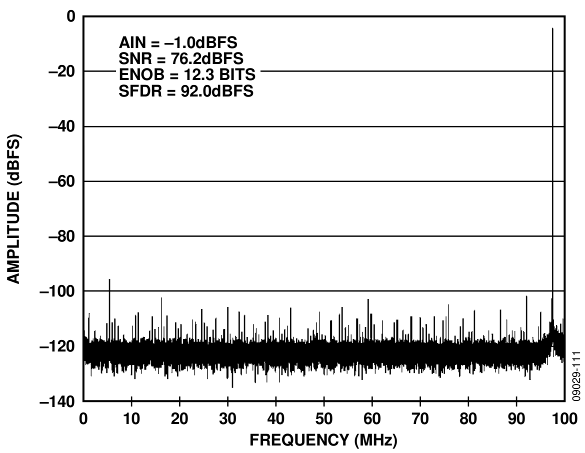

Figure 11. Single-Tone FFT with f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-200

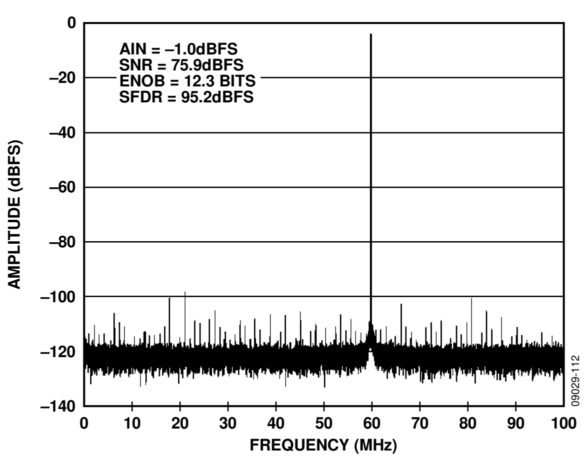

Figure 12. Single-Tone FFT with f_{IN} = 140.3 MHz, 2.5 V p-p FS, AD9467-200

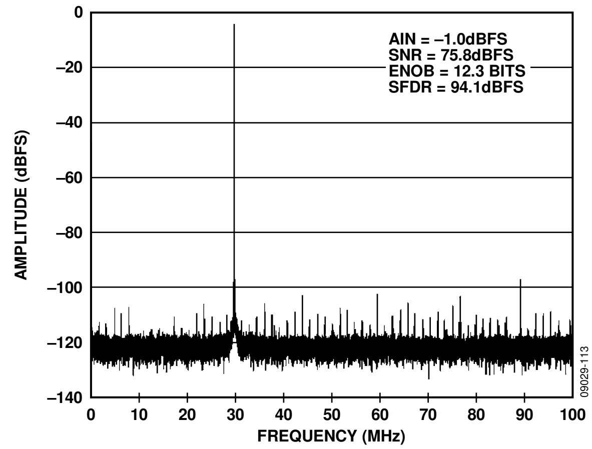

Figure 13. Single-Tone FFT with f_{IN} = 170.3 MHz, 2.5 V p-p FS, AD9467-200

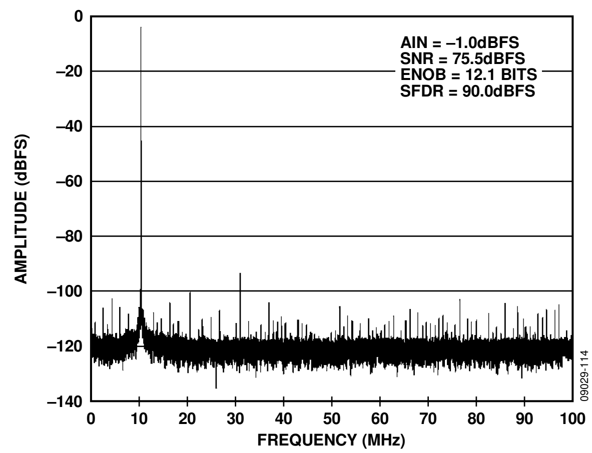

Figure 14. Single-Tone FFT with f_{IN} = 210.3 MHz, 2.5 V p-p FS, AD9467-200

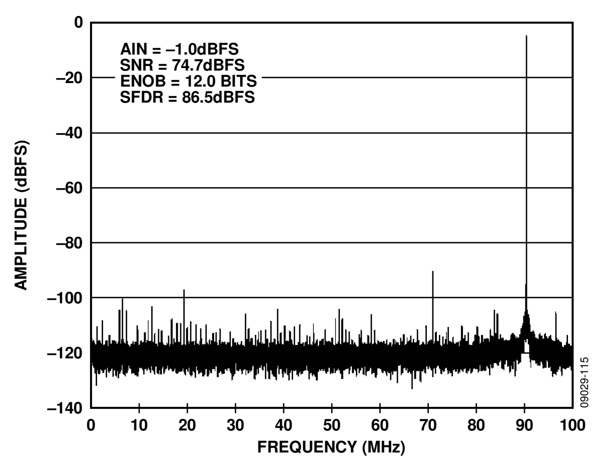

Figure 15. Single-Tone FFT with f_{IN} = 290.3 MHz, 2.5 V p-p FS, AD9467-200

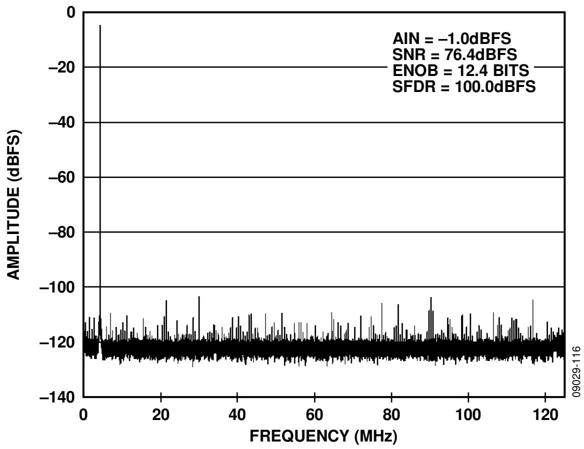

Figure 16. Single-Tone FFT with f_{IN} = 4.3 MHz, 2.5 V p-p FS, AD9467-250

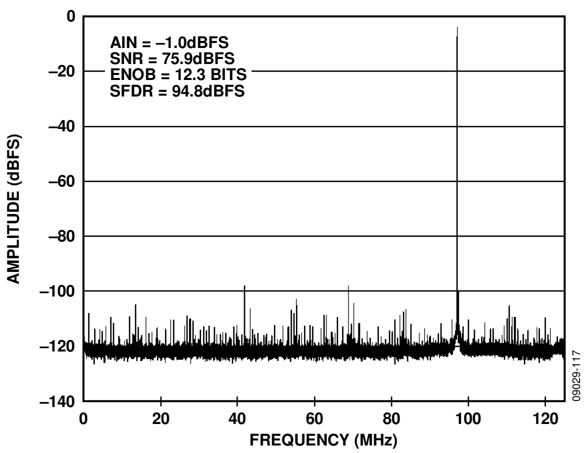

Figure 17. Single-Tone FFT with f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-250

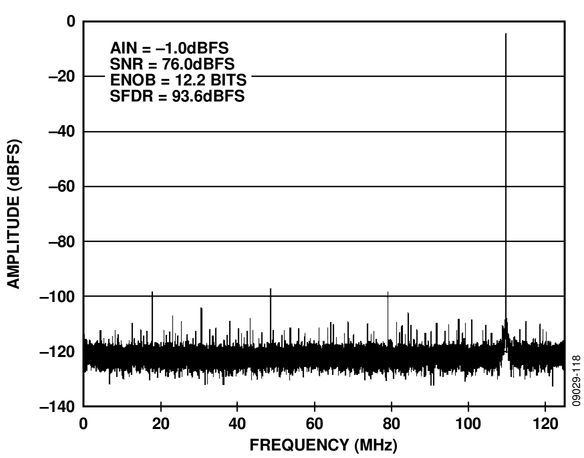

Figure 18. Single-Tone FFT with f_{IN} = 140.3 MHz, 2.5 V p-p FS, AD9467-250

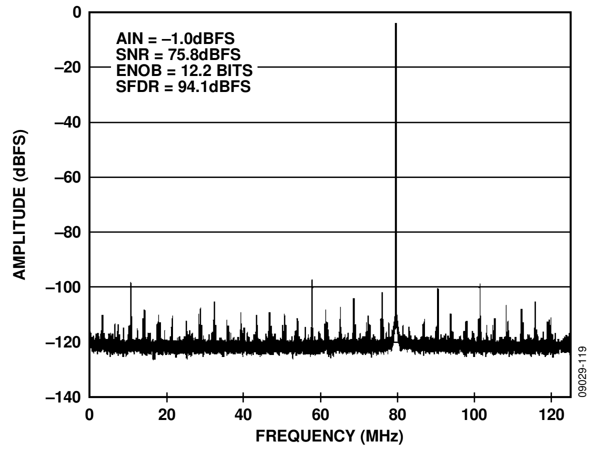

Figure 19. Single-Tone FFT with f_{IN} = 170.3 MHz, 2.5 V p-p FS, AD9467-250

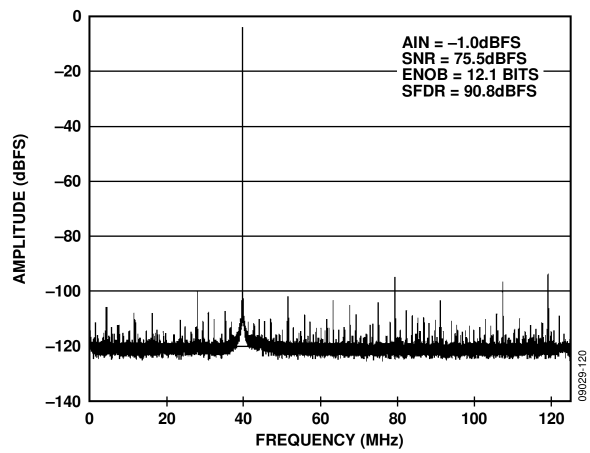

Figure 20. Single-Tone FFT with f_{IN} = 210.3 MHz, 2.5 V p-p FS, AD9467-250

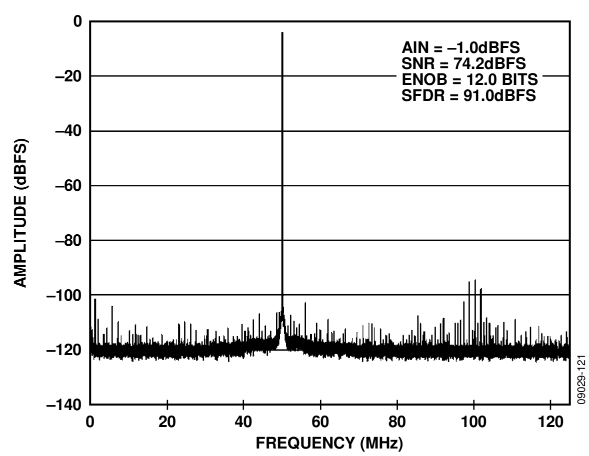

Figure 21. Single-Tone FFT with f_{IN} = 300.3 MHz, 2.5 V p-p FS, AD9467-250

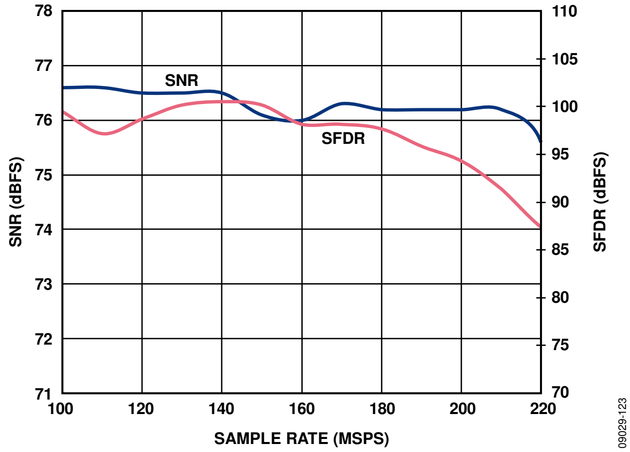

Figure 22. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-200

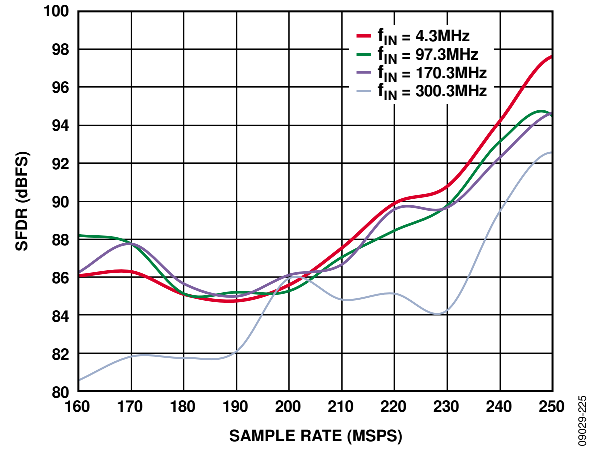

Figure 25. SFDR vs. f_{SAMPLE}, 2.5 V p-p FS, AD9467-250

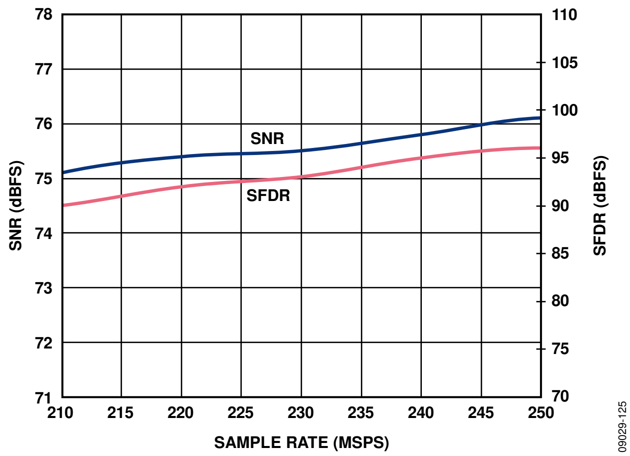

Figure 23. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-250

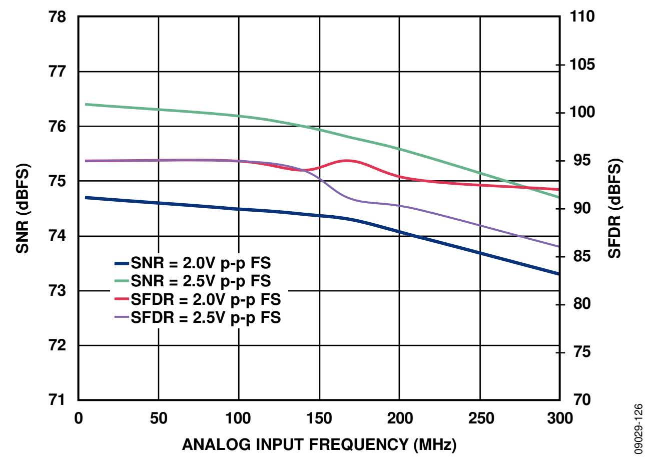

Figure 26. SNR/SFDR vs. f_{IN}, 2.0/2.5 V p-p FS, AD9467-200

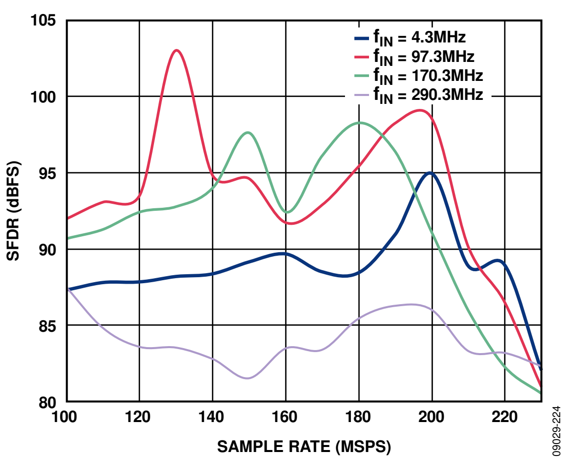

Figure 24. SFDR vs. f_{SAMPLE}, 2.5 V p-p FS, AD9467-200

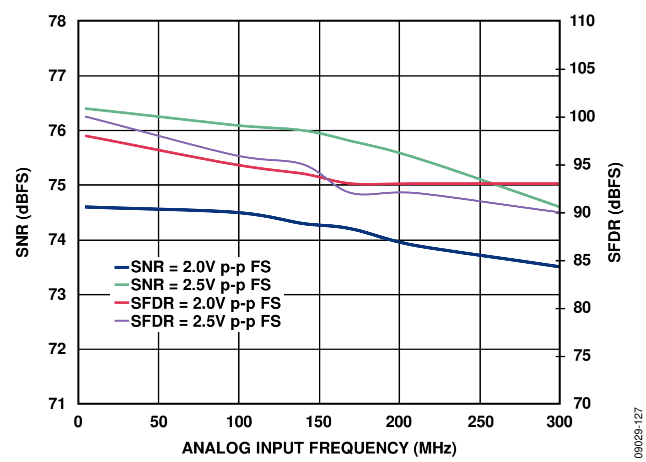

Figure 27. SNR/SFDR vs. f_{IN}, 2.0/2.5 V p-p FS, AD9467-250

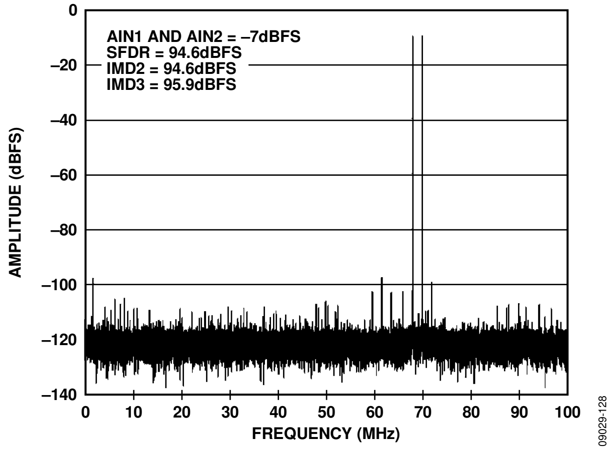

Figure 28. Two-Tone FFT with f_{IN1} = 70 MHz and f_{IN2} = 72 MHz, 2.5 V p-p FS, AD9467-200

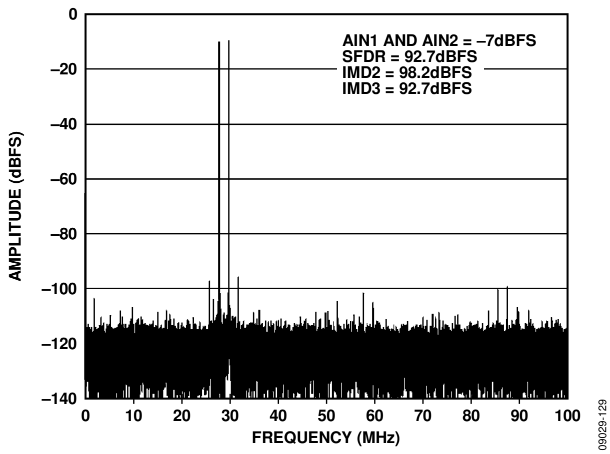

Figure 29. Two-Tone FFT with f_{IN1} = 170 MHz and f_{IN2} = 172 MHz, 2.5 V p-p FS, AD9467-200

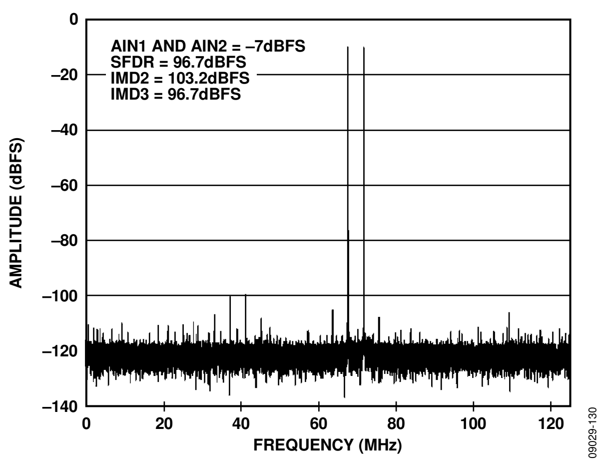

Figure 30. Two-Tone FFT with f_{IN1} = 70 MHz and f_{IN2} = 72 MHz, 2.5 V p-p FS, AD9467-250

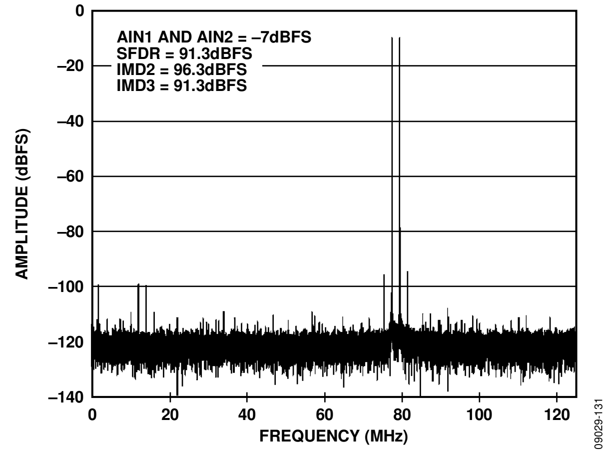

Figure 31. Two-Tone FFT with f_{IN1} = 170 MHz and f_{IN2} = 172 MHz, 2.5 V p-p FS, AD9467-250

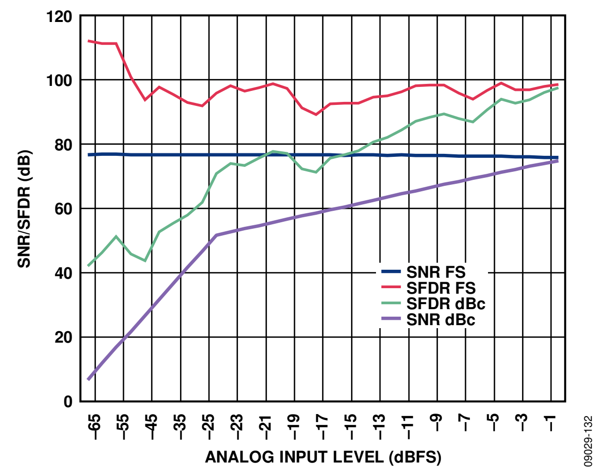

Figure 32. SNR/SFDR vs. Analog Input Level, f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-200

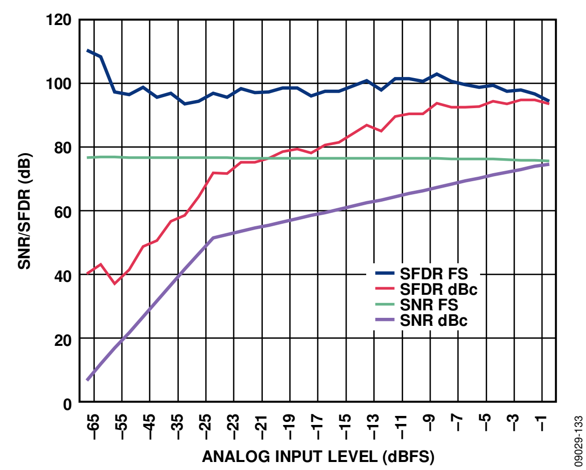

Figure 33. SNR/SFDR vs. Analog Input Level, f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-250

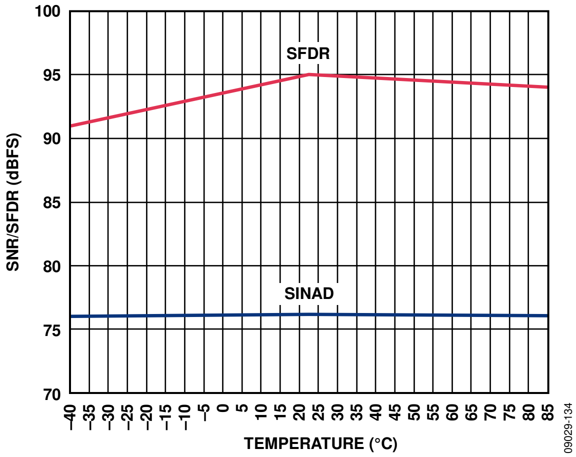

Figure 34. SINAD/SFDR vs. Temperature, f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-200

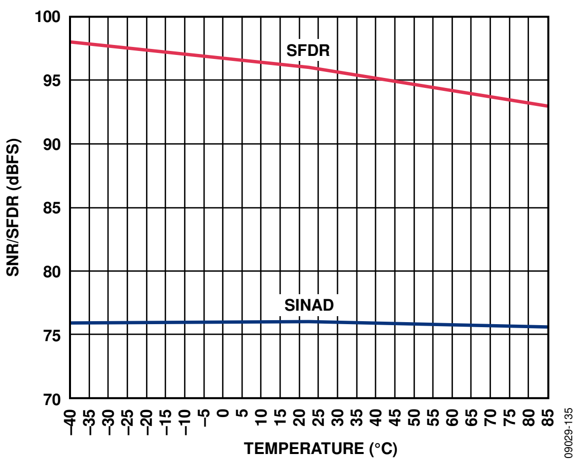

Figure 35. SINAD/SFDR vs. Temperature, f_{IN} = 97.3 MHz, 2.5 V p-p FS, AD9467-250

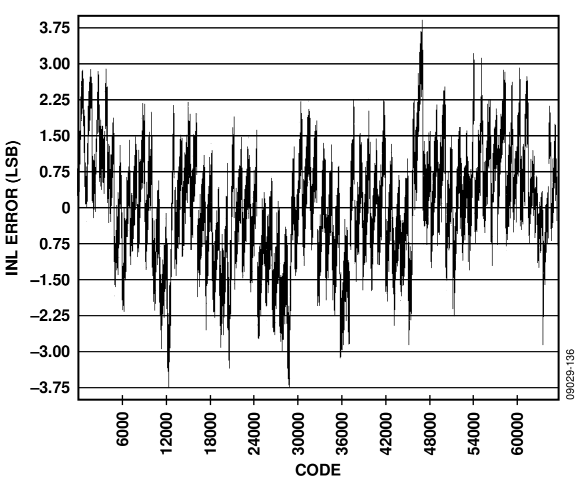

Figure 36. INL, f_{IN} = 4.3 MHz, 2.5 V p-p FS, AD9467-200

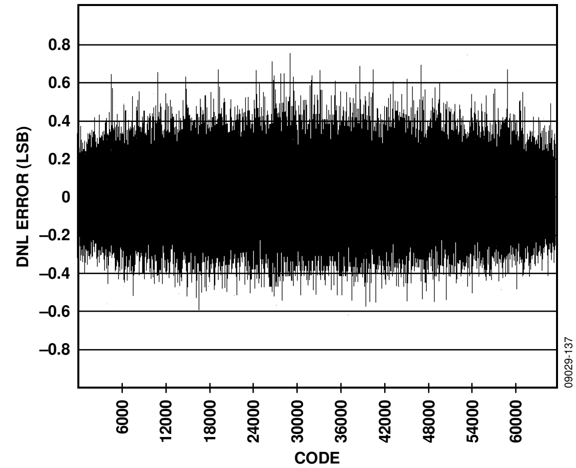

Figure 37. DNL, f_{IN} = 4.3 MHz, 2.5 V p-p FS, AD9467-200

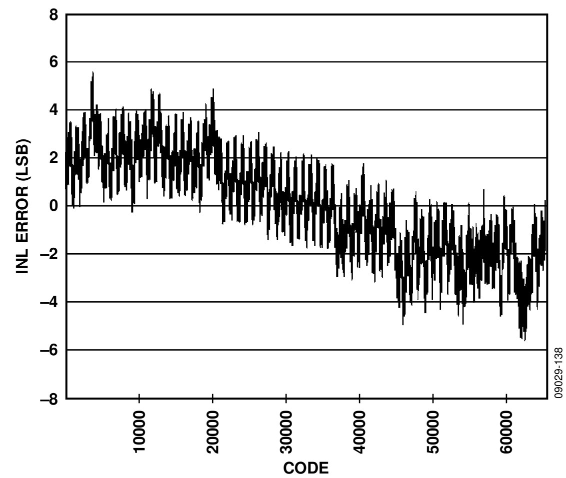

Figure 38. INL, f_{IN} = 4.3 MHz, 2.5 V p-p FS, AD9467-250

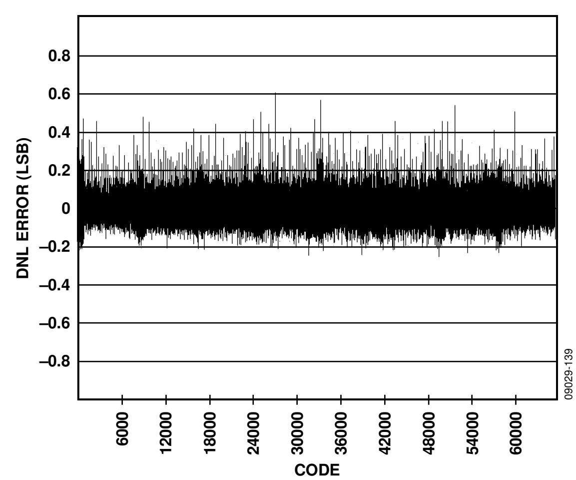

Figure 39. DNL, f_{IN} = 4.3 MHz, 2.5 V p-p FS, AD9467-250

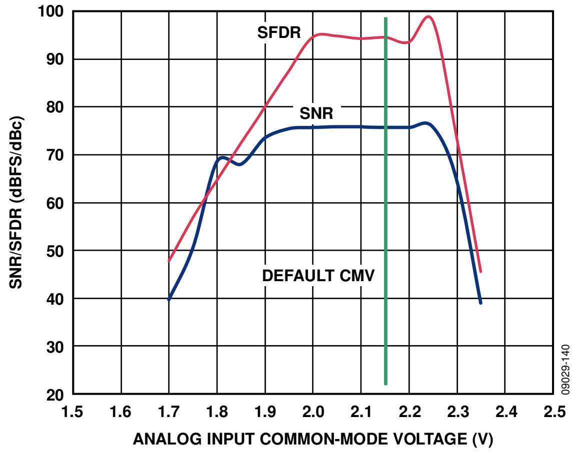

Figure 40. SNR/SFDR vs. Analog Input Common-Mode Voltage, AIN = 100 MHz, 2.5 V p-p FS, AD9467-250

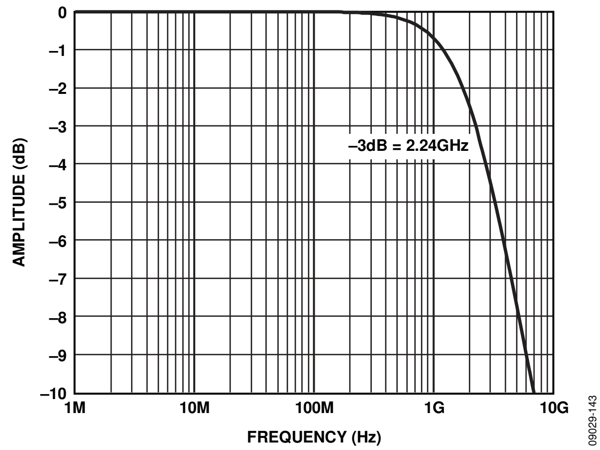

Figure 43. Converter AC Bandwidth AD9467-250

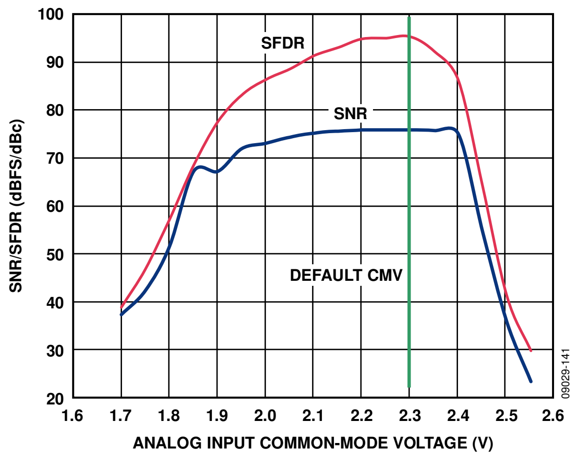

Figure 41. SNR/SFDR vs. Analog Input Common-Mode Voltage, AIN = 100 MHz, 2.5 V p-p FS, AD9467-200

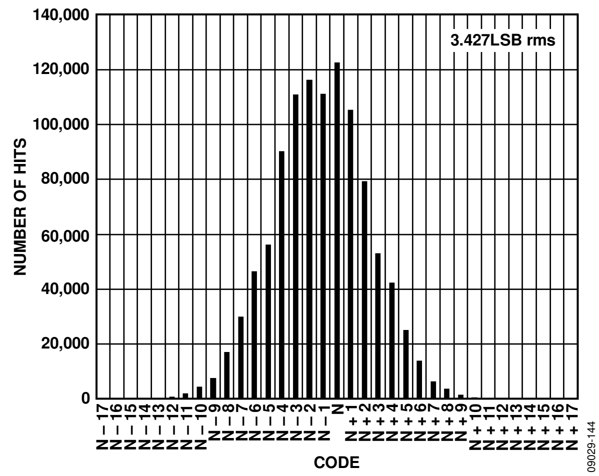

Figure 44. Input-Referred Noise Histogram, 2.5 V p-p FS, AD9467-200

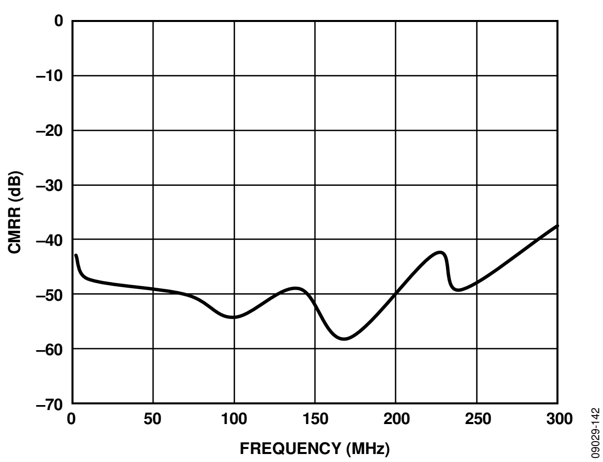

Figure 42. Common-Mode Rejection Ratio (CMRR), AD9467-250

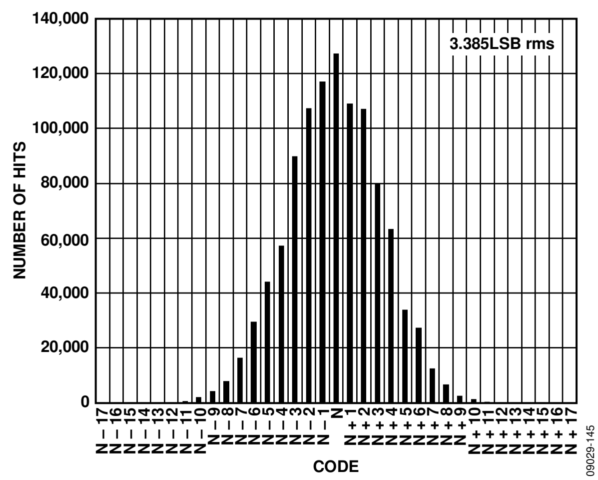

Figure 45. Input-Referred Noise Histogram, 2.5 V p-p FS, AD9467-250

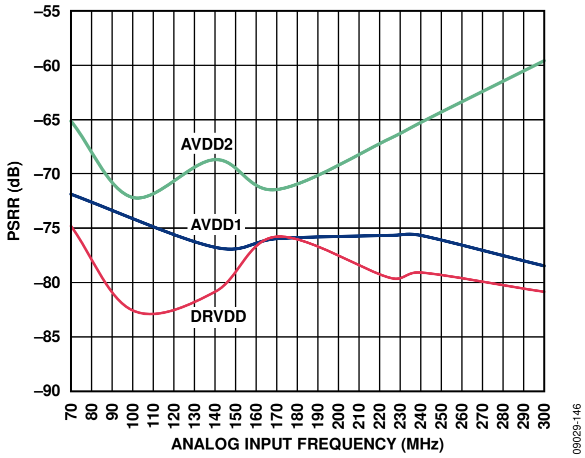

Figure 46. Power Supply Rejection (PSR), AD9467-250

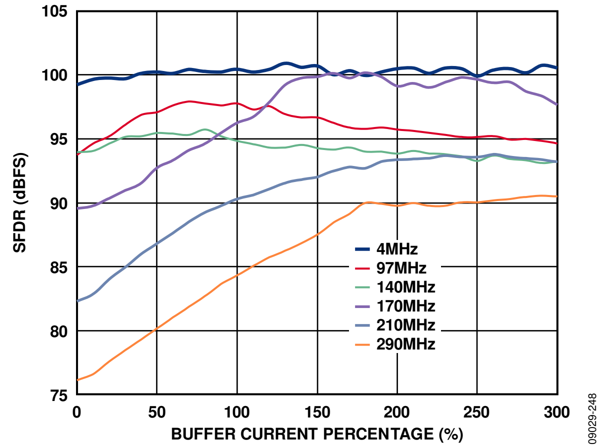

Figure 48. SFDR Performance vs. Buffer Current Percentage Over Analog Input Frequency, AD9467-250

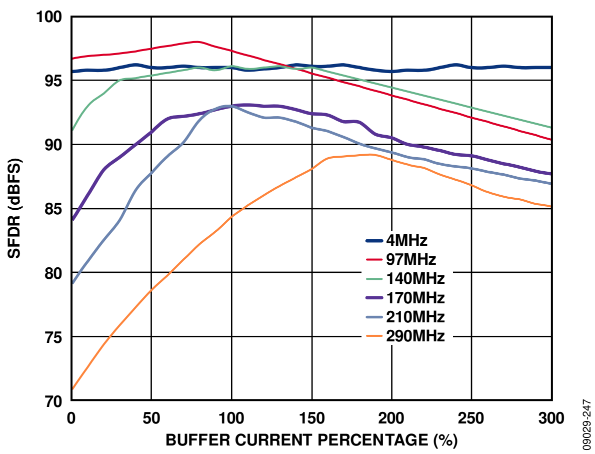

Figure 47. SFDR Performance vs. Buffer Current Percentage Over Analog Input Frequency, AD9467-200

THEORY OF OPERATION

The AD9467 architecture consists of an input-buffered pipelined ADC that consists of a 3-bit first stage, a 4-bit second stage, followed by four 3-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stage.

The input buffer provides a linear high input impedance (for ease of drive) and reduces the kick-back from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9467 is a differential buffer. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal.

In either case, a small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, the AN-935 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the default case of the AD9467, the largest input span available is 2.5 V p-p. For other input full-scale options, see the Full-Scale and Reference Options section.

SFDR Optimization—Buffer Current Adjustment

Using Register 36 and Register 107, the buffer currents can be changed as a percentage to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, this does change the amount of current required by AVDD2. However, the current consumption is small in comparison to the overall currents required by this supply. The current specifications listed in Table 1 incorporate this variation. For a complete list of buffer current settings, see Table 13 for more details.

The following buffer current settings reflect the performance that can be achieved using the input networks as described in Figure 51 and Figure 52. These curves describe the percentages used to obtain data sheet typical specifications for both the 250 MSPS and 200 MSPS parts. For example, when using IFs from 150 MHz to 250 MHz, 160% is actually the average of the entire buffer current. Therefore, both Register 36 and Register 107 need to be set to 160%.

AD9467BCPZ-250 buffer current settings:

- DC to 150 MHz at 80% (default setting)
- 150 MHz to 250 MHz at 160%
- 250 MHz and higher at 210%

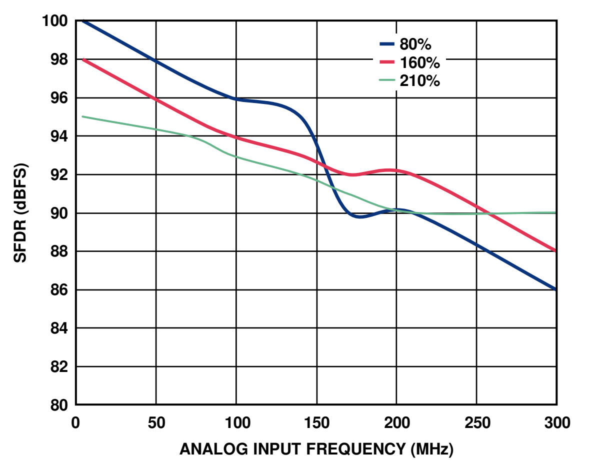

Figure 49. Buffer Current Sweeps, 2.5 V p-p, AD9467-250

AD9467BCPZ-200 buffer current settings:

- DC to 150 MHz at 80% (default setting)
- 150 MHz to 250 MHz at 100%
- 250 MHz and higher at 160%

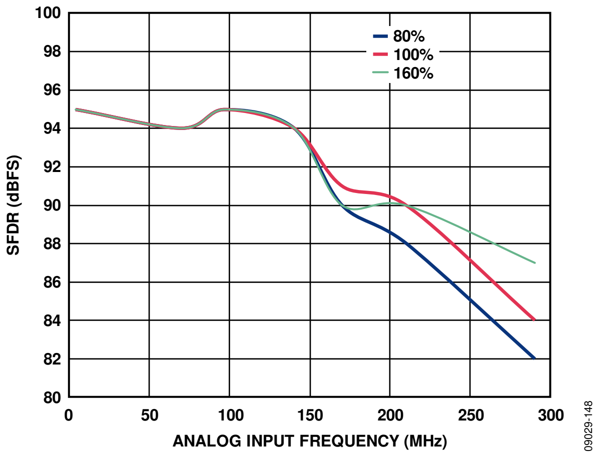

Figure 50. Buffer Current Sweeps, 2.5 V p-p, AD9467-200

Note that for sample rates less than 150 MSPS and analog inputs less than 100 MHz, it is recommended to set the buffer current to 0%. Depending on the input network design and frequency band of interest, the optimum buffer current settings may be slightly different than the input network recommendations shown in Figure 53 and Figure 54.

Differential Input Configurations

There are several ways to drive the AD9467, either actively or passively; however, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 51 and Figure 52) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9467.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed (see Figure 51, Figure 52, and Figure 53)

Using the ADL5562 or ADL5201 differential drivers to drive the AD9467 provides an excellent and flexible gain option to interface to the ADC (see Figure 54 and Figure 56) for both baseband and high IF applications. Using an amplifier also provides better isolation from the preceding stages as well as better pass-band flatness. Performance plots of these amplifiers can also be seen in Figure 55 and Figure 57.

When using any dc-coupled amplifier, the user has the option to disconnect the input common-mode voltage buffer from the analog inputs. This allows the common-mode output pin of the amplifier to set this voltage between the interface of the two devices. Otherwise, use an ac coupling capacitor in series on each of the analog input as shown in Figure 54 for IF applications that do not require dc coupling. See the Memory Map section for more details.

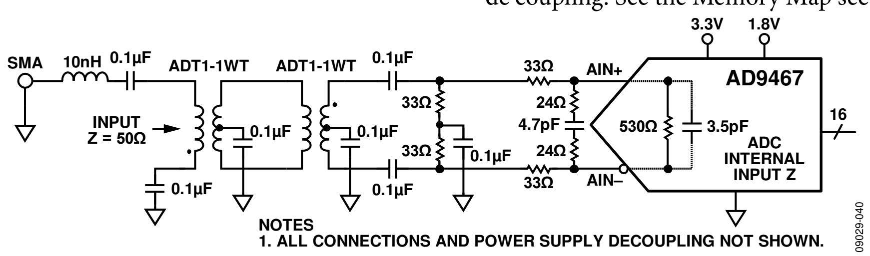

Figure 51. Differential Transformer-Coupled Configuration for Baseband Applications up to 150 MHz

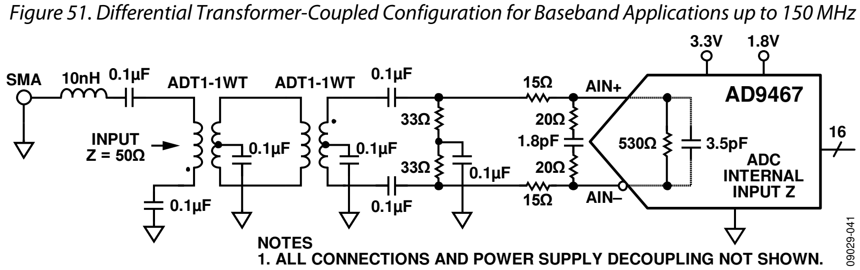

Figure 52. Differential Transformer-Coupled Configuration for IF Applications from 150 MHz to 300 MHz

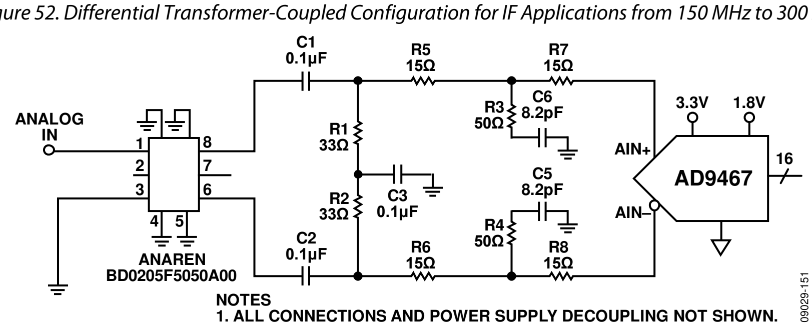

Figure 53. Wideband Balun-Coupled Configuration for IF Applications Up Greater Than 100 MHz

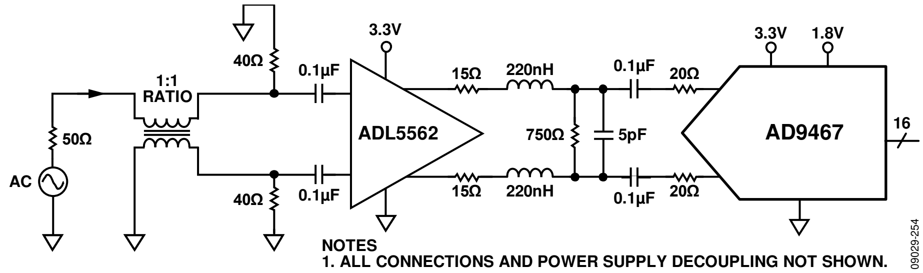

Figure 54. Wideband Differential Amplifier Input Configuration Using the ADL5562

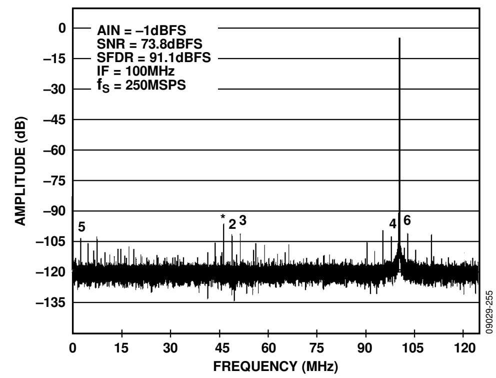

Figure 55. Single-Tone FFT Performance Plot Using the ADL5562 Amplifier, Gain = 6 dB, and the AD9467-250

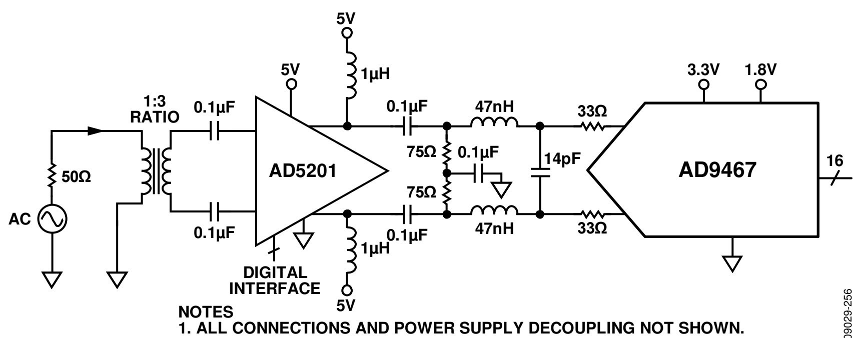

Figure 56. Wideband Differential VGA Input Configuration Using the ADL5201

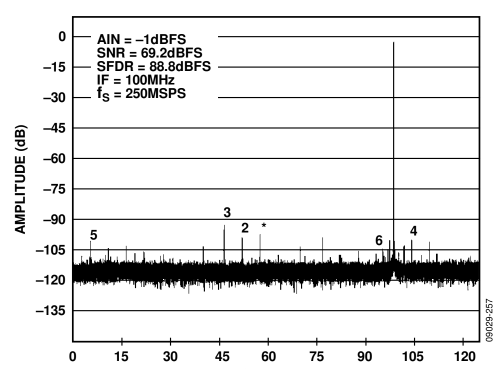

Figure 57. Single-Tone FFT Performance Plot Using the ADL5201 VGA, Gain = 20 dB, and the AD9467-250

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9467 sample clock inputs (CLK+ and CLK−) should be clocked with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Figure 58 shows a preferred method for clocking the AD9467. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9467 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9467, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

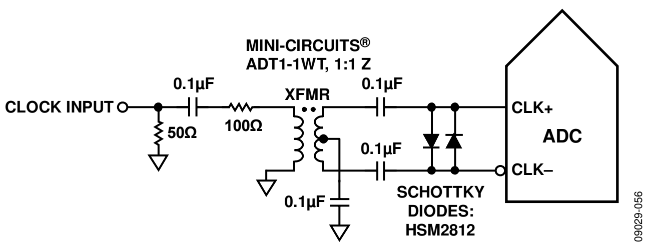

Figure 58. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL or LVDS signal to the sample clock input pins, as shown in Figure 59 and Figure 60. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9520/AD9522/AD9523/AD9524 family of clock drivers offers excellent jitter performance.

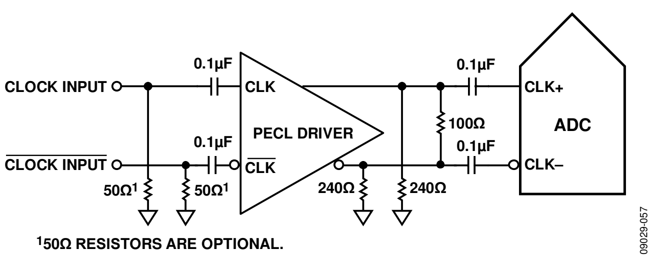

Figure 59. Differential PECL Sample Clock

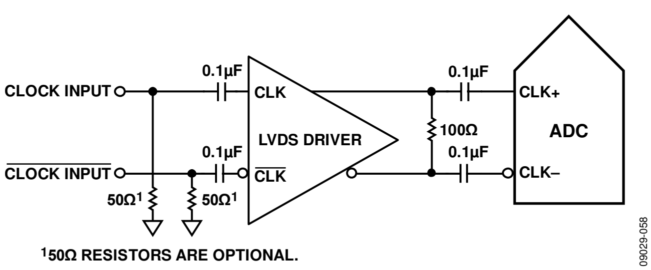

Figure 60. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9467 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9467.

Any changes to the sampling frequency require several clock cycles to allow the internal timing to acquire and lock at the new sampling rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20 \times \log 10(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 61).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9467. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

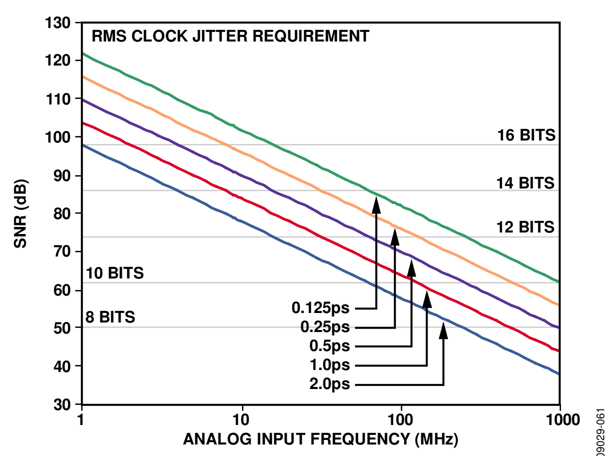

Figure 61. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 62, the power dissipated by the AD9467 is proportional to its sample rate. The output power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

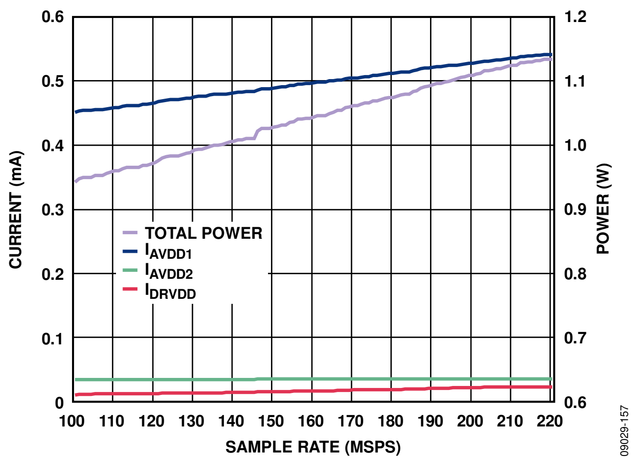

Figure 62. Supply Current vs. f_{SAMPLE} for f_{IN} = 5 MHz, AD9467-200

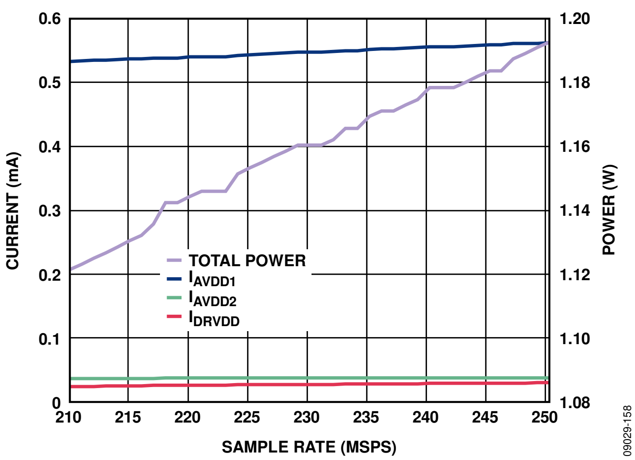

Figure 63. Supply Current vs. f_{SAMPLE} for f_{IN} = 5 MHz, AD9467-250

By asserting the power-down option via the SPI register map (0x08[1:0]), the AD9467 is placed into power-down mode. In this state, the ADC typically dissipates 5 mW. During power-down, the LVDS output drivers are placed in a high impedance state.

In power-down mode, low power dissipation is achieved by shutting down the internal reference, reference buffer, digital output, and biasing networks. The device requires approximately 100 ms to restore full operation.

See the Memory Map section for more details on using these features.

Power Supplies

To achieve the best dynamic performance of the AD9467, it is recommended that each power supply pin be decoupled as closely to the package as possible with 0.1 µF, X7R or X5R type decoupling capacitors. For optimum performance, all supplies should be at typical values or slightly higher to accommodate elevated temperature drifts, which depend on the application.

Full-Scale and Reference Options

The analog inputs support both an input full scale of 2.5 V p-p (default) and 2.0 V p-p differentially. Choosing one full-scale input range over the other presents some trade-offs to the user. Using an input full scale of 2.5 V p-p yields the best SNR performance. If system trade-offs require improved SFDR performance, then a 2.0 V p-p input full scale should be used. However, in this mode, SNR degrades by roughly 2 dB. Other input full-scale ranges are available for use between 2.0 V p-p and 2.5 V p-p. See Register 18 in Table 13 and the Memory Map section for details.

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve gain matching when using multiple ADCs.

The internal reference can be disabled via the SPI, allowing the use of an external reference. See the Memory Map section for more details. The external reference is loaded by the input of an internal buffer amplifier having 3 pF of capacitance to ground. There is also a 1 kΩ internal resistor in series with the input of that buffer. The external reference must be limited to a nominal 1.25 V for an input full-scale swing of 2.5 V p-p. Additional capacitance may be necessary to keep this pin quiet depending on the external reference used.

When not using the XVREF pin, it must be tied to ground directly or through a 0.1 µF decoupling capacitor. However, keep this pin quiet regardless.

Digital Outputs and Timing

The AD9467 differential outputs conform to the ANSI-644 LVDS standard on default power-up. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.0 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 300 mV swing at the receiver.

The AD9467 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be no longer than 18 inches and that the differential output traces be kept close together and at equal lengths. An example of the DCO and data with proper trace length and position is shown in Figure 64.

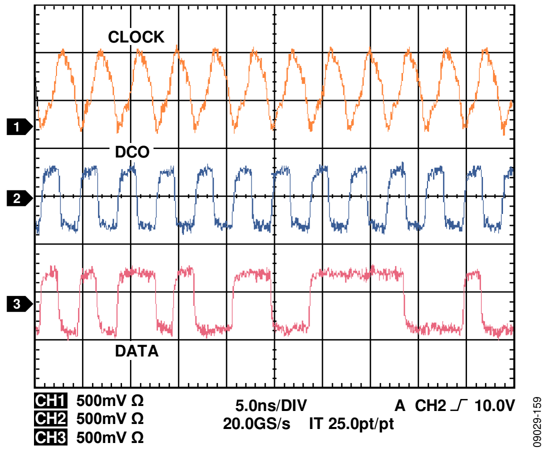

Figure 64. Output Timing Example in LVDS Mode (Default), AD9467-250

An example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of six inches on standard FR-4 material is shown in Figure 65. It is the responsibility of the user to determine if the waveforms meet the timing budget of the design.

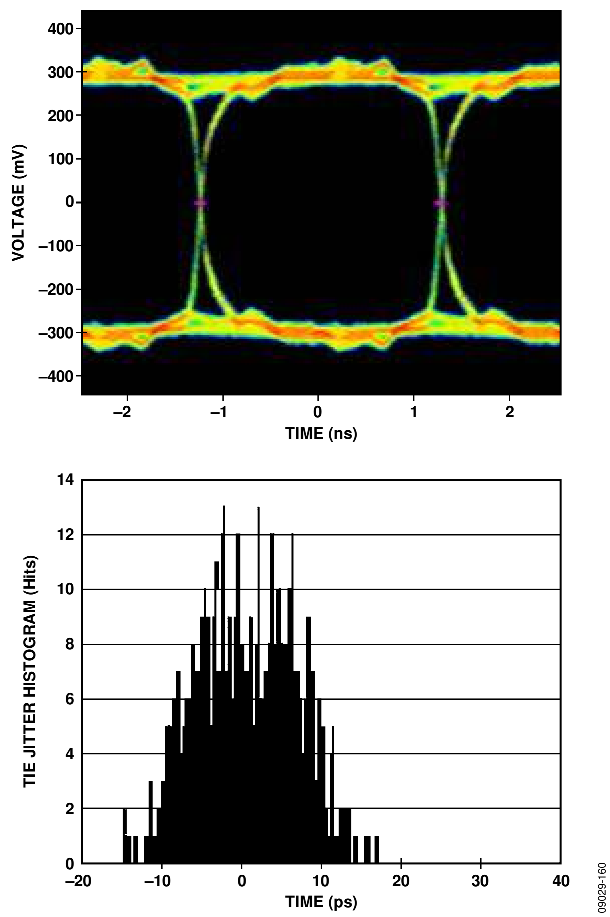

Figure 65. Data Eye for LVDS Outputs in ANSI-644 Mode with 6-Inch Trace Lengths on Standard FR-4, AD9467-250

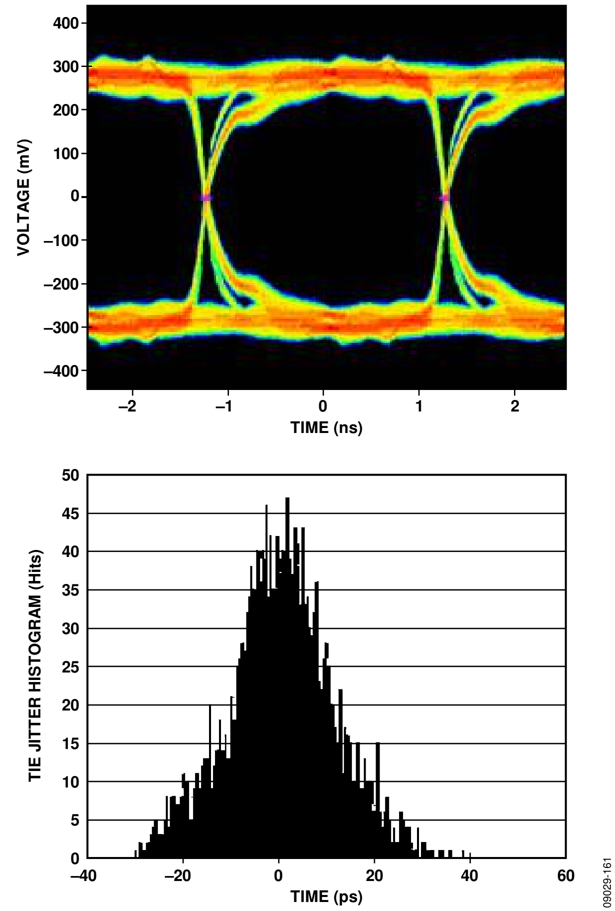

Figure 66. Data Eye for LVDS Outputs in ANSI-644 Mode with 18-Inch Trace Lengths on Standard FR-4, AD9467-250

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 8. To change the output data format to twos complement or Gray code, see the Memory Map section.

Table 8. Digital Output Coding

Code	(VIN+) − (VIN−), Input Span = 2.5 V p-p (V)	Digital Output Offset Binary (D15:D0)
65,536	+1.25	1111 1111 1111 1111
32,768	0.00	1000 0000 0000 0000
32,767	−0.000038	0111 1111 1111 1111
0	−1.25	0000 0000 0000 0000

An output clock is provided to assist in capturing data from the AD9467. Data is clocked out of the AD9467 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. See the timing diagram shown in Figure 2 for more information.

There are eight digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 10 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. Note that some patterns may not adhere to the data format select option.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The only difference is that the starting value must be a specific value instead of all 1s (see Table 9 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The only differences are that the starting value must be a specific value instead of all 1s (see Table 9 for the initial values) and the AD9467 inverts the bit stream with relation to the ITU standard.

Table 9. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN 9 Sequence, Short	0xFFFF	0x87BE, 0xAE64, 0x929D
PN 23 Sequence, Long	0x7FFF	0x7E00, 0x807C, 0x801F

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

Overrange (OR) Output Pins

The OR+ and OR− output pins indicate when an applied analog input is above or below the input full scale of the converter.

If the analog input is in an overrange condition, the OR bit goes high, coinciding with output data hitting above or below full-scale. The delay between the time the part actually overranges and the OR bit going high is the pipeline latency of the part.

SPI Pins: SCLK, SDIO, CSB

For normal SPI operation, these pins should be tied to AGND through a 100 kΩ resistor on each pin. These pins are both 1.8 V and 3.3 V tolerant. However, the SDIO output logic level is dependent on the bias of the SPIVDD pin. For 3.3 V output logic, tie SPIVDD to 3.3 V (AVDD2). For 1.8 V output logic, tie SPIVDD to 1.8 V (AVDD1).

The CSB pin should be tied to AVDD1 for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored.

Table 10. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A[1]	N/A[1]	N/A[1]
0001	Midscale short	1000 0000 0000 0000	Same	Yes
0010	+Full-scale short	1111 1111 1111 1111	Same	Yes
0011	−Full-scale short	0000 0000 0000 0000	Same	Yes
0100	Checkerboard	1010 1010 1010 1010	0101 0101 0101 0101	No
0101	PN sequence long[2]	N/A[1]	N/A[1]	Yes
0110	PN sequence short[2]	N/A[1]	N/A[1]	Yes
0111	One-/zero-word toggle	1111 1111 1111 1111	0000 0000 0000 0000	No

[1] N/A = not applicable.
[2] All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths to verify data capture to the receiver.

SERIAL PORT INTERFACE (SPI)

The AD9467 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided down into fields, as detailed in the Memory Map section. Detailed operational information can be found in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

There are three pins that define the SPI: SCLK, SDIO, and CSB (see Table 11). The SCLK pin is used to synchronize the read and write data presented to the ADC. The SDIO pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 11. Serial Port Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin. The typical role for this pin is an input or output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip select bar (active low). This control gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 68 and Table 12. During normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDIO to process instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This allows complete memory transfers without requiring additional instructions. Regardless of the mode, if CSB is taken high in the middle of a byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port configuration influences how the AD9467 operates. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 11 compose the physical interface between the programming device of the user and the serial port of the AD9467. The SCLK and CSB pins function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

If multiple SDIO pins share a common connection, care should be taken to ensure that proper V_{OH} levels are met. Assuming the same load for each AD9467, Figure 67 shows the number of SDIO pins that can be connected together and the resulting V_{OH} level.

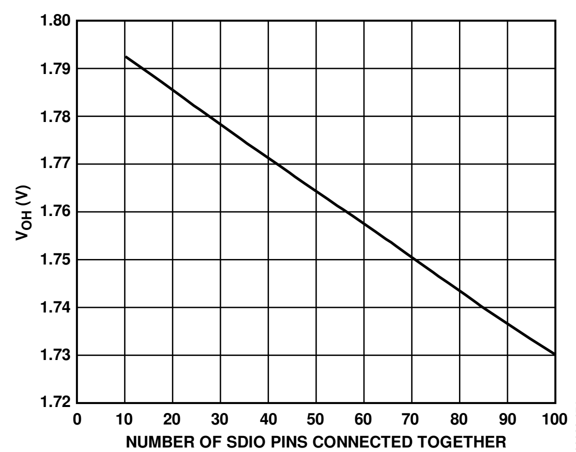

Figure 67. SDIO Pin Loading

This interface is flexible enough to be controlled by either serial PROMS or PIC mirocontrollers, providing the user with an alternative method, other than a full SPI controller, to program the ADC (see the AN-812 Application Note).

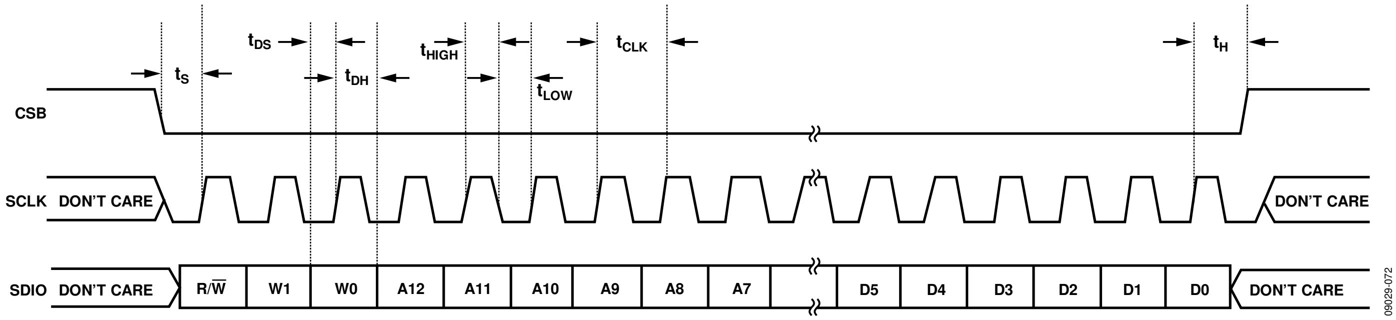

Figure 68. Serial Timing Details

Table 12. Serial Timing Definitions

Parameter	Timing (Minimum, ns)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HIGH}	16	Minimum period that SCLK should be in a logic high state
t_{LOW}	16	Minimum period that SCLK should be in a logic low state
t_{EN_SDIO}	10	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 68)
t_{DIS_SDIO}	10	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 68)

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map register table (see Table 13) has eight address locations. The memory map is divided into three sections: the chip configuration register map (Address 0x00 to Address 0x02), the device index and transfer register map (Address 0xFF), and the ADC functions register map (Address 0x08 to Address 0x107).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second right-most column. The (MSB) Bit 7 column is the start of the default hexadecimal value given. For example, Address 0x2C, the analog input register, has a default value of 0x00, meaning Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 0, or 0000 0000 in binary. This setting is the default for an ac-coupled analog input condition. By writing a 1 to Bit 2 of this address, the internal input common-mode buffer is disabled allowing a dc-coupled input for which the input common mode voltage can be set externally. For more information on this and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

When the AD9467 comes out of a reset, critical registers are preloaded with default values. These values are indicated in Table 13, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Table 13. Memory Map Register[1]

Addr. (Hex)	Parameter Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Register											
00	chip_port_config	X	LSB first 1 = on 0 = off (default)	Soft reset 1 = on 0 = off (default)	1	1	X	X	X	0x18	The nibbles should be mirrored so that LSB- or MSB-first mode is set correctly regardless of shift mode.
01	chip_id	8-Bit Chip ID Bits[7:0] (AD9467 = 0x50, default)								Read only	Default is unique chip ID, different for each device. This is a read-only register.
02	chip_grade	X	Child ID Bits[6:4] (identify device variants of chip ID) 001 = 200 MSPS 010 = 250 MSPS			X	X	X	X	Read only	Child ID used to differentiate graded devices.
Device Index and Transfer Register											
FF	device_update	X	X	X	X	X	X	X	SW transfer 1 = on 0 = off (default)	0x00	Synchronously transfers data from the master shift register to the slave.

Addr. (Hex)	Parameter Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Default Notes/ Comments
ADC Functions											
08	modes	X	X	X	X	X	X	Internal power-down mode 00 = chip run (default) 01 = full power-down		0x00	Determines various generic modes of chip operation.
0D	test_io	X	X	Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Output test mode—see Table 10 in the Digital Outputs and Timing section 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = −FS short 0100 = checkerboard output 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one-/zero-word toggle				0x00	When this register is set, the test data is placed on the output pins in place of normal data.
0F	adc_input	XVREF 1 = on 0 = off (default)	X	X	X	X	Analog disconnect 1 = on 0 = off (default)	X	X	0x00	Analog input functions.
10	offset	8-bit digital offset adjustment 0111 1111 = 127 0111 1110 = 126 … 0000 0010 = 2 0000 0001 = 1 0000 0000 = 0 1111 1111 = -1 1111 1110 = -2 … 1000 0001 = -126 1000 0000 = -127								0x00	Bipolar, twos complement digital offset adjustment in LSBs.
14	output_mode	X	0	X	Digital output disable 1 = on 0 = off (default)	1	Output invert 1 = on 0 = off (default)	Data format select 00 = offset binary (default) 01 = twos complement 10 = Gray code		0x08	Configures the outputs and the format of the data.
15	output_adjust	X	X	X	X	Coarse LVDS adjust 0 = 3.0 mA (default) 1 = 1.71 mA	Output current drive adjust 001 = 3.0 mA (default) 010 = 2.79 mA 011 = 2.57 mA 100 = 2.35 mA 101 = 2.14 mA 110 = 1.93 mA 111 = 1.71 mA			0x00	Determines LVDS or other output properties.
16	output_phase	DCO output invert 1 = on 0 = off (default)	X	X	X	X	X	X	X	0x00	Determines digital clock output phase.
18	vref	X	X	X	X	Input full-scale range adjust 0000 = 2.0 V p-p 0110 = 2.1 V p-p 0111 = 2.2 V p-p 1000 = 2.3 V p-p 1001 = 2.4 V p-p 1010 = 2.5 V p-p (default)				0x0A	

Addr. (Hex)	Parameter Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Default Notes/ Comments
2C	analog_input	X	X	X	X	X	Input coupling mode 0 = ac coupling (default) 1 = dc coupling	X	X	0x00	Determines the input coupling mode.
36	Buffer Current Select 1	110101 = +530% 110100 = +520% … 001000 = +80% (default) … 000010 = +20% 000001 = +10% 000000 = nominal, 0% 111111 = −10% 111110 = −20% … 110111 = −90% 110110 = −100%						1	0	0x22	
107	Buffer Current Select 2	110101 = +530% 110100 = +520% … 001000 = +80% (default) … 000010 = +20% 000001 = +10% 000000 = nominal, 0% 111111 = −10% 111110 = −20% … 110111 = −90% 110110 = −100%						X	X	0x20	

[1] X = undefined feature, don't write.

Power and Ground Recommendations

When connecting power to the AD9467, it is recommended that three separate supplies be used: one for analog AVDD1 and AVDD3 (1.8 V), one for analog AVDD2 (3.3 V), and one for digital output drivers DRVDD (1.8 V). If only one 1.8 V supply is available, it should be routed to AVDD1 and AVDD3 first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts, with minimal trace lengths.

A single PC board ground plane should be sufficient when using the AD9467. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance can be easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9467. An exposed continuous copper plane on the PCB should be connected to the AD9467 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 69 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

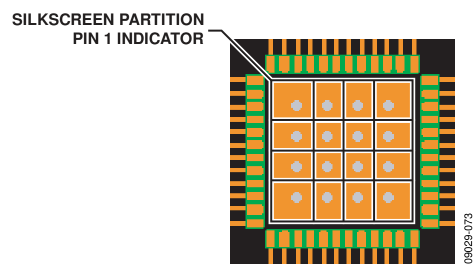

Figure 69. Typical PCB Layout

OUTLINE DIMENSIONS

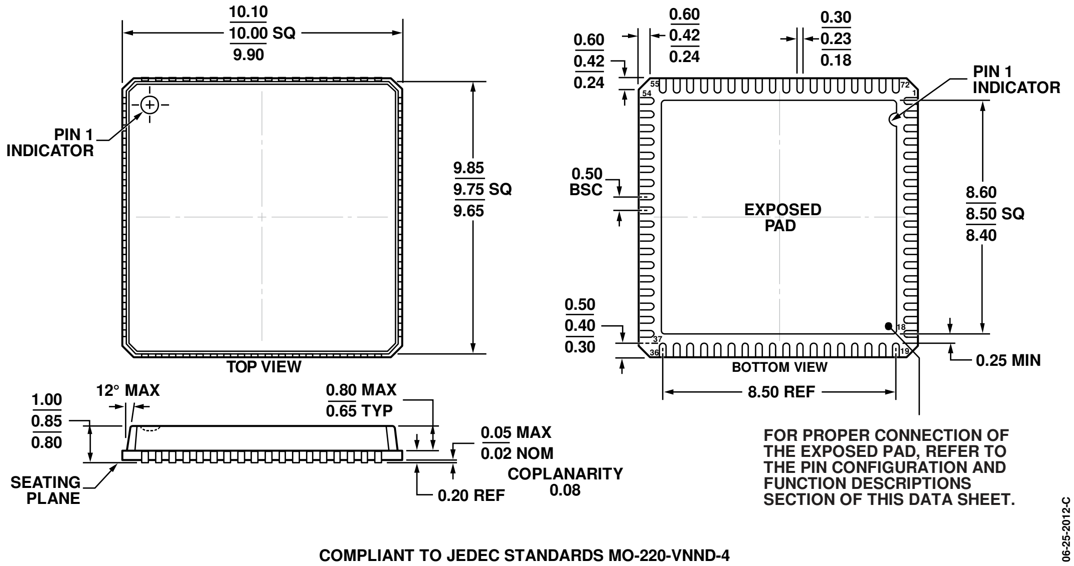

Figure 70. 72-Lead Lead Frame Chip Scale Package, Exposed Pad [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9467BCPZ-200	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-5
AD9467BCPZRL7-200	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-5
AD9467BCPZ-250	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-5
AD9467BCPZRL7-250	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-5
AD9467-200EBZ		AD9467-200 Evaluation Board	
AD9467-250EBZ		AD9467-250 Evaluation Board	
AD9467-FMC-250EBZ		AD9467-250 Native FMC Card	

[1] Z = RoHS Compliant Part.

D09029-0-2/13(D)