MC33260

GreenLine™ Compact Power Factor Controller: Innovative Circuit for Cost Effective Solutions

The MC33260 is a controller for Power Factor Correction preconverters meeting international standard requirements in electronic ballast and off−line power conversion applications. Designed to drive a free frequency discontinuous mode, it can also be synchronized and in any case, it features very effective protections that ensure a safe and reliable operation.

This circuit is also optimized to offer extremely compact and cost effective PFC solutions. While it requires a minimum number of external components, the MC33260 can control the follower boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered.

Also able to function in a traditional way (constant output voltage regulation level), any intermediary solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

General Features

- Standard Constant Output Voltage or “Follower Boost” Mode
- Switch Mode Operation: Voltage Mode
- Latching PWM for Cycle−by−Cycle On−Time Control
- Constant On−Time Operation That Saves the Use of an Extra Multiplier
- Totem Pole Output Gate Drive
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Improved Regulation Block Dynamic Behavior
- Synchronization Capability
- Internally Trimmed Reference Current Source
- These are Pb−Free Devices

Safety Features

- Overvoltage Protection: Output Overvoltage Detection
- Undervoltage Protection: Protection Against Open Loop
- Effective Zero Current Detection
- Accurate and Adjustable Maximum On−Time Limitation
- Overcurrent Protection
- ESD Protection on Each Pin

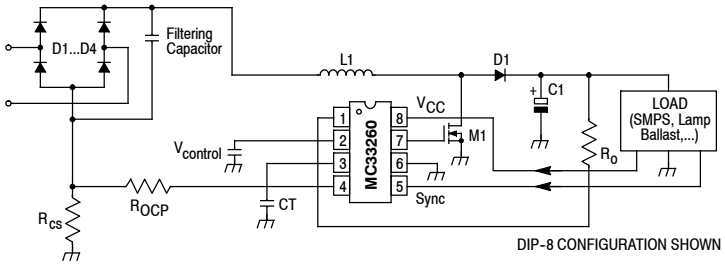

Figure 1. Typical Application

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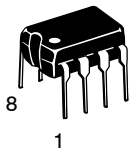
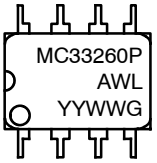
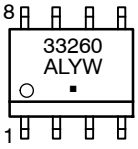
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626

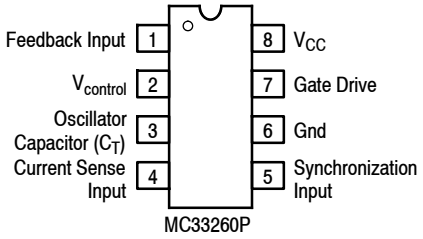


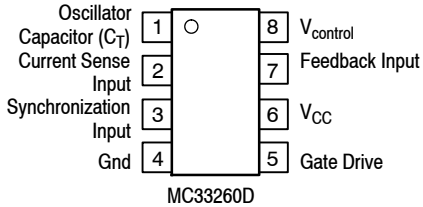
SO−8
D SUFFIX
CASE 751



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

PIN CONNECTIONS





ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

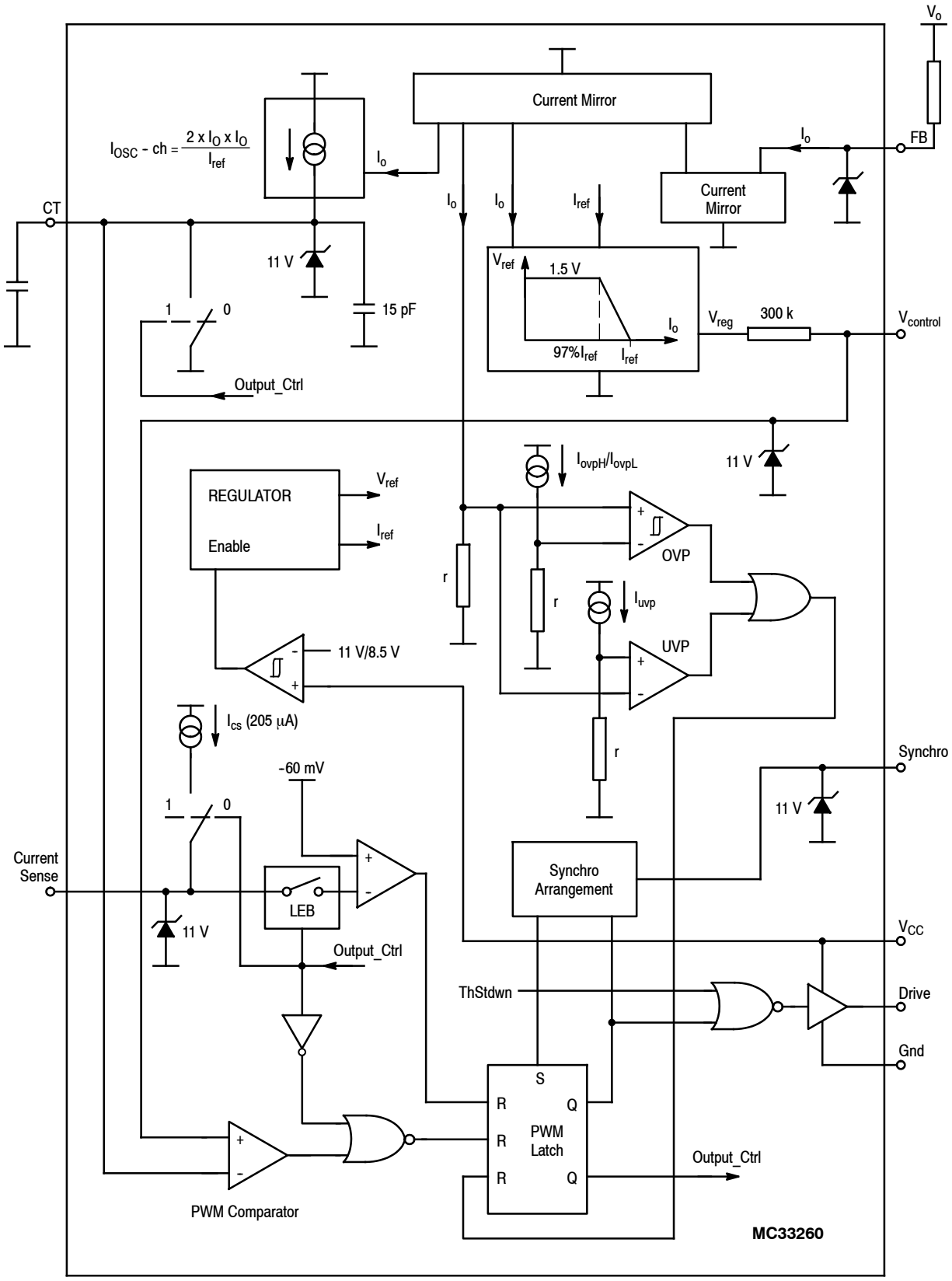


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Pin # PDIP-8	Pin # SO-8	Symbol	Value	Unit
Gate Drive Current* Source Sink	7	5	 $I_{O(Source)}$ $I_{O(Sink)}$	 -500 500	mA
V_{CC} Maximum Voltage	8	6	$(Vcc)_{max}$	16	V
Input Voltage			V_{in}	-0.3 to +10	V
Power Dissipation and Thermal Characteristics P Suffix, PDIP Package Maximum Power Dissipation @ T_A = 85°C Thermal Resistance Junction-to-Air			 P_D $R_{\theta JA}$	 600 100	 mW °C/W
Operating Junction Temperature			T_J	150	°C
Operating Ambient Temperature			T_A	-40 to +105	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V, T_J = 25°C for typical values, T_J = -40 to 105°C for min/max values unless otherwise noted.)

Characteristic	Pin # PDIP-8	Pin # SO-8	Symbol	Min	Typ	Max	Unit
GATE DRIVE SECTION							
Gate Drive Resistor Source Resistor @ I_{Drive} = 100 mA Sink Resistor @ I_{Drive} = 100 mA	7	5	 R_{OL} R_{OH}	 10 5	 20 10	 35 25	Ω
Gate Drive Voltage Rise Time (From 3.0 V Up to 9.0 V) (Note 1)	7	5	t_r	-	50	-	ns
Output Voltage Falling Time (From 9.0 V Down to 3.0 V) (Note 1)	7	5	t_f	-	50	-	ns
OSCILLATOR SECTION							
Maximum Oscillator Swing	3	1	ΔV_T	1.4	1.5	1.6	V
Charge Current @ I_{FB} = 100 μA	3	1	I_{charge}	87.5	100	112.5	μA
Charge Current @ I_{FB} = 200 μA	3	1	I_{charge}	350	400	450	μA
Ratio Multiplier Gain Over Maximum Swing @ I_{FB} = 100 μA	3	1	K_{osc}	5600	6400	7200	1/(V.A)
Ratio Multiplier Gain Over Maximum Swing @ I_{FB} = 200 μA	3	1	K_{osc}	5600	6400	7200	1/(V.A)
Average Internal Oscillator Pin Capacitance Over Oscillator Maximum Swing (C_T Voltage Varying From 0 Up to 1.5 V) (Note 2)	3	1	C_{int}	10	15	20	pF
Discharge Time (C_T = 1.0 nF)	3	1	T_{disch}	-	0.5	1.0	μs
REGULATION SECTION							
Regulation High Current Reference	1	7	I_{regH}	192	200	208	μA
Ratio (Regulation Low Current Reference) / I_{regH}	1	7	I_{regL}/I_{regH}	0.965	0.97	0.98	-
$V_{control}$ Impedance	1	7	$Z_{Vcontrol}$	-	300	-	kΩ

NOTE: I_{FB} is the current that is drawn by the Feedback Input Pin.
1. 1.0 nF being connected between the Pin 7 and ground for PDIP-8, between Pin 5 and ground for SO-8.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V, T_J = 25°C for typical values, T_J = −40 to 105°C for min/max values unless otherwise noted.)

Characteristic	Pin # PDIP−8	Pin # SO−8	Symbol	Min	Typ	Max	Unit
REGULATION SECTION (continued)							
Feedback Pin Clamp Voltage @ I_{FB} = 100 μA	1	7	V_{FB-100}	1.5	2.1	2.5	V
Feedback Pin Clamp Voltage @ I_{FB} = 200 μA	1	7	V_{FB-200}	2.0	2.6	3.0	V
CURRENT SENSE SECTION							
Zero Current Detection Comparator Threshold	4	2	V_{ZCD-th}	−90	−60	−30	mV
Negative Clamp Level (I_{CS-pin} = −1.0 mA)	4	2	Cl−neg	−	−0.7	−	V
Bias Current @ Vcs = V_{ZCD-th}	4	2	I_{b-cs}	−0.2	−	−	μA
Propagation Delay (Vcs > V_{ZCD-th}) to Gate Drive High	7	5	T_{ZCD}	−	500	−	ns
Current Sense Pin Internal Current Source	4	2	I_{OCP}	192	205	218	μA
Leading Edge Blanking Duration			τ_{LEB}	−	400	−	ns
OverCurrent Protection Propagation Delay (Vcs < V_{ZCD-th} to Gate Drive Low)	7	5	T_{OCP}	100	160	240	ns
SYNCHRONIZATION SECTION							
Synchronization Threshold PDIP−8 SO−8	 5 −	 − 3	 $V_{sync-th}$ $V_{sync-th}$	 0.8 0.8	 1.0 1.0	 1.2 1.4	 V V
Negative Clamp Level (I_{sync} = −1.0 mA)	5	3	Cl−neg	−	−0.7	−	V
Minimum Off−Time	7	5	T_{off}	1.5	2.1	2.7	μs
Minimum Required Synchronization Pulse Duration	5	3	T_{sync}	−	−	0.5	μs
OVERVOLTAGE PROTECTION SECTION							
OverVoltage Protection High Current Threshold and I_{regH} Difference	1	7	I_{OVPH}−I_{regH}	8.0	13	18	μA
OverVoltage Protection Low Current Threshold and I_{regH} Difference	1	7	I_{OVPL}−I_{regH}	0	−	−	−
Ratio (I_{OVPH}/I_{OVPL})	1	7	I_{OVPH} / I_{OVPL}	1.02	−	−	−
Propagation Delay (I_{FB} > 110% I_{ref} to Gate Drive Low)	7	5	T_{OVP}	−	500	−	ns
UNDERVOLTAGE PROTECTION SECTION							
Ratio (UnderVoltage Protection Current Threshold) / I_{regH}	1	7	I_{UVP}/I_{regH}	12	14	16	%
Propagation Delay (I_{FB} < 12% I_{ref} to Gate Drive Low)	7	5	T_{UVP}	−	500	−	ns
THERMAL SHUTDOWN SECTION							
Thermal Shutdown Threshold	7	5	T_{stdwn}	—	150	−	°C
Hysteresis	7	5	ΔT_{stdwn}	−	30	−	°C
V_{CC} UNDERVOLTAGE LOCKOUT SECTION							
Startup Threshold	8	6	$V_{stup-th}$	9.7	11	12.3	V
Disable Voltage After Threshold Turn−On	8	6	$V_{disable}$	7.4	8.5	9.6	V
TOTAL DEVICE							
Power Supply Current Startup (V_{CC} = 5 V with V_{CC} Increasing) Operating @ I_{FB} = 200 μA	8	6	I_{CC}	 − −	 0.1 4.0	 0.25 8.0	mA

NOTE: Vcs is the Current Sense Pin Voltage and I_{FB} is the Feedback Pin Current.

Pin Numbers are Relevant to the PDIP−8 Version

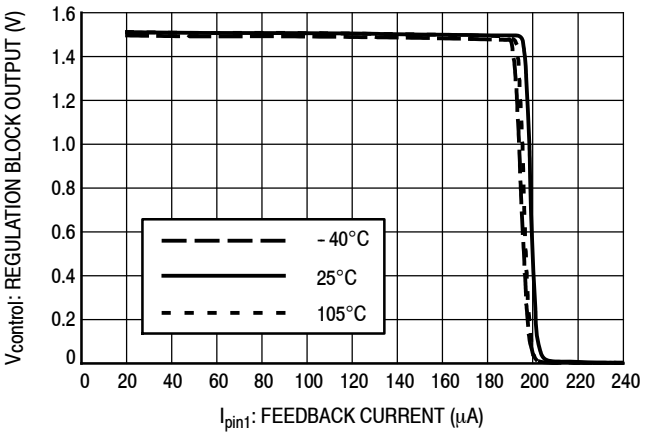


Figure 3. Regulation Block Output versus Feedback Current

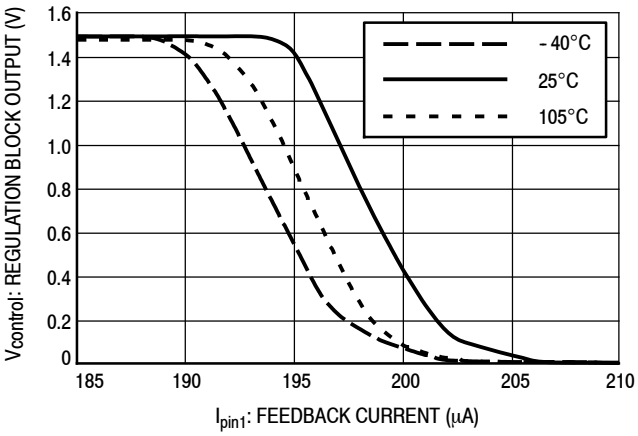


Figure 4. Regulation Block Output versus Feedback Current

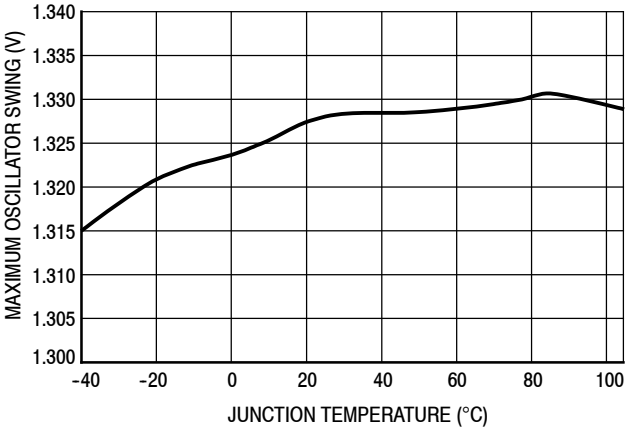


Figure 5. Maximum Oscillator Swing versus Temperature

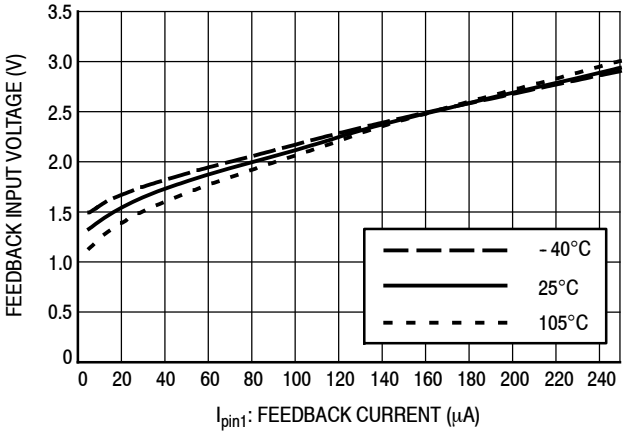


Figure 6. Feedback Input Voltage versus Feedback Current

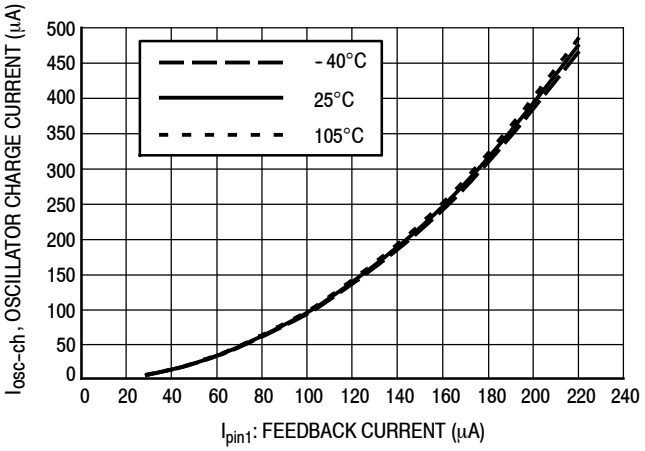


Figure 7. Oscillator Charge Current versus Feedback Current

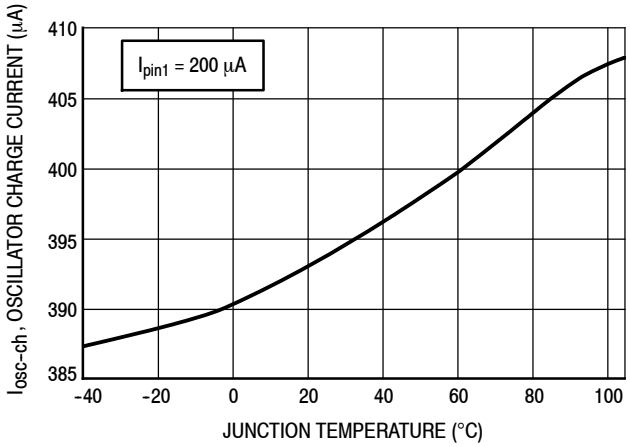


Figure 8. Oscillator Charge Current versus Temperature

Pin Numbers are Relevant to the PDIP−8 Version

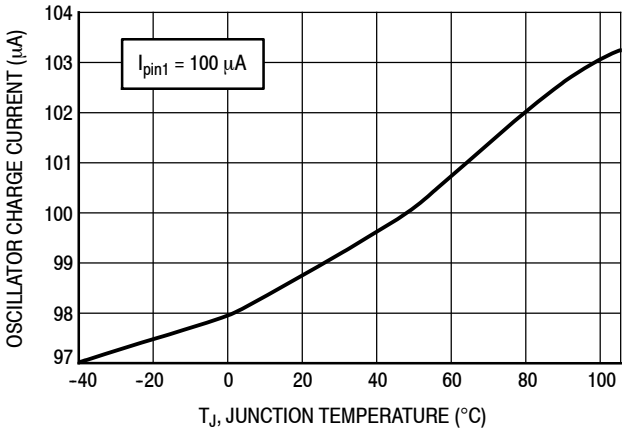


Figure 9. Oscillator Charge Current versus Temperature

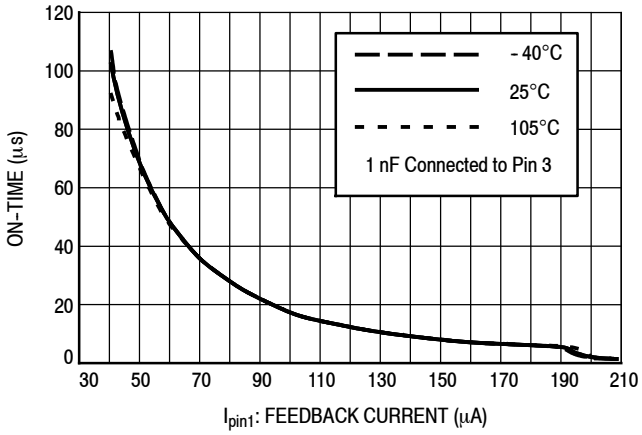


Figure 10. On−Time versus Feedback Current

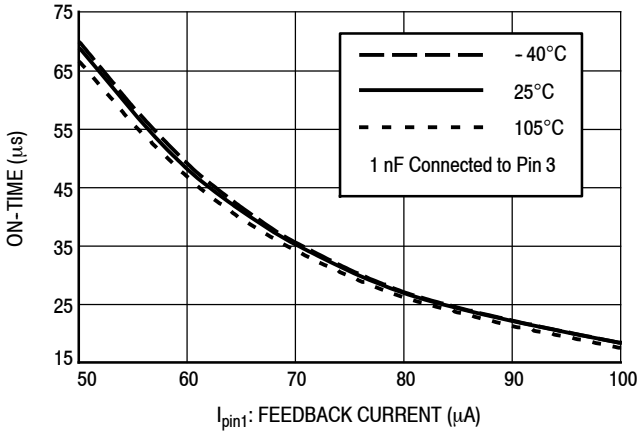


Figure 11. On−Time versus Feedback Current

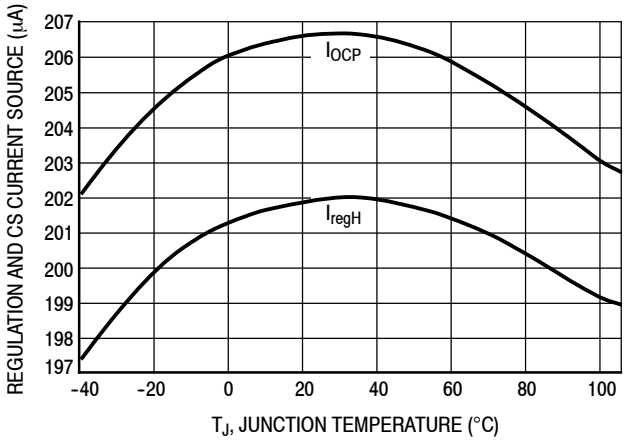


Figure 12. Internal Current Sources versus Temperature

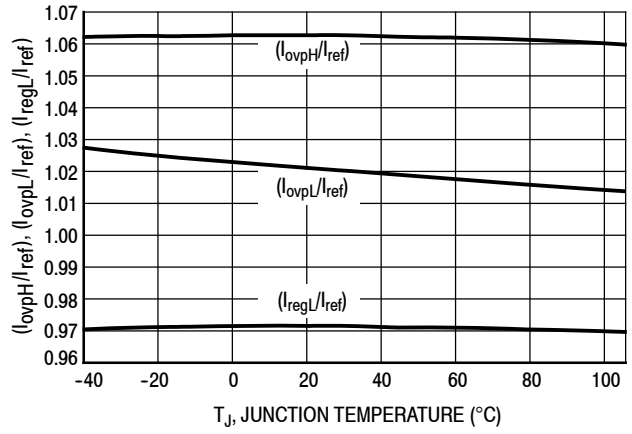


Figure 13. (I_{ovpH}/I_{ref}), (I_{ovpL}/I_{ref}), (I_{regL}/I_{ref}) versus Temperature

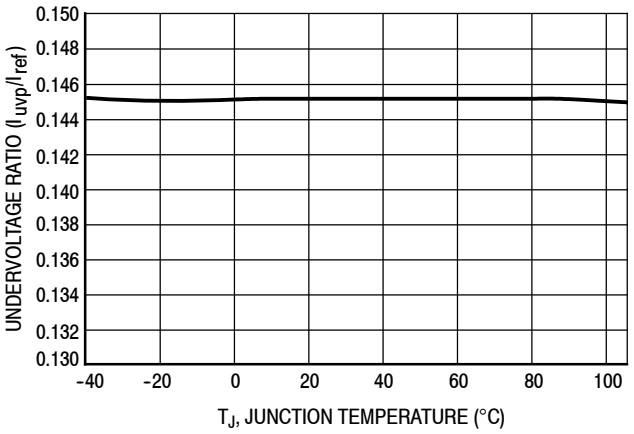


Figure 14. Undervoltage Ratio versus Temperature

Pin Numbers are Relevant to the PDIP−8 Version

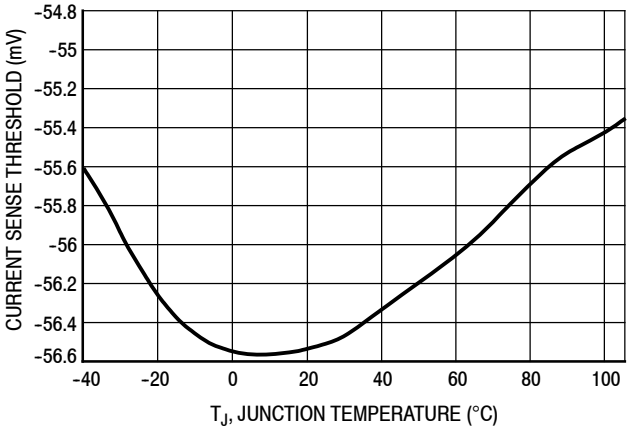


Figure 15. Current Sense Threshold versus Temperature

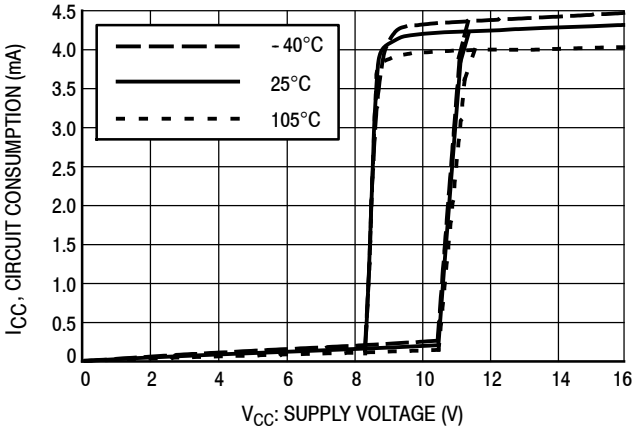


Figure 16. Circuit Consumption versus Supply Voltage

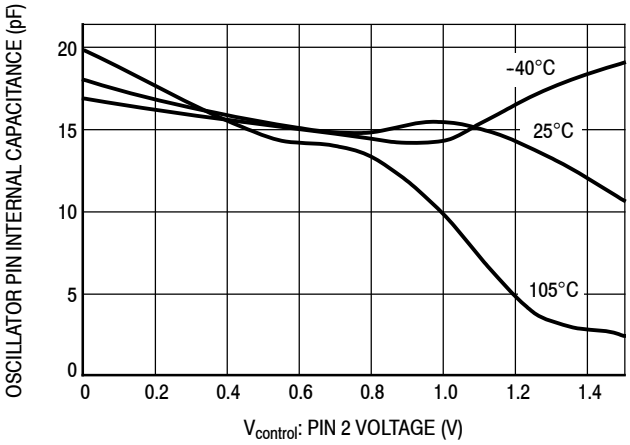


Figure 17. Oscillator Pin Internal Capacitance

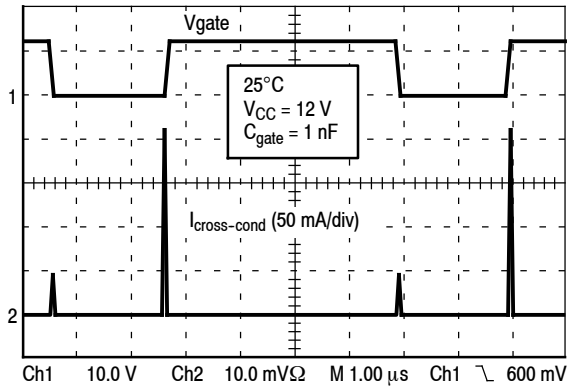


Figure 18. Gate Drive Cross Conduction

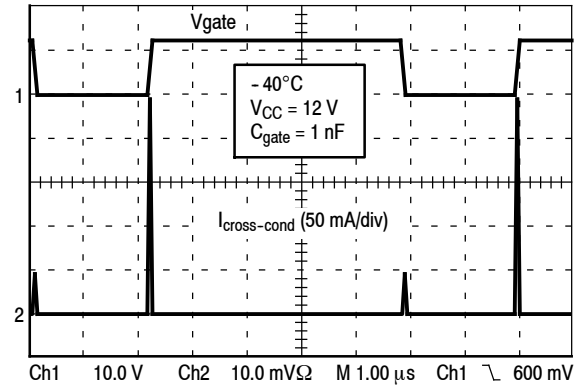


Figure 19. Gate Drive Cross Conduction

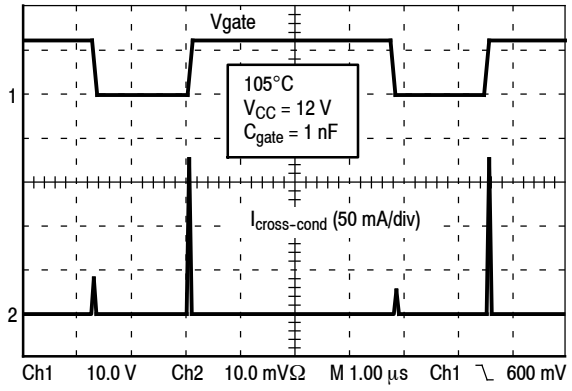


Figure 20. Gate Drive Cross Conduction

PIN FUNCTION DESCRIPTION

Pin # PDIP−8	Pin # SO−8	Function	Description
1	7	Feedback Input	This pin is designed to receive a current that is proportional to the preconverter output voltage. This information is used for both the regulation and the overvoltage and undervoltage protections. The current drawn by this pin is internally squared to be used as oscillator capacitor charge current.
2	8	$V_{control}$	This pin makes available the regulation block output. The capacitor connected between this pin and ground, adjusts the control bandwidth. It is typically set below 20 Hz to obtain a nondistorted input current.
3	1	Oscillator Capacitor (C_T)	The circuit uses an on−time control mode. This on−time is controlled by comparing the C_T voltage to the $V_{control}$ voltage. C_T is charged by the squared feedback current.
4	2	Zero Current Detection Input	This pin is designed to receive a negative voltage signal proportional to the current flowing through the inductor. This information is generally built using a sense resistor. The Zero Current Detection prevents any restart as long as the Pin 4 voltage is below (−60 mV). This pin is also used to perform the peak current limitation. The overcurrent threshold is programmed by the resistor connected between the pin and the external current sense resistor.
5	3	Synchronization Input	This pin is designed to receive a synchronization signal. For instance, it enables to synchronize the PFC preconverter to the associated SMPS. If not used, this pin must be grounded.
6	4	Ground	This pin must be connected to the preregulator ground.
7	5	Gate Drive	The gate drive current capability is suited to drive an IGBT or a power MOSFET.
8	6	V_{CC}	This pin is the positive supply of the IC. The circuit turns on when V_{CC} becomes higher than 11 V, the operating range after startup being 8.5 V up to 16 V.

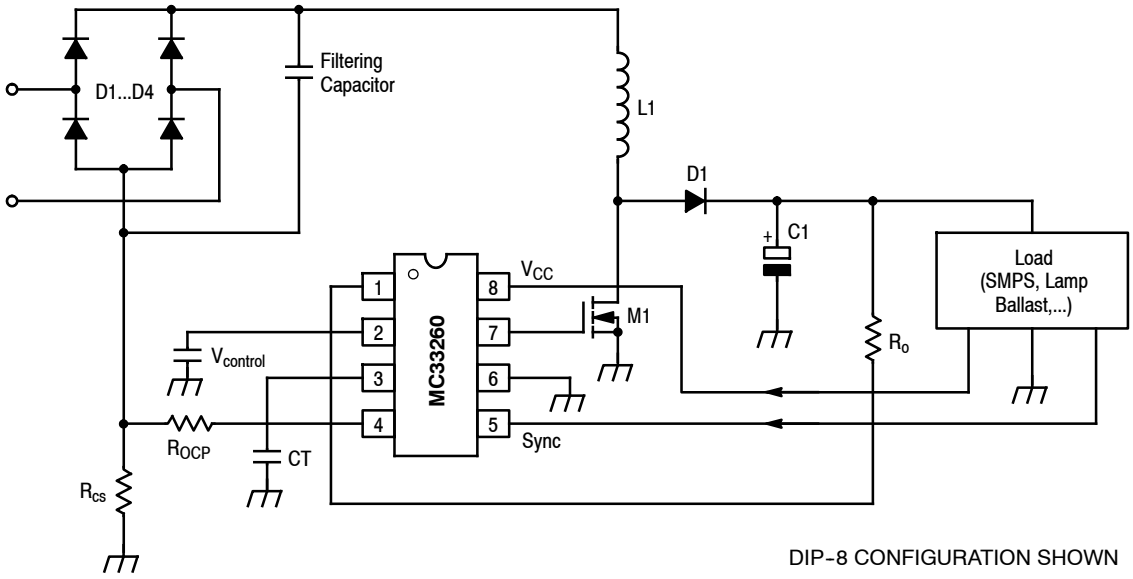


Figure 21. Application Schematic

FUNCTIONAL DESCRIPTION

Pin Numbers are Relevant to the PDIP−8 Version

INTRODUCTION

The need of meeting the requirements of legislation on line current harmonic content, results in an increasing demand for cost effective solutions to comply with the Power Factor regulations. This data sheet describes a monolithic controller specially designed for this purpose.

Most off−line appliances use a bridge rectifier associated to a huge bulk capacitor to derive raw dc voltage from the utility ac line.

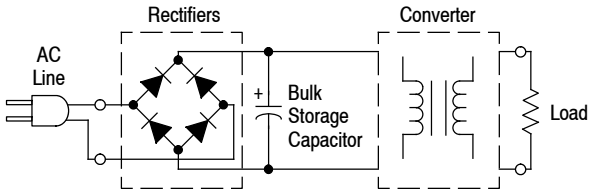


Figure 22. Typical Circuit Without PFC

This technique results in a high harmonic content and in poor power factor ratios. In effect, the simple rectification technique draws power from the mains when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike. Consequently, a poor power factor (in the range of 0.5 − 0.7) is generated, resulting in an apparent input power that is much higher than the real power.

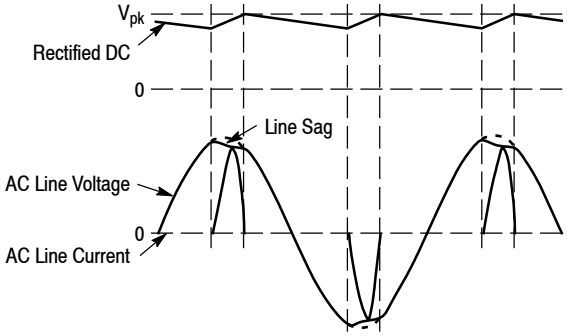


Figure 23. Line Waveforms Without PFC

Active solutions are the most popular way to meet the legislation requirements. They consist of inserting a PFC pre−regulator between the rectifier bridge and the bulk capacitor. This interface is, in fact, a step−up SMPS that outputs a constant voltage while drawing a sinusoidal current from the line.

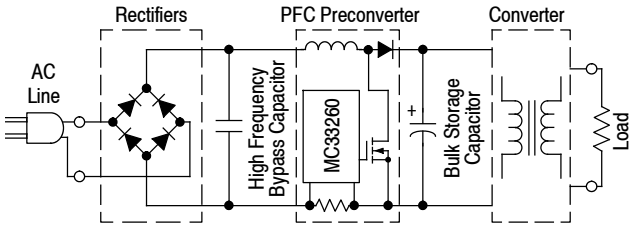


Figure 24. PFC Preconverter

The MC33260 was developed to control an active solution with the goal of increasing its robustness while lowering its global cost.

OPERATION DESCRIPTION

The MC33260 is optimized to just as well drive a free running as a synchronized discontinuous voltage mode.

It also features valuable protections (overvoltage and undervoltage protection, overcurrent limitation, ...) that make the PFC preregulator very safe and reliable while requiring very few external components. In particular, it is able to safely face any uncontrolled direct charges of the output capacitor from the mains which occur when the output voltage is lower than the input voltage (startup, overload, ...).

In addition to the low count of elements, the circuit can control an innovative mode named “Follower Boost” that permits to significantly reduce the size of the preconverter inductor and power MOSFET. With this technique, the output regulation level is not forced to a constant value, but can vary according to the a.c. line amplitude and to the power. The gap between the output voltage and the ac line is then lowered, what allows the preconverter inductor and power MOSFET size reduction. Finally, this method brings a significant cost reduction.

A description of the functional blocks is given below.

REGULATION SECTION

Connecting a resistor between the output voltage to be regulated and the Pin 1, a feedback current is obtained. Typically, this current is built by connecting a resistor between the output voltage and the Pin 1. Its value is then given by the following equation:

$$I_{pin1} = \frac{V_o - V_{pin1}}{R_o}$$

where:

R_o is the feedback resistor,

V_o is the output voltage,

V_{pin1} is the Pin 1 clamp value.

The feedback current is compared to the reference current so that the regulation block outputs a signal following the characteristic depicted in Figure 25. According to the power and the input voltage, the output voltage regulation level varies between two values $(V_o)_{regL}$ and $(V_o)_{regH}$ corresponding to the I_{regL} and I_{regH} levels.

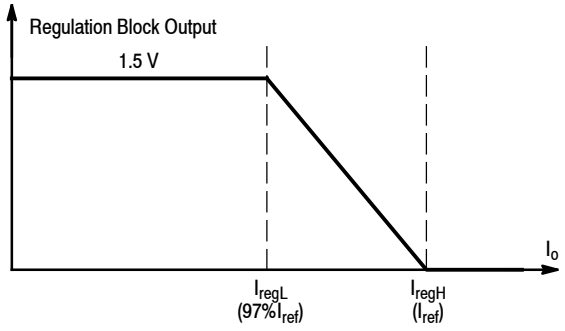


Figure 25. Regulation Characteristic

The feedback resistor must be chosen so that the feedback current should equal the internal current source I_{regH} when the output voltage exceeds the chosen upper regulation voltage $[(V_o)_{regH}]$.

Pin Numbers are Relevant to the PDIP−8 Version

Consequently:

$$R_o = \frac{(V_o)_{regH} - V_{pin1}}{I_{regH}}$$

In practice, V_{pin1} is small compared to $(V_o)_{regH}$ and this equation can be simplified as follows (I_{regH} being also replaced by its typical value 200 μA):

$$R_o \approx 5 \times (V_o)_{regH}\ (k\Omega)$$

The regulation block output is connected to the Pin 2 through a 300 kΩ resistor. The Pin 2 voltage ($V_{control}$) is compared to the oscillator sawtooth for PWM control.

An external capacitor must be connected between Pin 2 and ground, for external loop compensation. The bandwidth is typically set below 20 Hz so that the regulation block output should be relatively constant over a given ac line cycle. This integration that results in a constant on−time over the ac line period, prevents the mains frequency output ripple from distorting the ac line current.

OSCILLATOR SECTION

The oscillator consists of three phases:

- Charge Phase: The oscillator capacitor voltage grows up linearly from its bottom value (ground) until it exceeds $V_{control}$ (regulation block output voltage). At that moment, the PWM latch output gets low and the oscillator discharge sequence is set.
- Discharge Phase: The oscillator capacitor is abruptly discharged down to its valley value (0 V).
- Waiting Phase: At the end of the discharge sequence, the oscillator voltage is maintained in a low state until the PWM latch is set again.

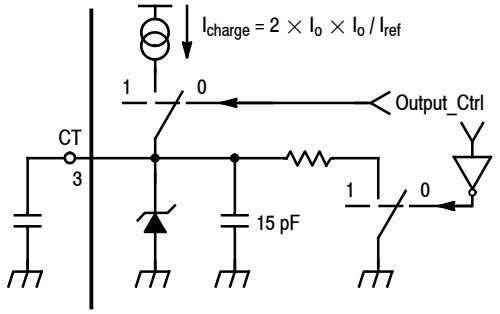


Figure 26. Oscillator

The oscillator charge current is dependent on the feedback current (I_o). In effect

$$I_{charge} = 2 \times \frac{I_o^2}{I_{ref}}$$

where:

I_{charge} is the oscillator charge current,
I_o is the feedback current (drawn by Pin 1),
I_{ref} is the internal reference current (200 μA).

So, the oscillator charge current is linked to the output voltage level as follows:

$$I_{charge} = \frac{2 \times \left(V_o - V_{pin1}\right)^2}{R_o^2 \times I_{ref}}$$

where:

V_o is the output voltage,
R_o is the feedback resistor,
V_{pin1} is the Pin 1 clamp voltage.

In practice, V_{pin1} that is in the range of 2.5 V, is very small compared to V_o. The equation can then be simplified by neglecting V_{pin1}:

$$I_{charge} \approx \frac{2 \times V_o^2}{R_o^2 \times I_{ref}}$$

It must be noticed that the oscillator terminal (Pin 3) has an internal capacitance (C_{int}) that varies versus the Pin 3 voltage. Over the oscillator swing, its average value typically equals 15 pF (min 10 pF, max 20 pF).

The total oscillator capacitor is then the sum of the internal and external capacitors.

$$C_{pin3} = C_T + C_{int}$$

PWM LATCH SECTION

The MC33260 operates in voltage mode: the regulation block output ($V_{control}$ − Pin 2 voltage) is compared to the oscillator sawtooth so that the gate drive signal (Pin 7) is high until the oscillator ramp exceeds $V_{control}$.

The on−time is then given by the following equation:

$$t_{on} = \frac{C_{pin3} \times V_{control}}{I_{ch}}$$

where:

t_{on} is the on−time,
C_{pin3} is the total oscillator capacitor (sum of the internal and external capacitor),
I_{charge} is the oscillator charge current (Pin 3 current),
$V_{control}$ is the Pin 2 voltage (regulation block output).

Consequently, replacing I_{charge} by the expression given in the **Oscillator Section**:

$$t_{on} = \frac{R_o^2 \times I_{ref} \times C_{pin3} \times V_{control}}{2 \times V_o^2}$$

One can notice that the on−time depends on V_o (preconverter output voltage) and that the on−time is maximum when Vcontrol is maximum (1.5 V typically).

At a given V_o, the maximum on−time is then expressed by the following equation:

$$(t_{on})max = \frac{C_{pin3} \times R_o^2 \times I_{ref} \times \left(V_{control}\right)_{max}}{2 \times V_o^2}$$

This equation can be simplified replacing

$$\left\{\frac{2}{[(V_{control})\ max * I_{ref}]}\right\} \text{ by } K_{osc}$$

Refer to **Electrical Characteristics, Oscillator Section**. Then:

$$(t_{on})\ max = \frac{C_{pin3} \times R_o^2}{K_{osc} \times V_o^2}$$

Pin Numbers are Relevant to the PDIP-8 Version

This equation shows that the maximum on-time is inversely proportional to the squared output voltage. This property is used for follower boost operation (refer to **Follower Boost** section).

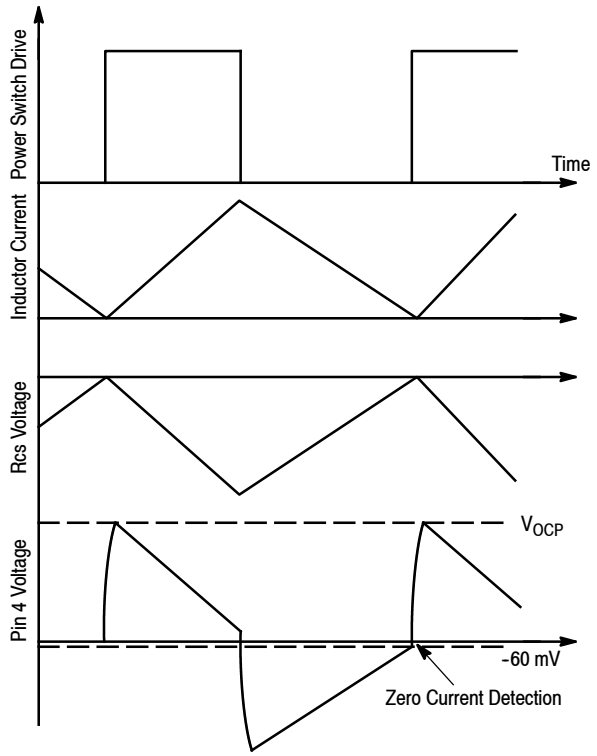
CURRENT SENSE BLOCK

The inductor current is converted into a voltage by inserting a ground referenced resistor (R_{cs}) in series with the input diodes bridge (and the input filtering capacitor). Therefore a negative voltage proportional to the inductor current is built:

$$V_{cs} = -\left(R_{cs} \times I_L\right)$$

where:

I_L is the inductor current,
R_{cs} is the current sense resistor,
V_{cs} is the measured R_{cs} voltage.



$V_{OCP} = R_{OCP} \times I_{OCP}$
An overcurrent is detected if V_{pin4} crosses the threshold (-60 mV) during the Power Switch on state

Figure 27. Current Sensing

The negative signal V_{cs} is applied to the current sense through a resistor R_{OCP}. The pin is internally protected by a negative clamp (-0.7 V) that prevents substrate injection.

As long as the Pin 4 voltage is lower than (-60 mV), the Current Sense comparator resets the PWM latch to force the gate drive signal low state. In that condition, the power MOSFET cannot be on.

During the on-time, the Pin 4 information is used for the overcurrent limitation while it serves the zero current detection during the off time.

Zero Current Detection

The Zero Current Detection function guarantees that the MOSFET cannot turn on as long as the inductor current hasn't reached zero (discontinuous mode).

The Pin 4 voltage is simply compared to the (-60 mV) threshold so that as long as V_{cs} is lower than this threshold, the circuit gate drive signal is kept in low state. Consequently, no power MOSFET turn on is possible until the inductor current is measured as smaller than ($60\,mV/R_{cs}$) that is, the inductor current nearly equals zero.

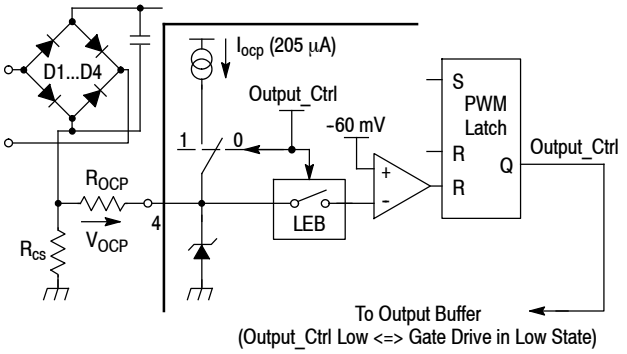


Figure 28. Current Sense Block

Overcurrent Protection

During the power switch conduction (i.e. when the Gate Drive Pin voltage is high), a current source is applied to the Pin 4. A voltage drop V_{OCP} is then generated across the resistor R_{OCP} that is connected between the sense resistor and the Current Sense Pin (refer to Figure 28). So, instead of V_{cs}, the sum ($V_{cs} + V_{OCP}$) is compared to (-60 mV) and the maximum permissible current is the solution of the following equation:

$$-\left(R_{cs} \times Ipk_{max}\right) + V_{OCP} = -60\ mV$$

where:

Ipk_{max} is maximum allowed current,
R_{cs} is the sensing resistor.

The overcurrent threshold is then:

$$Ipk_{max} = \frac{\left(R_{OCP} \times I_{OCP}\right) + 60 \times 10^{-3}}{R_{cs}}$$

where:

R_{OCP} is the resistor connected between the pin and the sensing resistor (R_{cs}),
I_{OCP} is the current supplied by the Current Sense Pin when the gate drive signal is high (power switch conduction phase). I_{OCP} equals 205 μA typically.

Practically, the V_{OCP} offset is high compared to 60 mV and the precedent equation can be simplified. The maximum current is then given by the following equation:

$$Ipk_{max} \approx \frac{R_{OCP}(k\Omega)}{R_{cs}(\Omega)} \times 0.205\ (A)$$

Consequently, the R_{OCP} resistor can program the OCP level whatever the R_{cs} value is. This gives a high freedom in the choice of R_{cs}. In particular, the inrush resistor can be utilized.

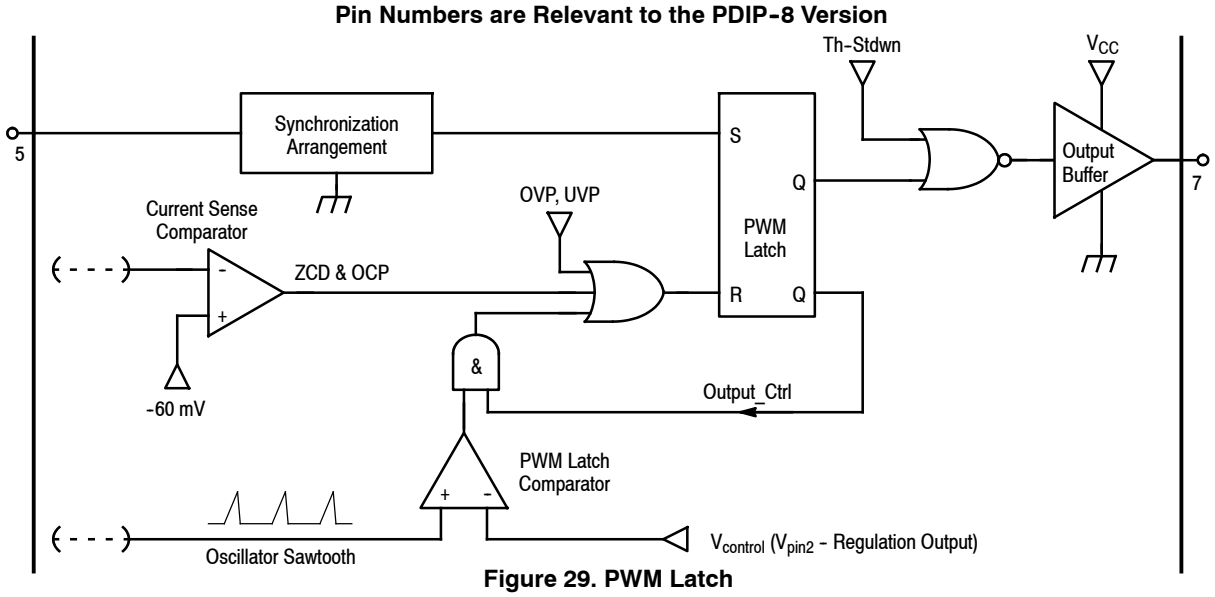


Figure 29. PWM Latch

A LEB (Leading Edge Blanking) has been implemented. This circuitry disconnects the Current Sense comparator from Pin 4 and disables it during the 400 first ns of the power switch conduction. This prevents the block from reacting on the current spikes that generally occur at power switch turn on. Consequently, proper operation does not require any filtering capacitor on Pin 4.

PROTECTIONS

OCP (Overcurrent Protection)

Refer to **Current Sense Block**.

OVP (Overvoltage Protection)

The feedback current (I_o) is compared to a threshold current (I_{ovpH}). If it exceeds this value, the gate drive signal is maintained low until this current gets lower than a second level (I_{ovpL}).

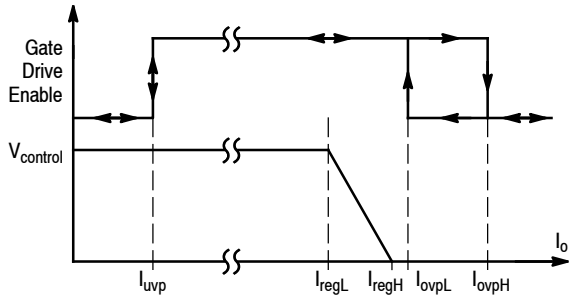


Figure 30. Internal Current Thresholds

So, the OVP upper threshold is:

$$V_{ovpH} = V_{pin1} + \left(R_o \times I_{ovpH}\right)$$

where:

R_o is the feedback resistor that is connected between Pin 1 and the output voltage,

I_{ovpH} is the internal upper OVP current threshold,

V_{pin1} is the Pin 1 clamp voltage.

Practically, V_{pin1} that is in the range of 2.5 V, can be neglected. The equation can then be simplified:

$$V_{ovpH} = R_o(M\Omega) \times I_{ovpH}(\mu A)\ (V)$$

On the other hand, the OVP low threshold is:

$$V_{ovpL} = V_{pin1} + \left(R_o \times I_{ovpL}\right)$$

where I_{ovpL} is the internal low OVP current threshold. Consequently, V_{pin1} being neglected:

$$V_{ovpL} = R_o(M\Omega) \times I_{ovpL}(\mu A)\ (V)$$

The OVP hysteresis prevents erratic behavior.

I_{ovpL} is guaranteed to be higher than IregH (refer to parameters specification). This ensures that the OVP function doesn't interfere with the regulation one.

UVP (Undervoltage Protection)

This function detects when the feedback current is lower than 14% of I_{ref}. In this case, the PWM latch is reset and the power switch is kept off.

This protection is useful to:

- Protect the preregulator from working in too low mains conditions.
- To detect the feedback current absence (in case of a nonproper connection for instance).

The UVP threshold is:

$$V_{uvp} \approx V_{pin1} + \left(R_o(M\Omega) \times I_{uvp}(\mu A)\right)\ (V)$$

Practically (V_{pin1} being neglected),

$$V_{uvp} = R_o(M\Omega) \times I_{uvp}(\mu A)\ (V)$$

Maximum On−Time Limitation

As explained in **PWM Latch**, the maximum on−time is accurately controlled.

Pin Protection

All the pins are ESD protected.

Pin Numbers are Relevant to the PDIP−8 Version

In particular, a 11 V Zener diode is internally connected between the terminal and ground on the following pins: Feedback, $V_{control}$, Oscillator, Current Sense, and Synchronization.

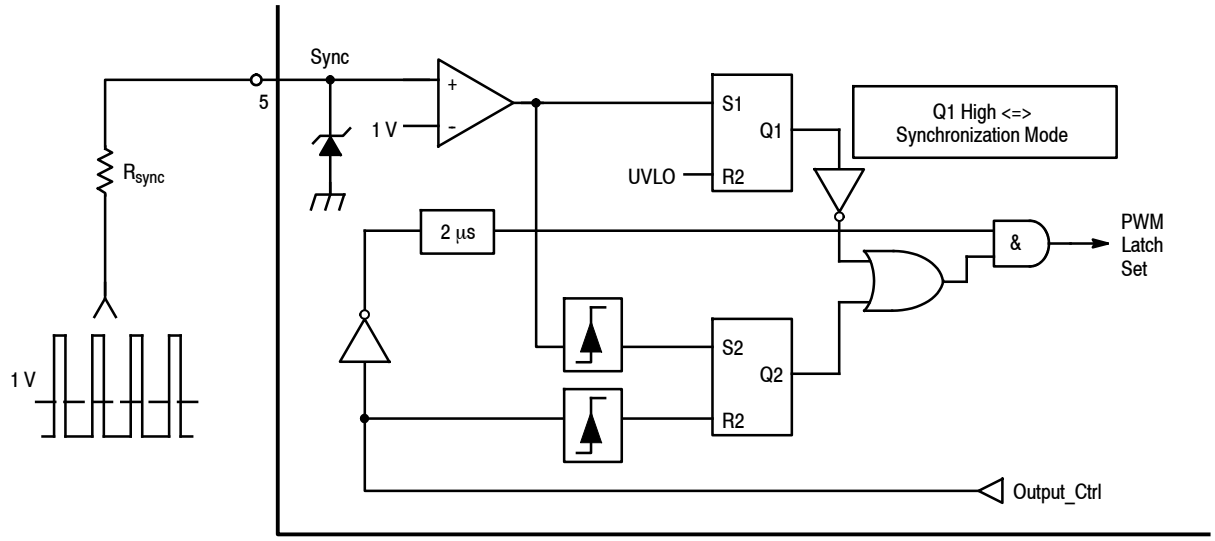


Figure 31. Synchronization Arrangement

SYNCHRONIZATION BLOCK

The MC33260 features two modes of operation:

- Free Running Discontinuous Mode: The power switch is turned on as soon as there is no current left in the inductor (Zero Current Detection). This mode is simply obtained by grounding the synchronization terminal (Pin 5).
- Synchronization Mode: This mode is set as soon as a signal crossing the 1.0 V threshold, is applied to the Pin 5. In this case, operation in free running can only be recovered after a new circuit startup. In this mode, the power switch cannot turn on before the two following conditions are fulfilled.

- Still, the zero current must have been detected.
- The precedent turn on must have been followed by (at least) one synchronization raising edge crossing the 1.0 V threshold.

In other words, the synchronization acts to prolong the power switch off time.

Consequently, a proper synchronized operation requires that the current cycle (on−time + inductor demagnetization) is shorter than the synchronization period. Practically, the inductor must be chosen accordingly. Otherwise, the system will keep working in free running discontinuous mode. Figure 36 illustrates this behavior.

It must be noticed that whatever the mode is, a 2.0 μs minimum off−time is forced. This delay limits the switching frequency in light load conditions.

OUTPUT SECTION

The output stage contains a totem pole optimized to minimize the cross conduction current during high speed operation. The gate drive is kept in a sinking mode whenever the Undervoltage Lockout is active. The rise and fall times have been controlled to typically equal 50 ns while loaded by 1.0 nF.

REFERENCE SECTION

An internal reference current source (I_{ref}) is trimmed to be ±4% accurate over the temperature range (the typical value is 200 μA). I_{ref} is the reference used for the regulation ($I_{regH} = I_{ref}$).

UNDERVOLTAGE LOCKOUT SECTION

An Undervoltage Lockout comparator has been implemented to guarantee that the integrated circuit is operating only if its supply voltage (V_{CC}) is high enough to enable a proper working. The UVLO comparator monitors the Pin 8 voltage and when it exceeds 11 V, the device gets active. To prevent erratic operation as the threshold is crossed, 2.5 V of hysteresis is provided.

The circuit off state consumption is very low: in the range of 100 μA @ V_{CC} = 5.0 V. This consumption varies versus V_{CC} as the circuit presents a resistive load in this mode.

THERMAL SHUTDOWN

An internal thermal circuitry is provided to disable the circuit gate drive and then to prevent it from oscillating, if the junction temperature exceeds 150°C typically.

The output stage is again enabled when the temperature drops below 120°C typically (30°C hysteresis).

Pin Numbers are Relevant to the PDIP−8 Version

FOLLOWER BOOST

Traditional PFC preconverters provide the load with a fixed and regulated voltage that generally equals 230 V or 400 V according to the mains type (U.S., European, or universal).

In the "Follower Boost" operation, the preconverter output regulation level is not fixed but varies linearly versus the ac line amplitude at a given input power.

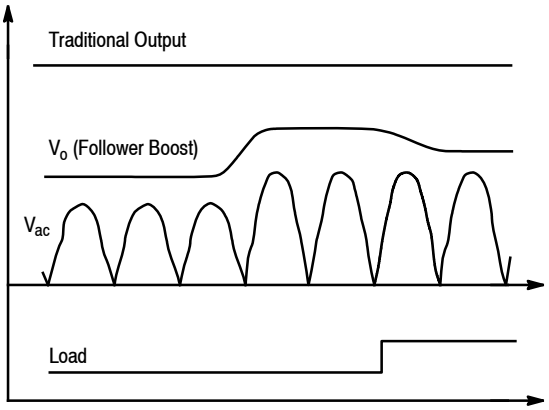


Figure 32. Follower Boost Characteristics

This technique aims at reducing the gap between the output and the input voltages to minimize the boost efficiency degradation.

Follower Boost Benefits

The boost presents two phases:

- The on−time during which the power switch is on. The inductor current grows up linearly according to a slope (V_{in}/L_p), where V_{in} is the instantaneous input voltage and L_p the inductor value.
- The off−time during which the power switch is off. The inductor current decreases linearly according the slope (V_o − V_{in})/L_p, where V_o is the output voltage. This sequence that terminates when the current equals zero, has a duration that is inversely proportional to the gap between the output and input voltages. Consequently, the off−time duration becomes longer in follower boost.

Consequently, for a given peak inductor current, the longer the off time, the smaller power switch duty cycle and then its conduction dissipation. This is the first benefit of this technique: the MOSFET on−time losses are reduced.

The increase of the off time duration also results in a switching frequency diminution (for a given inductor value). Given that in practise, the boost inductor is selected big enough to limit the switching frequency down to an acceptable level, one can immediately see the second benefit of the follower boost: it allows the use of smaller, lighter and cheaper inductors compared to traditional systems.

Finally, this technique utilization brings a drastic system cost reduction by lowering the size and then the cost of both the inductor and the power switch.

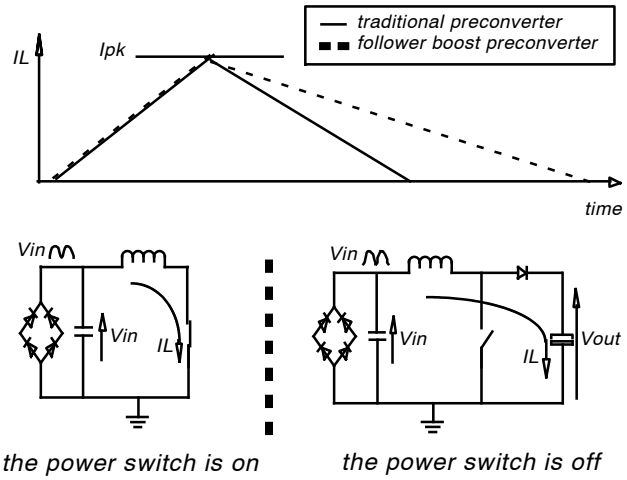


Figure 33. Off−Time Duration Increase

Follower Boost Implementation

In the MC33260, the on−time is differently controlled according to the feedback current level. Two areas can be defined:

- When the feedback current is higher than I_{regL} (refer to regulation section), the regulation block output ($V_{control}$) is modulated to force the output voltage to a desired value.
- On the other hand, when the feedback current is lower than I_{regL}, the regulation block output and therefore, the on−time are maximum. As explained in **PWM Latch Section,** the on−time is then inversely proportional to the output voltage square. The Follower Boost is active in these conditions in which the on−time is simply limited by the output voltage level. Note: In this equation, the Feedback Pin voltage (V_{pin1}) is neglected compared to the output voltage (refer to the **PWM Latch Section).**

$$t_{on} = (t_{on})max = \frac{C_{pin3} \times R_o^2}{K_{osc} \times V_o^2}$$

where:

C_{pin3} is the total oscillator capacitor (sum of the internal and external capacitors − C_{int} + C_T),
K_{osc} is the ratio (oscillator swing over oscillator gain),
V_o is the output voltage,
R_o is the feedback resistor.

Pin Numbers are Relevant to the PDIP−8 Version

On the other hand, the boost topology has its own rule that dictates the on−time necessary to deliver the required power:

$$t_{on} = \frac{4 \times L_p \times P_{in}}{V_{pk}^2}$$

where:

V_{pk} is the peak ac line voltage,
L_p is the inductor value,
P_{in} is the input power.

Combining the two equations, one can obtain the Follower Boost equation:

$$V_o = \frac{R_o}{2} \times \sqrt{\frac{C_{pin3}}{K_{osc} \times L_p \times P_{in}}} \times V_{pk}$$

Consequently, a linear dependency links the output voltage to the ac line amplitude at a given input power.

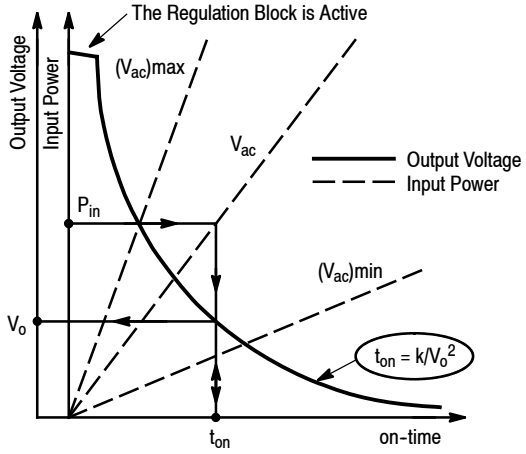


Figure 34. Follower Boost Characteristics

The behavior of the output voltage is depicted in Figures 34 and 35. In particular, Figure 35 illustrates how the output voltage converges to a stable equilibrium level. First, at a given ac line voltage, the on−time is dictated by the power demand. Then, the follower boost characteristic makes correspond one output voltage level to this on−time. Combining these two laws, it appears that the power level forces the output voltage.

One can notice that the system is fully stable:

- If an output voltage increase makes it move away from its equilibrium value, the on−time will immediately diminish according to the follower boost law. This will result in a delivered power decrease. Consequently, the supplied power being too low, the output voltage will decrease back,
- In the same way, if the output voltage decreases, more power will be transferred and then the output voltage will increase back.

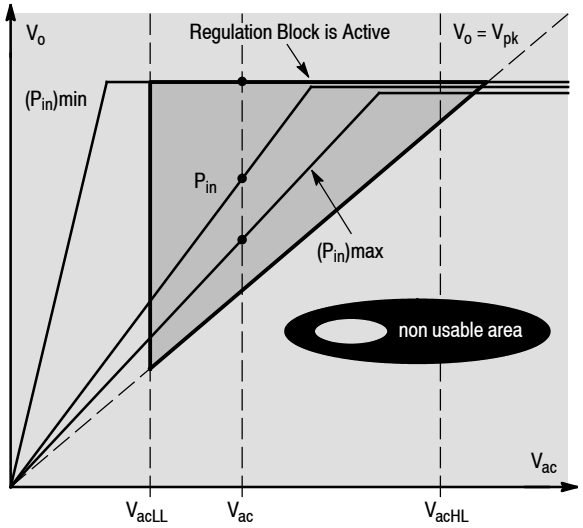


Figure 35. Follower Boost Output Voltage

Mode Selection

The operation mode is simply selected by adjusting the oscillator capacitor value. As shown in Figure 35, the output voltage first has an increasing linear characteristic versus the ac line magnitude and then is clamped down to the regulation value. In the traditional mode, the linear area must be rejected. This is achieved by dimensioning the oscillator capacitor so that the boost can deliver the maximum power while the output voltage equals its regulation level and this, whatever the given input voltage. Practically, that means that whatever the power and input voltage conditions are, the follower boost would generate output voltages values higher than the regulation level, if there was no regulation block.

In other words, if $(V_o)_{regL}$ is the low output regulation level:

$$(V_o)_{regL} \leq \frac{R_o}{2} \times \sqrt{\frac{C_T + C_{int}}{K_{osc} \times L_p \times (P_{in})max}} \times V_{pk}$$

Consequently,

$$C_T \geq -C_{int} + \frac{4 \times K_{osc} \times L_p \times (P_{in})max \times (V_o)_{regL}^2}{R_o^2 \times V_{pk}^2}$$

Using I_{regL} (regulation block current reference), this equation can be simplified as follows:

$$C_T \geq -C_{int} + \frac{4 \times K_{osc} \times L_p \times (P_{in})max \times I_{regL}^2}{V_{pk}^2}$$

In the Follower Boost case, the oscillator capacitor must be chosen so that the wished characteristics are obtained.

Consequently, the simple choice of the oscillator capacitor enables the mode selection.

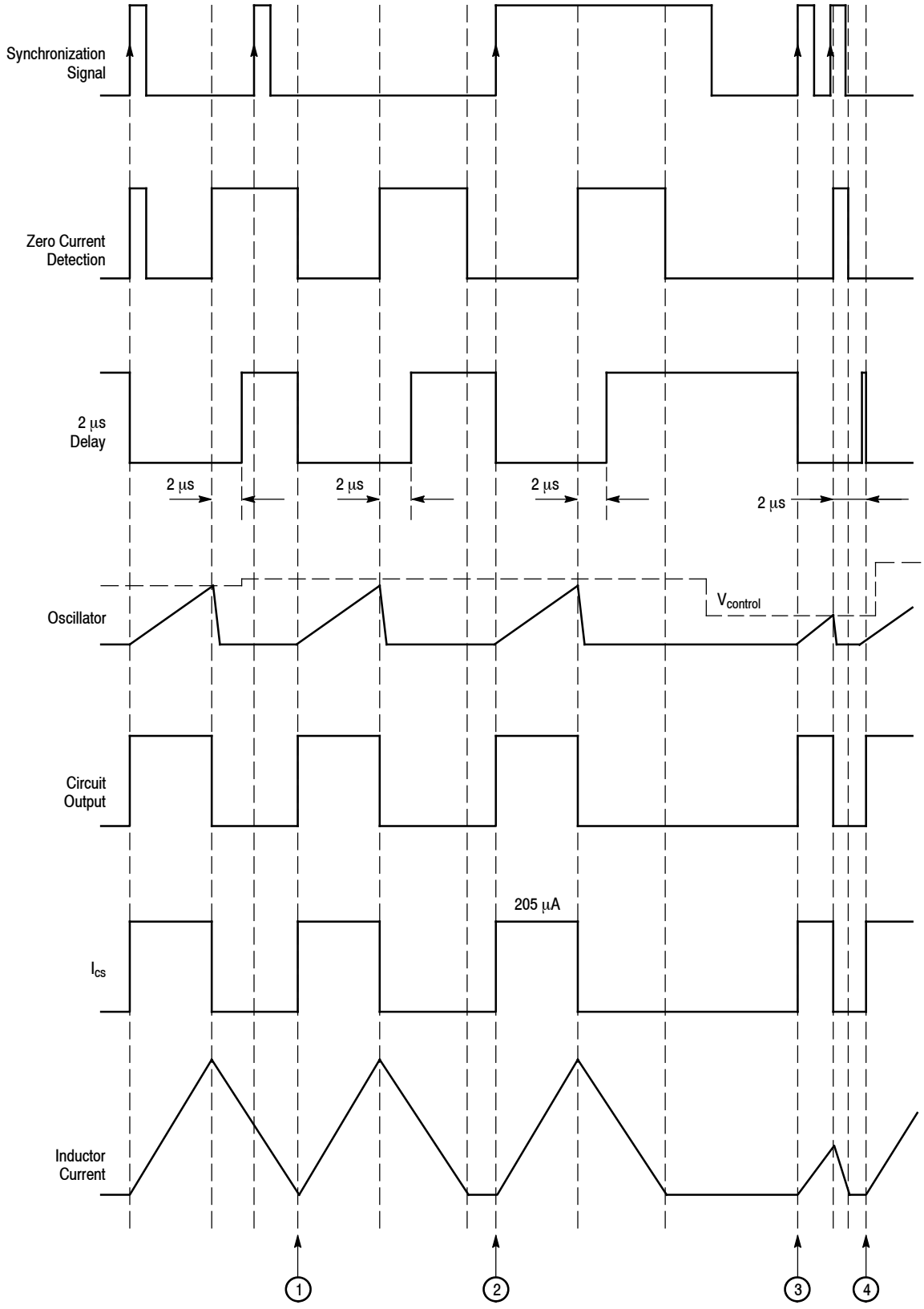
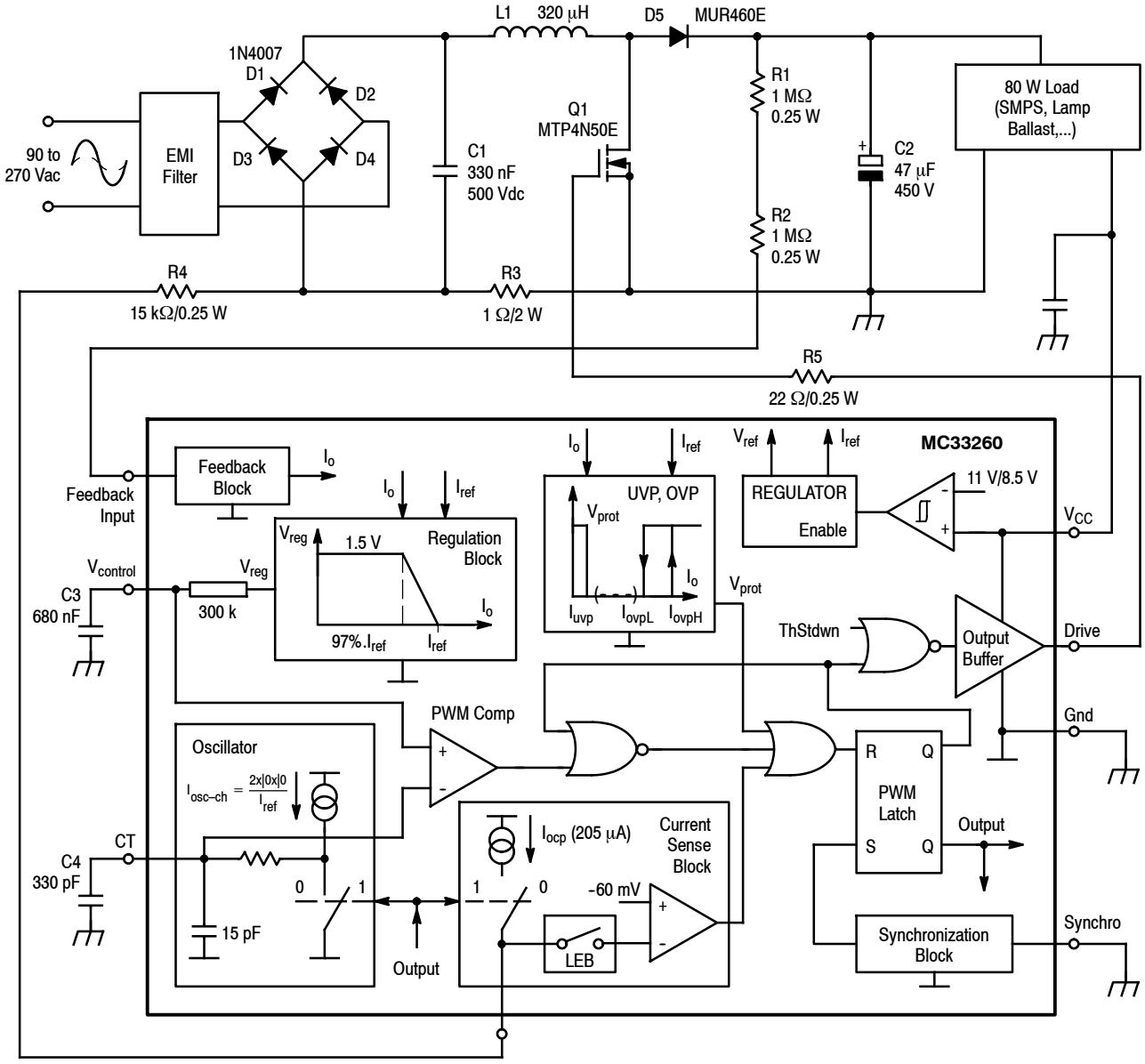


Figure 36. Typical Waveforms

MAIN DESIGN EQUATIONS (Note 3)

rms Input Current (I_{ac}) $$I_{ac} = \frac{P_o}{\eta \times V_{ac}}$$	η (preconverter efficiency) is generally in the range of 90 - 95%.
Maximum Inductor Peak Current ((I_{pk})max): $$(I_{pk})\,max = \frac{2 \times \sqrt{2} \times (P_o)\,max}{\eta \times V_{acLL}}$$	(I_{pk})max is the maximum inductor current.
Output Voltage Peak to Peak 100Hz (120Hz) Ripple ((ΔVo)pk-pk): $$(\Delta V_o)_{pk-pk} = \frac{P_o}{2\pi \times f_{ac} \times C_o \times V_o}$$	f_{ac} is the ac line frequency (50 or 60Hz).
Inductor Value (L_p): $$L_p = \frac{2 \times t \times \left(\frac{V_o}{\sqrt{2}} - V_{acLL}\right) \times V_{acLL}^{\,2}}{V_o \times V_{acLL} \times (I_{pk})\,max}$$	t is the maximum switching period. (t = 40 μs) for universal mains operation and (t = 20 μs) for narrow range are generally used.
Maximum Power MOSFET Conduction Losses ((p_{on})max): $$(P_{on})\,max \approx \frac{1}{3} \times (Rds)on \times (I_{pk})\,max^2 \times \left[1 - \frac{1.2 \times V_{acLL}}{V_o}\right]$$	(Rds)on is the MOSFET drain source on-time resistor. In Follower Boost, the ratio (V_{acLL}/V_o) is higher. The on-time MOSFET losses are then reduced.
Maximum Average Diode Current (I_d): $$(I_d)\,max = \frac{(P_o)\,max}{(V_o)\,min}$$	The Average Diode Current depends on the power and on the output voltage.
Current Sense Resistor Losses (pR_{cs}): $$pR_{cs} = \frac{1}{6} \times (Rds)on \times (I_{pk})^2\,max$$	This formula indicates the required dissipation capability for R_{cs} (current sense resistor).
Over Current Protection Resistor (R_{OCP}): $$R_{OCP} \approx \frac{R_{cs} \times (I_{pk})\,max}{0.205} \quad (k\Omega)$$	The overcurrent threshold is adjusted by R_{OCP} at a given R_{cs}. R_{cs} can be a preconverter inrush resistor.
Oscillator External Capacitor Value (C_T): -Traditional Operation $$C_T \geq -C_{int} + \frac{2 \times K_{osc} \times L_p \times (P_{in})\,max \times I_{regL}^2}{V_{ac}^2}$$ - Follower Boost: $$V_o = \frac{R_o}{2} \times \sqrt{\frac{C_T + C_{int}}{K_{osc} \times L_p \times P_{in}}} \times V_{pk}$$	The Follower Boost characteristic is adjusted by the C_T choice. The Traditional Mode is also selected by C_T. C_{int} is the oscillator pin internal capacitor.
Feedback Resistor (R_o): $$R_o = \frac{(V_o)_{reg} - V_{FB}}{I_{regH}} \approx \frac{V_o}{200} \quad (M\Omega)$$	The output voltage regulation level is adjusted by R_o.

3. The preconverter design requires the following characteristics specification:
   - $(V_o)_{reg}$: desired output voltage regulation level
   - $(\Delta V_o)_{pk-pk}$: admissible output peak to peak ripple voltage
   - P_o: desired output power
   - V_{ac}: ac rms operating line voltage
   - V_{acLL}: minimum ac rms operating line voltage
   - V_{FB}: Feedback Pin voltage



L1: Coilcraft N2881 – A (primary: 62 turns of # 22 AWG – Secondary: 5 turns of # 22 AWG Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance (Lp) of 320 μH)

Figure 37. 80 W Wide Mains Power Factor Corrector

POWER FACTOR CONTROLLER TEST DATA*

AC Line Input										DC Output				
				Current Harmonic Distortion (% I_{fund})										
V_{rms} (V)	P_{in} (W)	PF (-)	I_{fund} (mA)	THD	H2	H3	H5	H7	H9	V_o (V)	ΔV_o (V)	I_o (mA)	P_o (W)	η (%)
90	88.2	0.991	990	8.1	0.07	5.9	4.3	1.5	1.7	181	31.2	440	79.6	90.2
110	86.3	0.996	782	7.0	0.05	2.7	5.7	1.1	0.8	222	26.4	360	79.9	92.6
135	85.2	0.995	642	8.2	0.03	1.5	6.8	1.1	1.5	265	20.8	300	79.5	93.3
180	87.0	0.994	480	9.5	0.16	4.0	6.5	3.1	4.0	360	16.0	225	81.0	93.1
220	84.7	0.982	385	15	0.5	8.4	7.8	5.3	1.9	379	14.0	210	79.6	94.4
240	85.3	0.975	359	16.5	0.7	9.0	7.8	7.4	3.8	384	14.0	210	80.6	94.5
260	84.0	0.967	330	18.8	0.7	11.0	7.0	9.0	4.0	392	13.2	205	80.4	95.7

*Measurements performed using Voltech PM1200 ac power analysis.

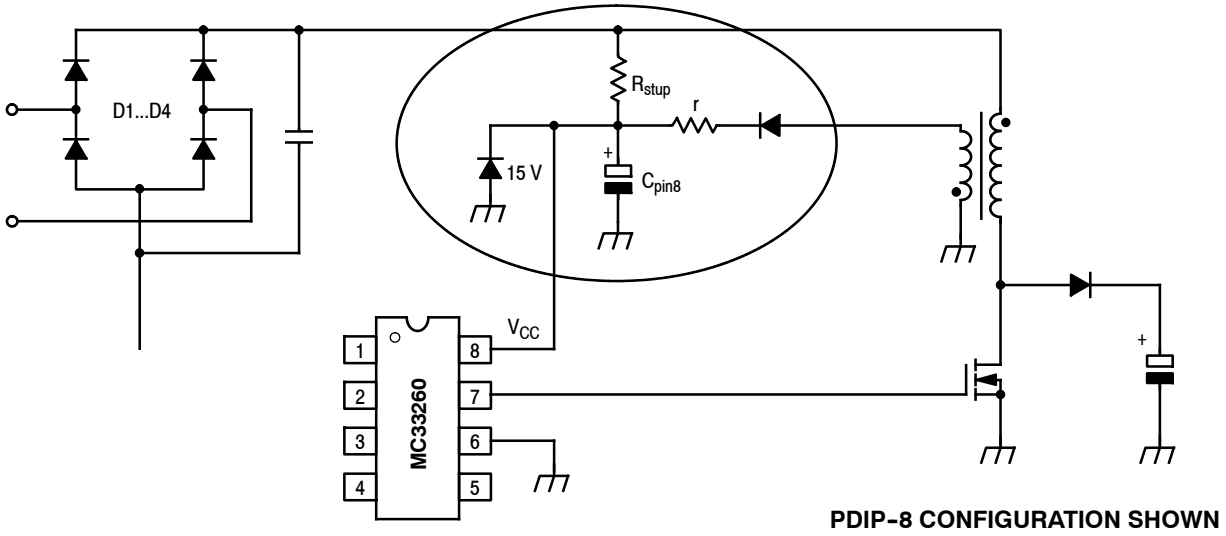


Figure 38. Circuit Supply Voltage

MC33260 V_{CC} SUPPLY VOLTAGE

In some applications, the arrangement shown in Figure 38 must be implemented to supply the circuit. A startup resistor is connected between the rectified voltage (or one−half wave) to charge the MC33260 V_{CC} up to its startup threshold (11 V typically). The MC33260 turns on and the V_{CC} capacitor (C_{pin8}) starts to be charged by the PFC transformer auxiliary winding. A resistor, r (in the range of 22 Ω) and a 15 V Zener should be added to protect the circuit from excessive voltages.

When the PFC preconverter is loaded by an SMPS, the MC33260 should preferably be supplied by the SMPS itself. In this configuration, the SMPS starts first and the PFC gets active when the MC33260 V_{CC} supplied by the power supply, exceeds the device startup level. With this configuration, the PFC preconverter doesn't require any auxiliary winding and finally a simple coil can be used.

PCB LAYOUT

The connections of the oscillator and $V_{control}$ capacitors should be as short as possible.

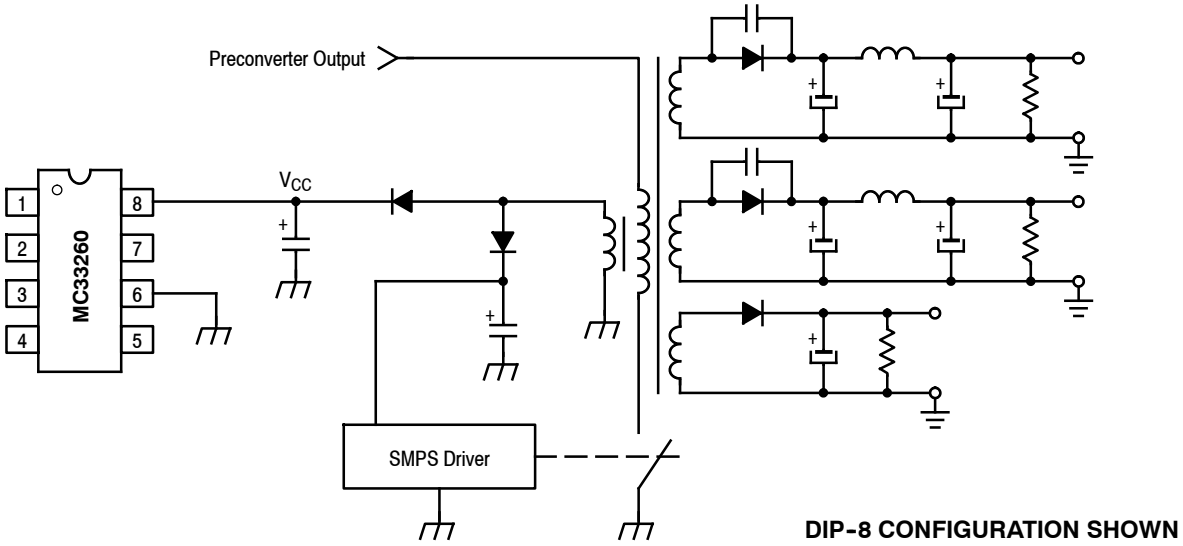


Figure 39. Preconverter Loaded by a Flyback SMPS: MC33260 V_{CC} Supply

ORDERING INFORMATION

Device	Package	Shipping†
MC33260PG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33260DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33260DR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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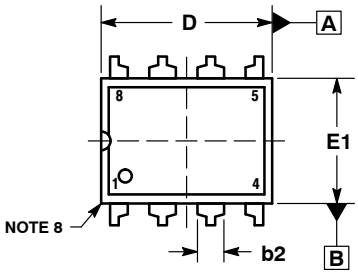
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

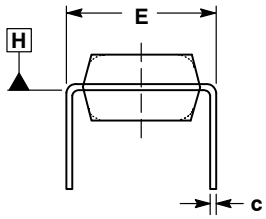
PDIP–8
CASE 626–05
ISSUE P

DATE 22 APR 2015

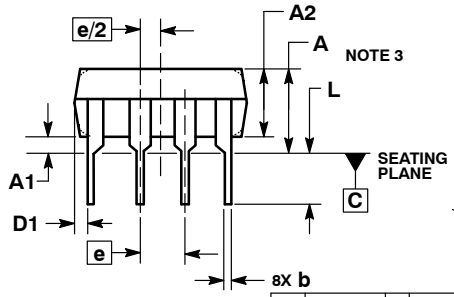
SCALE 1:1



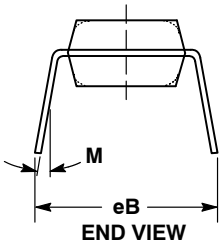
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



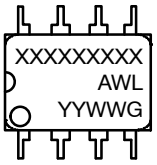
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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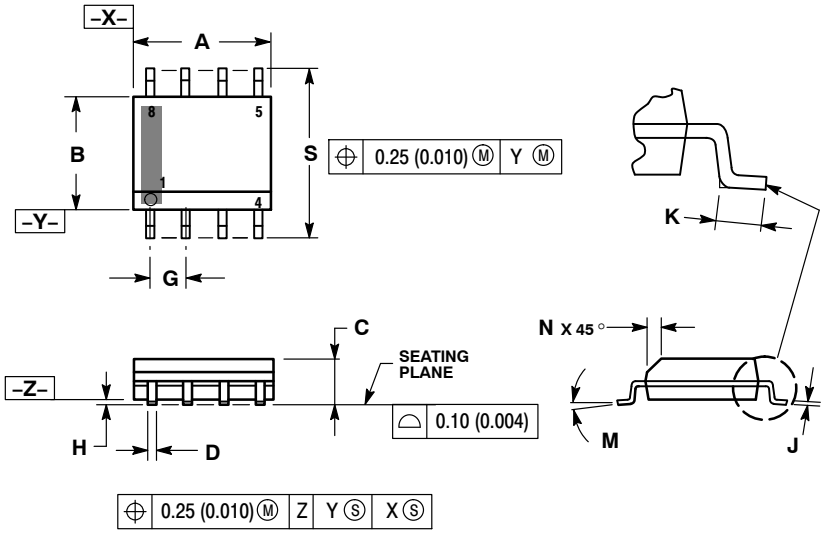
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

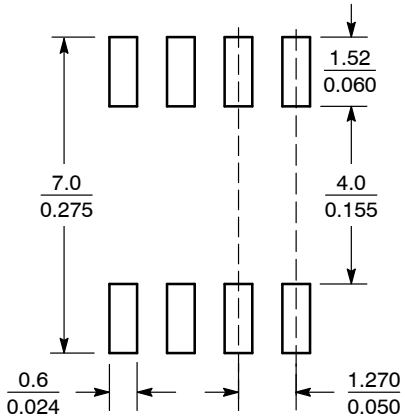
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

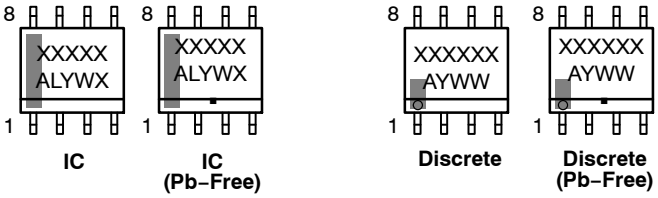
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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