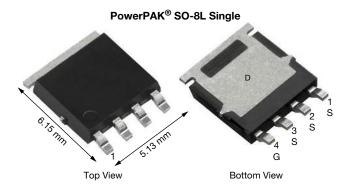
### SQJA78EP

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**Vishay Siliconix** 

# Automotive N-Channel 80 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	80
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0053
I <sub>D</sub> (A)	72
Configuration	Single
Package	PowerPAK SO-8L

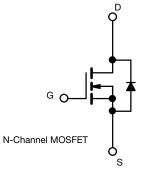
#### FEATURES

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



HALOGEN

FREE



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> :	= 25 °C, unles	s otherwise noted	)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	80	v	
Gate-source voltage		V <sub>GS</sub>	± 20	V	
Continuous drain current	T <sub>C</sub> = 25 °C	1	72		
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	41.5		
Continuous source current (diode conduction)		۱ <sub>S</sub>	62	А	
Pulsed drain current <sup>a</sup>	I <sub>DM</sub>	288			
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	37		
Single pulse avalanche energy		E <sub>AS</sub>	68.4	mJ	
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	PD	68	w	
Maximum power dissipation -	$T_{\rm C} = 125 ^{\circ}{\rm C}$ 22	vv			
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>c, d</sup>			260	C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	R <sub>thJA</sub>	68	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	2.2	0/10

Notes

b. When mounted on 1" square PCB (FR4 material)

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

1

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2  $\,\%$ 

c. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection





PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0, I_D = 250 \ \mu A$		80	-	-	v
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	2.3	2.8	3.3	v
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 80 V	-	-	1	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 175 °C	-	-	500	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	30	-	-	Α
		$V_{GS} = 10 V$	I <sub>D</sub> = 10 A	-	0.00432	0.00530	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	I <sub>D</sub> = 10 A, T <sub>J</sub> = 125 °C	-	-	0.00970	Ω
		$V_{GS} = 10 V$	I <sub>D</sub> = 10 A, T <sub>J</sub> = 175 °C	-	-	0.01210	
Forward transconductance b	g <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 10 A	-	51	-	S
Dynamic <sup>b</sup>				•		•	
Input capacitance	C <sub>iss</sub>			-	3767	5100	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 V$ , f = 1 MHz	-	700	950	pF
Reverse transfer capacitance	C <sub>rss</sub>			-	45	65	
Total gate charge <sup>c</sup>	Qg			-	62	95	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 40 \text{ V}, I_{D} = 10 \text{ A}$	-	16	-	nC
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	13	-	
Gate resistance	Rg	f = 1 MHz		0.25	0.52	0.80	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	16	30	
Rise time <sup>c</sup>	tr	$V_{DD}$ = 40 V, R <sub>L</sub> = 4 $\Omega$ I <sub>D</sub> $\cong$ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 $\Omega$		-	5	10	ns
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	29	50	
Fall time <sup>c</sup>	t <sub>f</sub>			-	7	15	
Source-Drain Diode Ratings and Charac	cteristics <sup>b</sup>			•		•	
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	288	Α
Forward voltage	V <sub>SD</sub>	$I_{\rm F} = 10$ A, $V_{\rm GS} = 0$		-	0.8	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>			-	51	110	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 8 A, di/dt = 100 A/μs		-	87	180	nC
Reverse recovery fall time	t <sub>a</sub>			-	39	-	
Reverse recovery rise time	t <sub>b</sub>			-	12	-	ns
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-3	-	Α

#### Notes

a. Pulse test; pulse width  $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

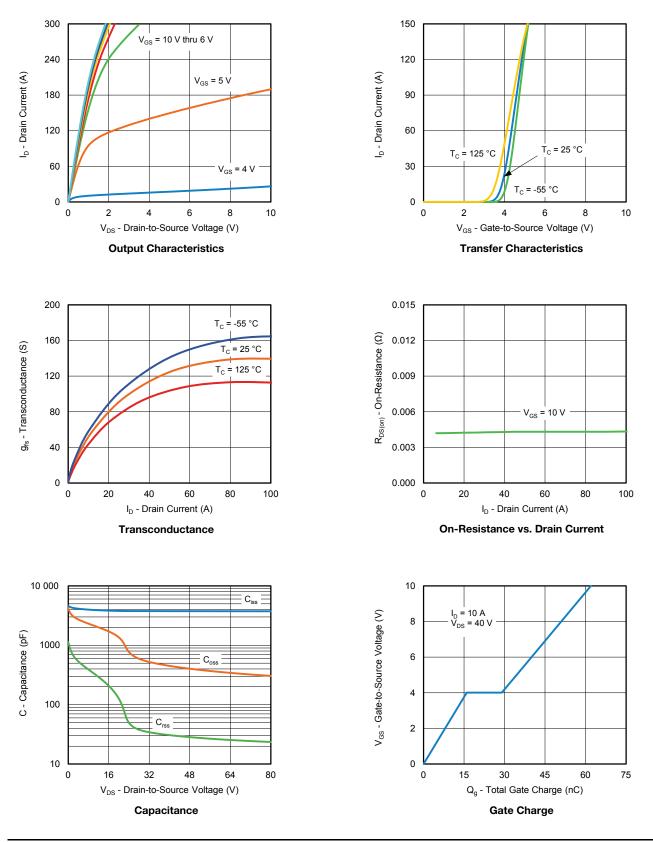
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2



### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



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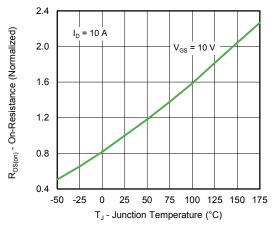
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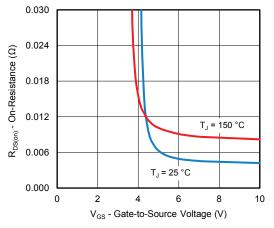
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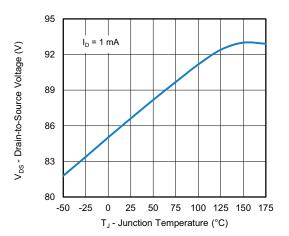
### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



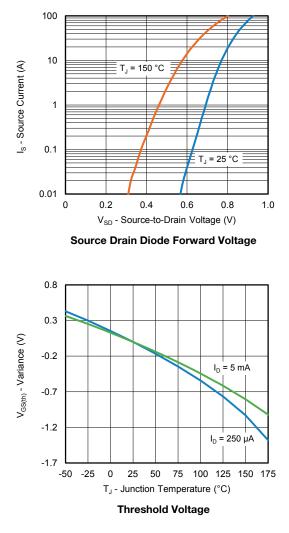
**On-Resistance vs. Junction Temperature** 

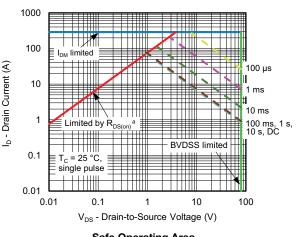


**On-Resistance vs. Gate-to Source Voltage** 

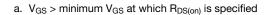


Drain Source Breakdown vs. Junction Temperature





Safe Operating Area



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Note

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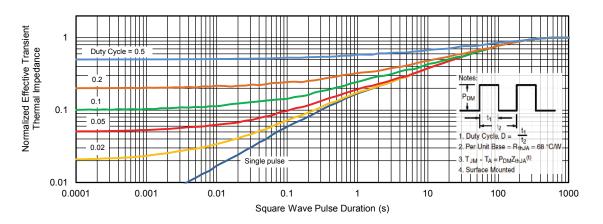
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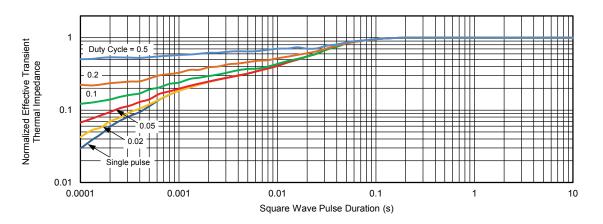
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### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

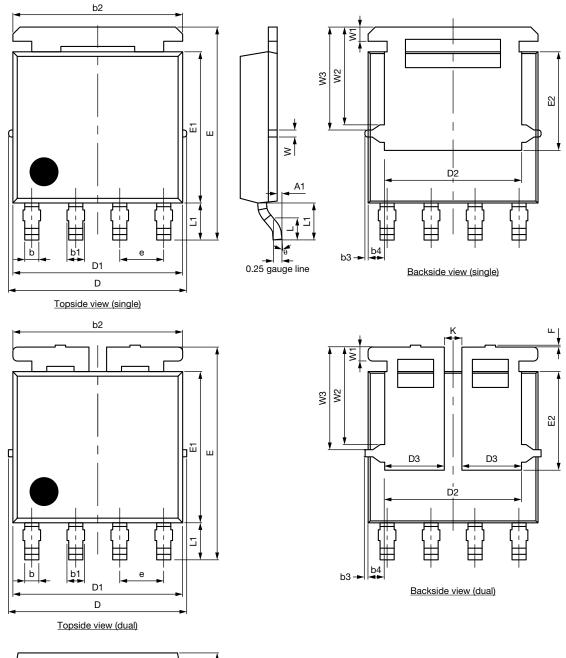
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

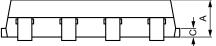
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1 For technical questions, contact: <u>pmostechsupport@vishay.com</u>

# **Package Information**



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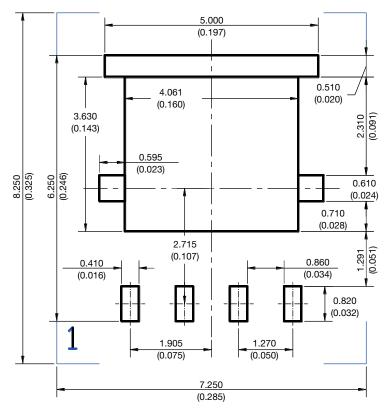
DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094			0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC		0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
К		0.51			0.020		
W	0.23			0.009			
W1	0.41			0.016			
W2	2.82			0.111			
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

Note

• Millimeters will govern



### RECOMMENDED MINIMUM PAD FOR PowerPAK<sup>®</sup> SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)

Revision: 07-Feb-12



Vishay

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