

HVD191

Silicon Epitaxial Planar Pin Diode for High Frequency Attenuator

REJ03G0015-0200
Rev.2.00
Jan 20, 2006

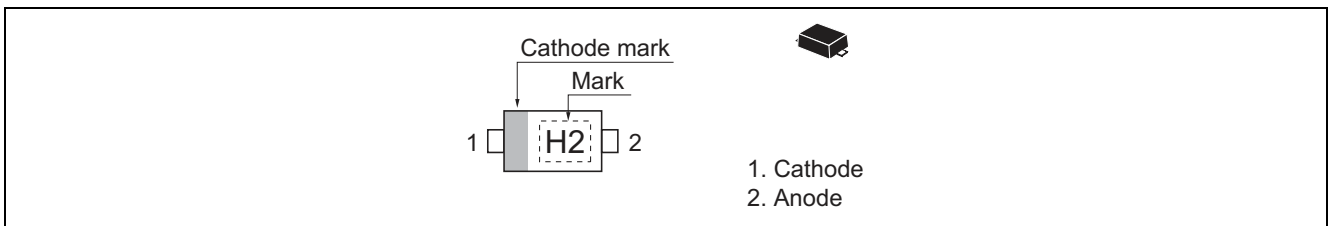
Features

- Low capacitance. ($C = 0.37 \text{ pF max}$)
- Low forward resistance. ($r_f = 2.5 \Omega \text{ max}$)
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code
HVD191	H2	SFP	PUSF0002ZB-A

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Reverse voltage	V_R	30	V
Forward current	I_F	100	mA
Power dissipation	P_d	150	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Forward voltage	V_F	—	—	1.0	V	$I_F = 10 \text{ mA}$
Reverse current	I_R	—	—	100	nA	$V_R = 30 \text{ V}$
Capacitance	C	—	—	0.37	pF	$V_R = 1 \text{ V}, f = 1 \text{ MHz}$
Forward resistance	r_f	—	—	2.5	Ω	$I_F = 10 \text{ mA}, f = 100 \text{ MHz}$

Note: For SFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

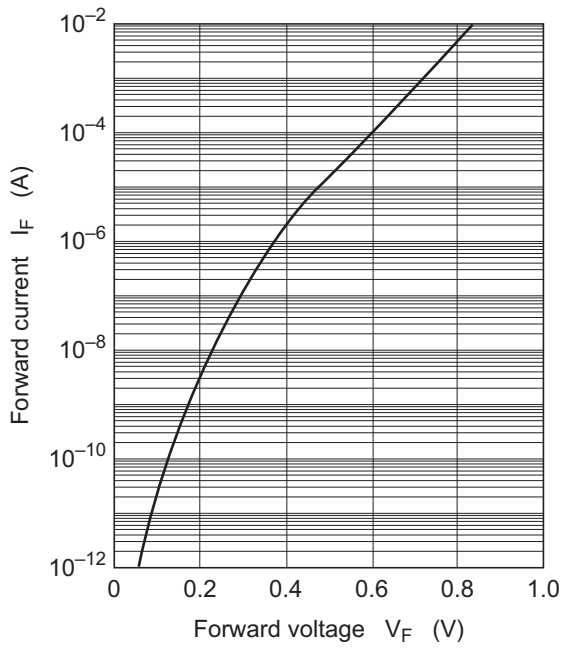


Fig.1 Forward current vs. Forward voltage

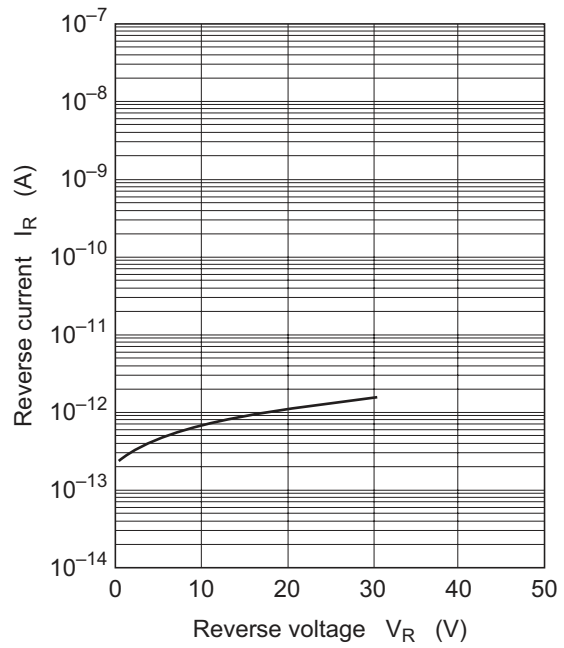


Fig.2 Reverse current vs. Reverse voltage

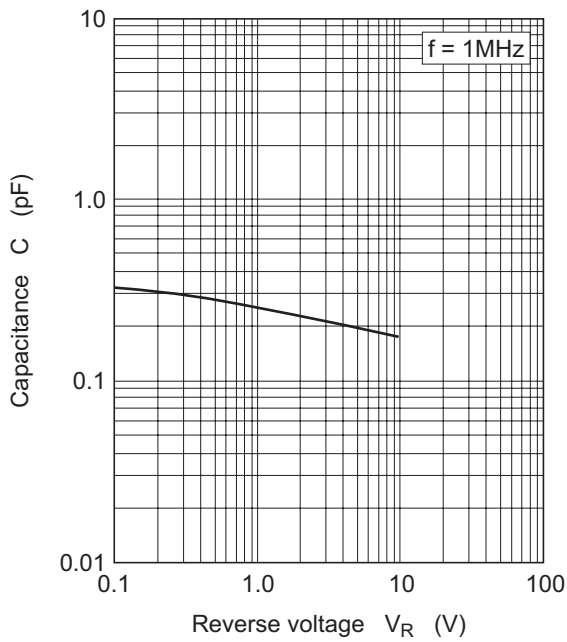


Fig.3 Capacitance vs. Reverse voltage

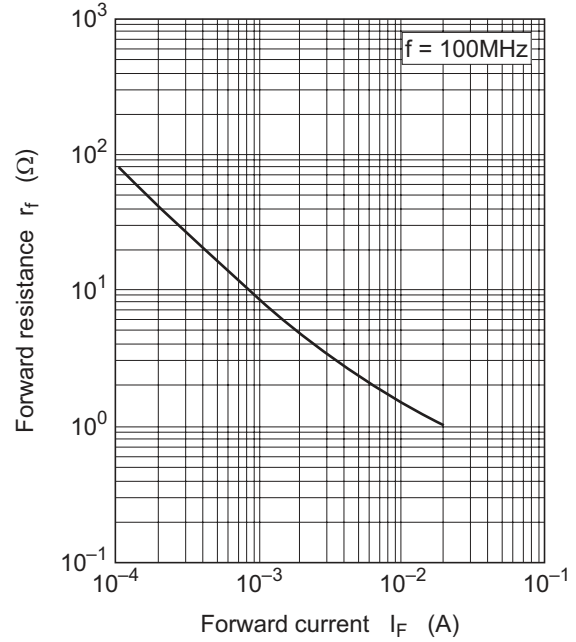
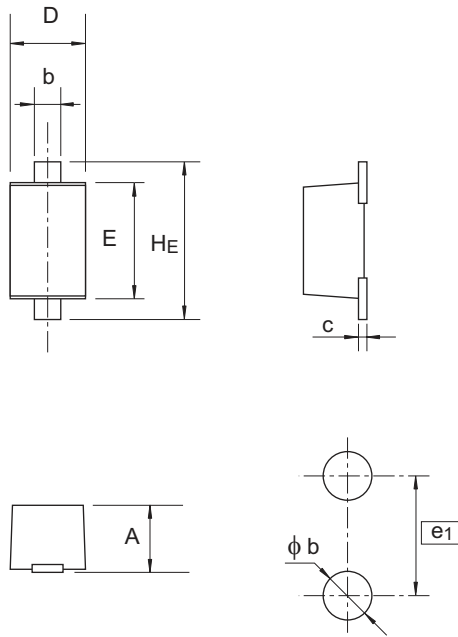


Fig.4 Forward resistance vs. Forward current

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SFP	—	PUSF0002ZB-A	SFP / SFPV	0.0010g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	—	0.55
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.90	1.00	1.10
H_E	1.30	1.40	1.50
ϕb	—	0.50	—
e_1	—	1.40	—

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April 1st, 2010
Renesas Electronics Corporation

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