

# CD74HC4538-Q1

## HIGH-SPEED CMOS LOGIC DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

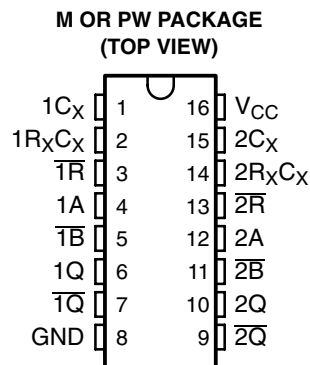
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- Qualified for Automotive Applications
- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of  $R_X$ ,  $C_X$
- Triggering From the Leading or Trailing Edge
- Q and  $\bar{Q}$  Buffered Outputs Available
- Separate Resets
- Wide Range of Output Pulse Widths
- Schmitt-Trigger Input on A and  $\bar{B}$  Inputs
- Retrigger Time Is Independent of  $C_X$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- $V_{CC}$  Voltage = 2 V to 6 V
- High Noise Immunity  $N_{IL}$  or  $N_{IH}$  = 30% of  $V_{CC}$ ,  $V_{CC} = 5$  V

### description/ordering information

The CD74HC4538 is a dual retriggerable/resettable precision monostable multivibrator for fixed-voltage timing applications. An external resistor ( $R_X$ ) and external capacitor ( $C_X$ ) control the timing and accuracy for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of  $R_X$  and  $C_X$ .

Leading-edge triggering (A) and trailing-edge triggering ( $\bar{B}$ ) inputs are provided for triggering from either edge of the input pulse. An unused A input should be tied to GND and an unused  $\bar{B}$  input should be tied to  $V_{CC}$ . On power up, the IC is reset. Unused resets and sections must be terminated. In normal operation, the circuit retriggers on the application of each new trigger pulse. To operate in the nontriggerable mode,  $\bar{Q}$  is connected to  $\bar{B}$  when leading-edge triggering (A) is used, or Q is connected to A when trailing-edge triggering ( $\bar{B}$ ) is used. The period ( $\tau$ ) can be calculated from  $\tau = (0.7) R_X C_X$ ;  $R_{MIN}$  is 5 k $\Omega$ .  $C_{MIN}$  is 0 pF.



### ORDERING INFORMATION<sup>†</sup>

$T_A$	PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC4538QM96Q1	HC4538M
	TSSOP – PW	Tape and reel	CD74HC4538QPWRQ1	HC4538M

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

<sup>‡</sup> Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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**TEXAS  
INSTRUMENTS**

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# CD74HC4538-Q1 HIGH-SPEED CMOS LOGIC DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

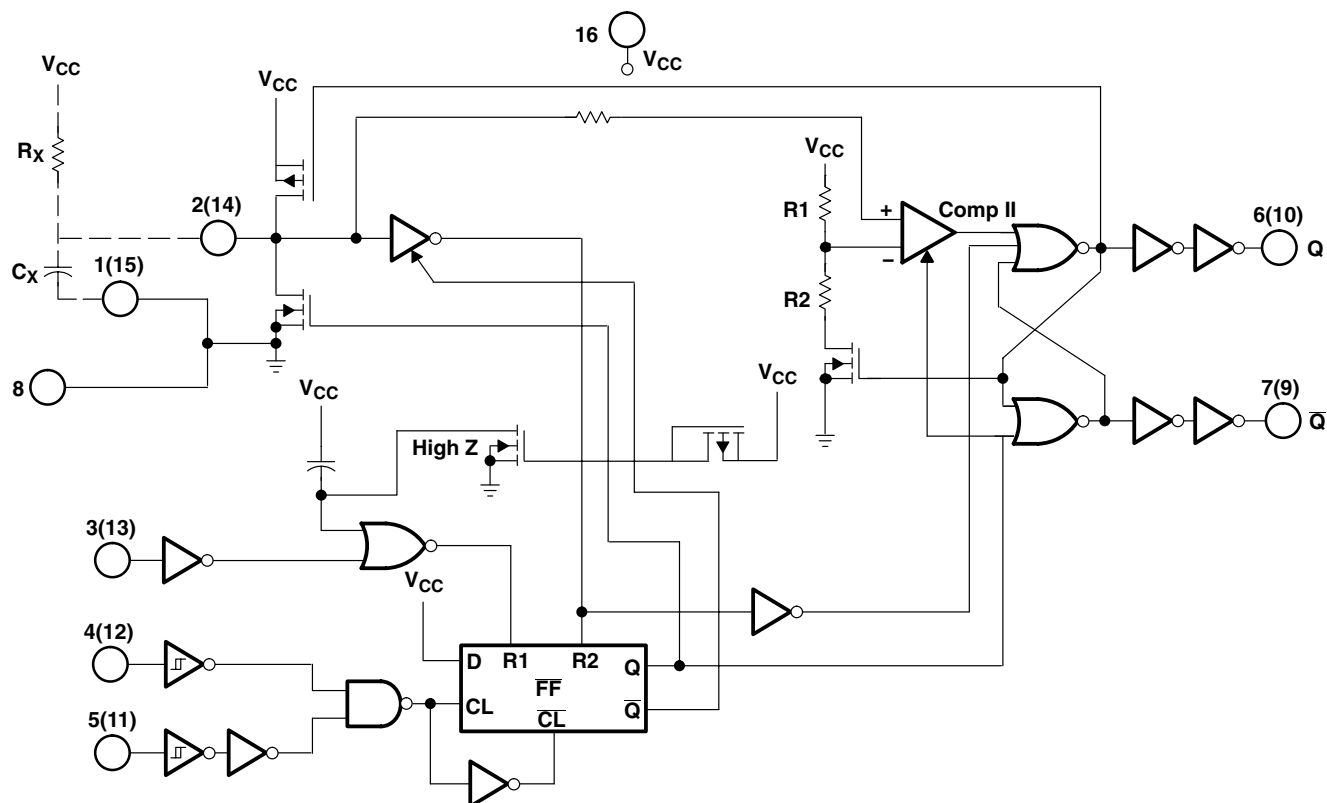
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FUNCTION TABLE

INPUTS			OUTPUTS	
R	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⌋	⌋
H	↑	H	⌋	⌋

NOTE: H = High voltage level  
 L = Low voltage level  
 ↑ = Transition from low to high level  
 ↓ = Transition from high to low level  
 ⌋ = one high-level pulse  
 ⌋ = one low-level pulse  
 X = Irrelevant

## logic diagram (positive logic)



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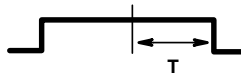
### FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V <sub>CC</sub> TO TERMINAL NUMBER		GND TO TERMINAL NUMBER		INPUT PULSE TO TERMINAL NUMBER		OTHER CONNECTIONS	
	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>
Leading-edge trigger/retriggerable	3, 5	11, 13			4	12		
Leading-edge trigger/nonretriggerable	3	13			4	12	5–7	11–9
Trailing-edge trigger/retriggerable	3	13	4	12	5	11		
Trailing-edge trigger/nonretriggerable	3	13			5	11	4–6	12–10

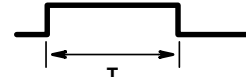
- NOTES: 1. A retriggerable one-shot multivibrator has an output pulse width that is extended one full time period (T) after application of the last trigger pulse.  
 2. A nonretriggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



Input Pulse Train



Retriggerable Mode  
Pulse Width (A Mode)



Nonretriggerable Mode  
Pulse Width (A Mode)

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 V to 7 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < –0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V)	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < –0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V)	±20 mA
Switch current per output pin, I <sub>O</sub> (V <sub>O</sub> > –0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V)	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): M package	73°C/W
PW package	108°C/W
Maximum junction temperature, T <sub>J</sub>	150°C
Lead temperature (during soldering):	
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max	300°C
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are referenced to GND, unless otherwise specified.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## HIGH-SPEED CMOS LOGIC DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

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### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
$V_{CC}$	Supply voltage		2	6	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V	
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 6\text{ V}$	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V	
		$V_{CC} = 4.5\text{ V}$		1.35		
		$V_{CC} = 6\text{ V}$		1.8		
$V_I$	Input voltage		0	$V_{CC}$	V	
$V_O$	Output voltage		0	$V_{CC}$	V	
$t_t$	Input transition (rise and fall) time	Reset input	$V_{CC} = 2\text{ V}$	0	1000	ns
			$V_{CC} = 4.5\text{ V}$	0	500	
			$V_{CC} = 6\text{ V}$	0	400	
	Trigger inputs A or $\bar{B}$	$V_{CC} = 2\text{ V}$	0	Unlimited		
		$V_{CC} = 4.5\text{ V}$	0	Unlimited		
		$V_{CC} = 6\text{ V}$	0	Unlimited		
$R_X$	External timing resistor (see Note 4)		5		k $\Omega$	
$C_X$	External timing capacitor (see Note 4)		0		F	
$T_A$	Operating free-air temperature		-40	125	$^{\circ}\text{C}$	

NOTES: 3. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4. The maximum allowable values of  $R_X$  and  $C_X$  are a function of leakage of capacitor  $C_X$ , leakage of the CD74HC4538, and leakage due to board layout and surface resistance. Values of  $R_X$  and  $C_X$  should be chosen so that the maximum current into pin 2 or pin 14 is 30 mA. Susceptibility to externally induced noise signals may occur for  $R_X > 1\text{ M}\Omega$ .



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		I <sub>O</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9	1.9	1.9			V	
				4.5 V	4.4	4.4	4.4				
				6 V	5.9	5.9	5.9				
		TTL loads		-4	4.5 V	3.98	3.84	3.7			
				-5.2	6 V	5.48	5.34	5.2			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V		0.1	0.1	0.1	V		
				4.5 V		0.1	0.1	0.1			
				6 V		0.1	0.1	0.1			
		TTL loads		4	4.5 V	0.26	0.33	0.4			
				5.2	6 V	0.26	0.33	0.4			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	A, $\bar{B}$ , R		6 V	±0.1	±1	±1	μA			
		R <sub>X</sub> C <sub>X</sub> (see Note 5)		6 V	±0.05	±0.5	±0.5				
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	Quiescent	0	6 V	8	80	160	μA			
		Active, Q = high, Pins 2 and 14 at V <sub>CC</sub> /4	0	6 V	0.6	0.8	1	mA			
C <sub>IN</sub>	C <sub>L</sub> = 50 pF				10	10	10	pF			

NOTE 5: When testing I<sub>I</sub>, the Q output must be high. If Q is low (device not triggered), the pullup P device is ON and the low-resistance path from V<sub>DD</sub> to the test pin causes a current far exceeding the specification.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub> Input pulse width	2 V	80			100	120		ns	
	4.5 V	16			20	24			
	6 V	14			17	20			
t <sub>SU</sub> Reset setup time	2 V	5			5	5		ns	
	4.5 V	5			5	5			
	6 V	5			5	5			
t <sub>rr</sub> Retrigger time (see Figure 4)	5 V		175					ns	
Output pulse-width match, same package			±1					%	



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, $\bar{B}$	Q or $\bar{Q}$	C <sub>L</sub> = 50 pF	2 V		250		315		375	ns	
				4.5 V		50		63		75		
				6 V		43		54		64		
	R	Q or $\bar{Q}$	C <sub>L</sub> = 15 pF	5 V		21						
				C <sub>L</sub> = 50 pF	2 V		250		315			375
					4.5 V		50		63			75
6 V		43			54		64					
C <sub>L</sub> = 15 pF	5 V		21									
	t <sub>t</sub>	C <sub>L</sub> = 50 pF	2 V		75		95		110	ns		
			4.5 V		15		19		22			
6 V				13		16		19				
τ <sup>†</sup>		C <sub>L</sub> = 50 pF	3 V	0.64	0.78	0.612	0.812	0.605	0.819	ms		
			5 V	0.63	0.77	0.602	0.798	0.595	0.805			

† Output pulse width with R<sub>X</sub> = 10 kΩ and C<sub>X</sub> = 0.1 μF

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, input t<sub>r</sub>, t<sub>f</sub> = 6 ns, C<sub>L</sub> = 15 pF

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance (see Note 6)	136	pF

NOTE 6: C<sub>pd</sub> is used to determine the dynamic power consumption, per one shot.

$$P_D = (C_{pd} + C_X) V_{CC}^2 f_I \Sigma(C_L V_{CC}^2 f_O)$$

f<sub>I</sub> = input frequency

f<sub>O</sub> = output frequency

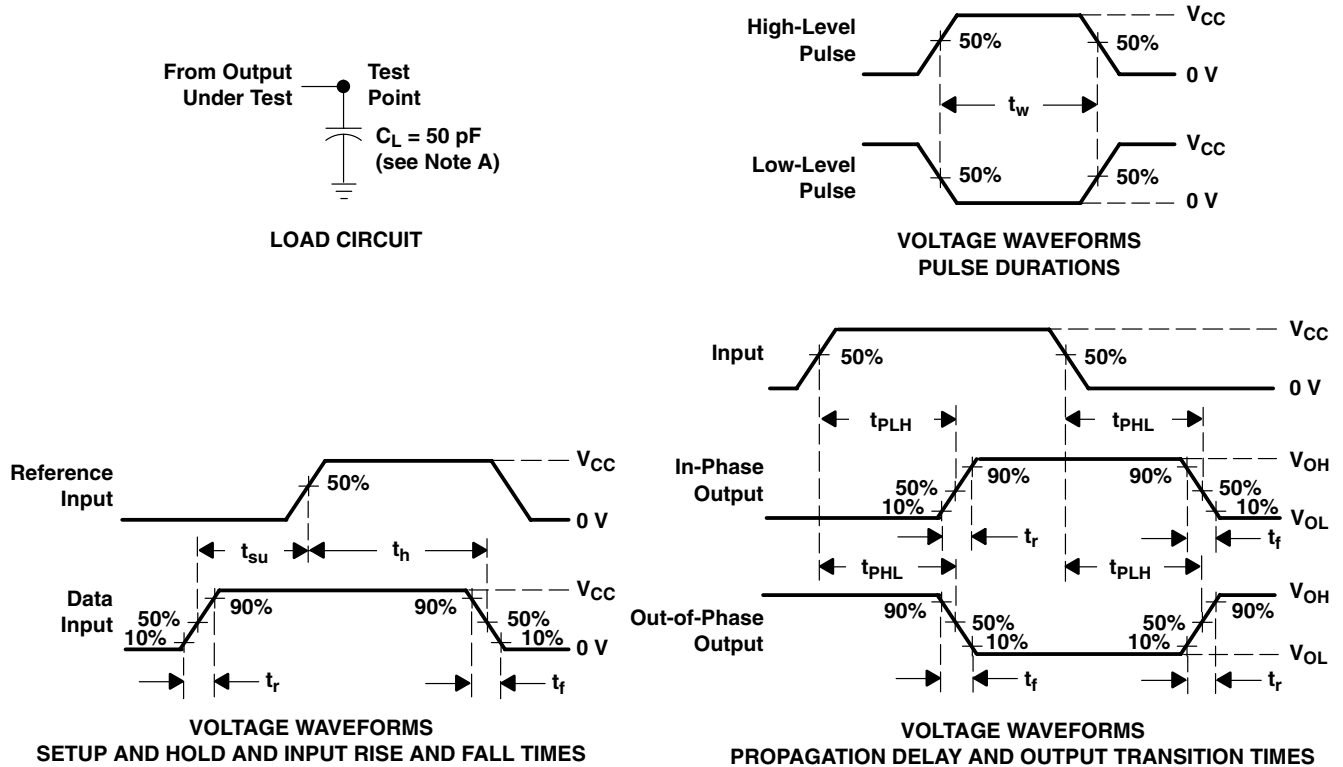
C<sub>L</sub> = output load capacitance

C<sub>X</sub> = external capacitance

V<sub>CC</sub> = supply voltage, assuming f<sub>I</sub> ≪ 1/τ



**PARAMETER MEASUREMENT INFORMATION**



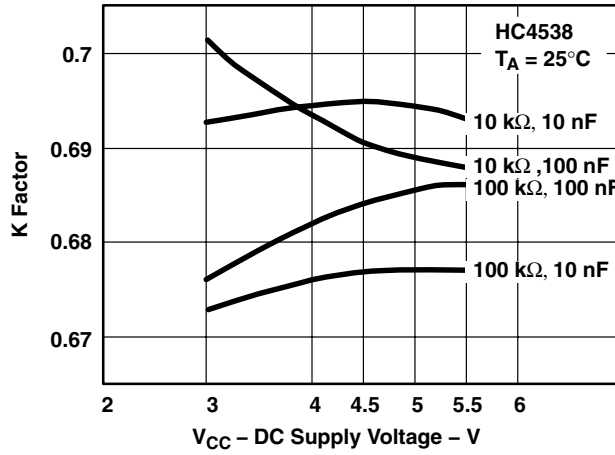
- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

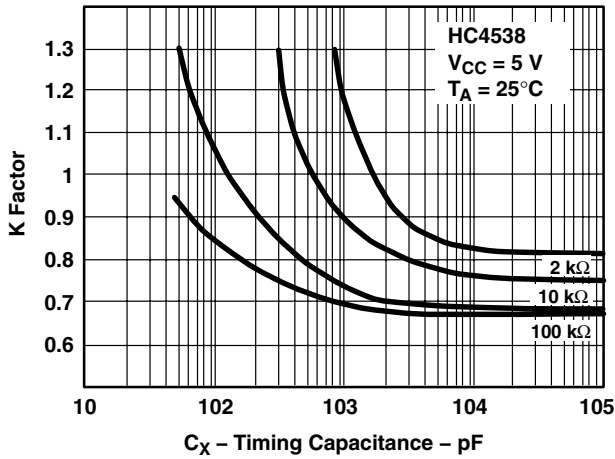
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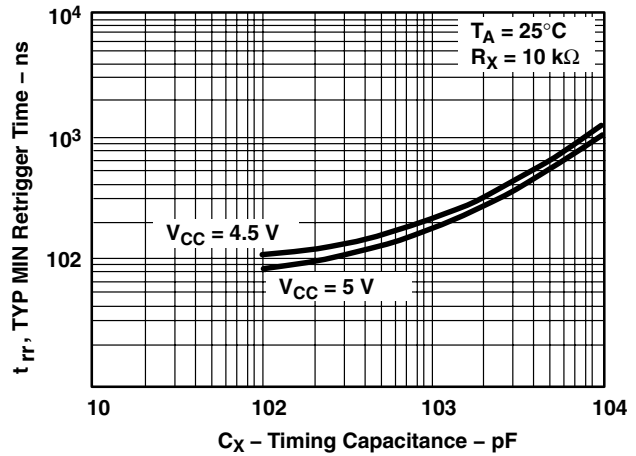
**TYPICAL CHARACTERISTICS**



**Figure 2. K Factor vs DC Supply Voltage**



**Figure 3. K Factor vs  $C_X$**



**Figure 4. Minimum Retrigger Time vs Timing Capacitance**

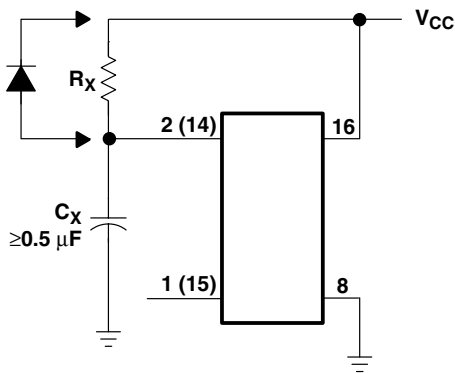


**TYPICAL APPLICATION DATA**

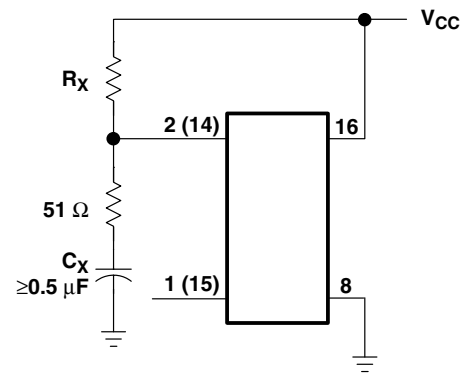
**power-down mode**

During a rapid power-down condition (as would occur with a power-supply short circuit with a poorly filtered power supply), the energy stored in  $C_X$  could discharge into pin 2 or pin 14. To avoid possible device damage in this mode when  $C_X$  is  $\geq 0.5 \mu\text{F}$ , a protection diode with a 1-A rating or higher (1N5395 or equivalent) and a separate ground return for  $C_X$  should be provided (see Figure 5).

An alternate protection method is shown in Figure 6, where a  $51\text{-}\Omega$  current-limiting resistor is inserted in series with  $C_X$ . Note that a small pulse-duration decrease occurs, however, and  $R_X$  must be increased appropriately to obtain the originally desired pulse duration.



**Figure 5. Rapid-Power-Down Protection Circuit**



**Figure 6. Alternative Rapid-Power-Down Protection Circuit**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4538QM96G4Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M	<a href="#">Samples</a>
CD74HC4538QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M	<a href="#">Samples</a>
CD74HC4538QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD74HC4538-Q1 :**

- Catalog: [CD74HC4538](#)
- Military: [CD54HC4538](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4538QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4538QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4538QPWRG4Q1	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4538QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0





4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

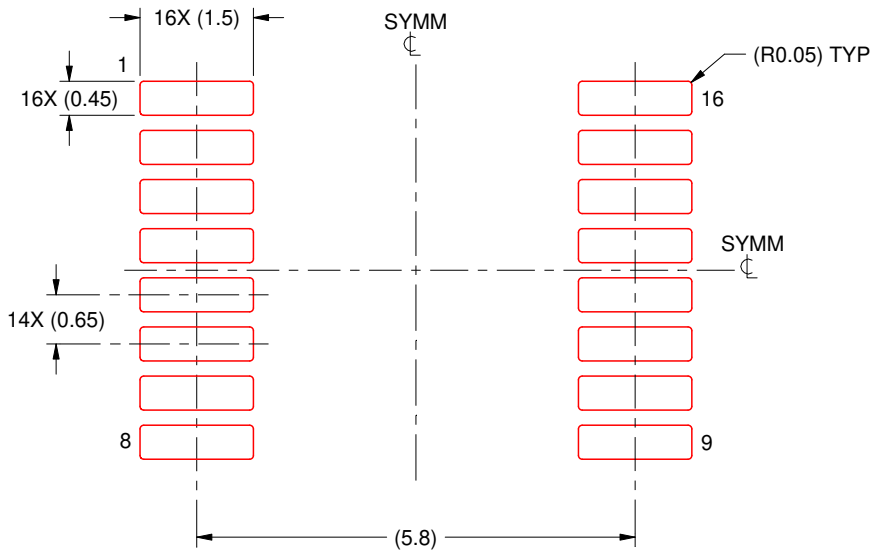


# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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